Migration Guide for i.MX31, i.MX27, and OMAP35x SOM-LVs

Application Note 375

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Abstract

This Application Note assists customers who want to design a custom baseboard that can support the i.MX31, i.MX27, and OMAP35x SOM-LV modules or update their existing baseboard to accommodate a different processor-based SOM-LV module. This document details the differences in the connector pin outs and feature sets between the three SOM-LV modules.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
1	Brad Brown	Internal draft	BB	06/27/08
A	Jed Anderson	Initial release	BB	10/08/08

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1 Introduction

Logic's System on Modules (SOMs) simplify development and provide the ability to easily upgrade to next generation hardware and software. The SOM-LV is a low-voltage module based on Freescale's i.MX and Texas Instruments' OMAP™ processors. This document will explain in-depth differences between the i.MX31, i.MX27, and the OMAP35x SOM-LVs to help in designing a custom baseboard that can accommodate all three modules.

Logic publishes an *Embedded Products Parametric Table* for a high-level description of the feature set available for every SOM we offer. Follow the link below to download a PDF of the Parametric Table.

- Embedded Products Parametric Table

1.1 Scope of Document

Though this document addresses the differences between the modules it is not intended to be all-inclusive. System designers should review the sets of schematics and any other applicable supporting documents for the i.MX31, i.MX27, and the OMAP35x SOM-LV modules before designing a baseboard that can utilize more than one of these products.

IMPORTANT NOTE: If there is ever a discrepancy between information within this document and the corresponding schematics, the schematics hold precedence.

2 References

2.1 Supporting Documents

Listed below are the links to the most current schematics for the i.MX31, i.MX27, and the OMAP35x SOM-LVs. Product registration is required to gain access to these documents. If you do not currently have a registered product, please contact your sales representative for access.

- i.MX31 SOM-LV Schematics
- i.MX27 SOM-LV Schematics
- OMAP35x SOM-LV Schematics

The Zoom Development Kits based on the i.MX31, i.MX27, and OMAP35x SOM-LVs all use the same LV baseboard (SDK2-APP-10).[1]

Table 2.1 lists the supporting documents that were used in the creation of this Application Note.

[1] The Zoom OMAP35x Development Kit uses a modified baseboard that has resistor R13 removed in order for the included 4.3" WQVGA LCD to work properly.

Table 2.1: Supporting Documents

Logic PN	Rev	Description
1005441	A	LV Baseboard (SDK2-APP-10) Schematic
1004734	11	i.MX31 SOM-LV Schematics
1009880	A	i.MX27 SOM-LV Schematics
1009917	A	OMAP35x SOM-LV Schematics
1009954	A	OMAP35x SOM-LV Hardware Specification
1005992	E	i.MX31 SOM-LV Hardware Specification
1007859	2	i.MX27 SOM-LV Hardware Specification
70000161	A	Interfacing LCDs to Logic's SDK Board AN 161
TI Literature #	**Version**	**Description**
SPRS505	-	OMAP3515/03 Applications Processor Datasheet
SPRUF98A	A	OMAP35x Multimedia Device Silicon Revision 2.0 and 2.1 TRM
SWCS019K	K	TPS65950 Integrated Power Management/Audio Codec Silicon Revision 3.1 Data Manual
SWCU026P	P	TPS65950 OMAP Power Management and System Companion Device Silicon Revision 3.1 TRM
Freescale Doc #	**Rev**	**Description**
MCIMX31RM	2.3	MCIMX31 and MCIMX31L Application Processor RM
MCIMX27RM	0.2	MCIMX27 Multimedia Application Processor RM
MC13783/D	3.4	MC13783 Power Management and Audio Circuit Data Sheet

2.2 Acronyms

AD-TFT	advanced thin film transistor (LCD technology)
AIC	analog interface chips
ATA	advanced technology attachment
BDM	background debug mode
BSP	board support package
CF	CompactFlash
CIR	consumer infrared
CODEC	coder/decoder
CPU	central processing unit
CSI	camera sensor interface
DC-DC	direct current to direct current converter
DSI	display serial interface
DSR	data set ready
DTR	data transmit ready
ETHER_RX	Ethernet receive signal
ETHER_TX	Ethernet transmit signal
FIR	fast infrared
GPIO	general purpose input or output
GPO	general purpose output
HR-TFT	high reflective thin film transistor (LCD technology)
i.MX27S	i.MX27 SOM-LV (only used within the tables of this document)
i.MX31S	i.MX31 SOM-LV (only used within the tables of this document)
I2C	Inter-integrated circuit bus
I2S	Inter-integrated circuit sound

IO or I/O	input/output signal
IrDA	infrared data association
IRQ	interrupt signal
JTAG	joint test action group
LCD	liquid crystal display
LDO	low dropout regulator
MAC	medium access control
MCBSP	multi-channel buffered serial port
MIR	medium infrared
MMC	multi-media card
OMAPS	OMAP35x SOM-LV (only used within the tables of this document)
PCM	pulse code modulation
PCMCIA	personal computer memory card international association
PHY	physical layer device
PMIC	power management integrated circuit
RFBI	remote frame buffer interface
SD	secure digital
SDI	TI Flatlink™ 3G serial display interface
SDIO	secure digital input/output
SIM	subscriber identity module
SIR	slow infrared
SOC	system-on-chip
SOM-LV	low-voltage System on Module
SPI	serial peripheral interface
STN	super-twisted nematic (STN) or passive matrix LCD technology
TDM	time division multiplexed
TFT	thin film transistor (TFT) or active matrix LCD technology
UART	universal asynchronous receiver/transmitter
uP	microprocessor (see SOC)

3 General Features Overview

This section gives a general feature set description of each SOM-LV module. Please refer to each module's *Hardware Specification* document for more detailed information about the physical specification requirements unique to that product.

Table 3.1: SOM-LV Comparison Overview

Specifications	i.MX31 SOM-LV	i.MX27 SOM-LV	OMAP35x SOM-LV
Form Factor	SOM-LV	SOM-LV	SOM-LV
Type	Type I	Type II	Type III
Size	59.1 x 76.2 x 7.9 mm	50.8 x 76.2 x 7.9 mm	31 x 76.2 x 7.4 mm
Available Software	Microsoft Windows Embedded CE Board Support Packages (BSPs)	Microsoft Windows Embedded CE BSPs	Microsoft Windows Embedded CE 6.0 BSPs Open source Linux BSP
RoHS	RoHS compliant	RoHS compliant	RoHS compliant
Temp	0˚C to 70˚C (commercial temp) or -30˚C to 85˚C (extended temp)	0˚C to 70˚C (commercial temp) or -20˚C to 85˚C (extended temp)	0˚C to 70˚C (commercial temp) or -40˚C to 85˚C (industrial temp)
ARM Core	ARM1136JF-S	ARM926EJ-S	Cortex-A8
Max Speed (MHz)	up to 532	up to 400	up to 600
Available SDRAM (MB)	64, 128*	64, 128*	128*, 256
Available NAND Flash (MB)	64	64	256*, 512
NOR Flash (MB)	2*, 4	2*, 4	0, 8*
Display	up to 800x600	up to 800x600	up to 1024x768
Touch Screen	Integrated 4-wire touch screen controller (Freescale MC13783)	Integrated 4-wire touch screen controller (Freescale MC13783)	Integrated 4-wire touchscreen controller (TSC2004)
Serial Ports	3	3	3
Audio	I2S compliant audio codec (Freescale MC13783; 16-bit stereo DAC, 13-bit ADC)	I2S compliant audio codec (Freescale MC13783; 16-bit stereo DAC, 13-bit ADC)	I2S compliant audio codec (16-bit stereo DAC, 13-bit ADC)
USB 2.0	yes	yes	yes
USB OTG	yes	yes	yes
MMC/SD	yes	yes	yes
ATA	yes	yes	no
TV Out	no	no	yes
CompactFlash Type 1	yes	yes	memory-mode only
10/100 Base-T Ethernet	available	yes	available
802.11b/g Ethernet	no	no	available
Bluetooth	no	no	available

* Standard configuration

available indicates the feature is present on some standard configurations of the SOM but not others. Please review the Standard SOM Configurations tables available on each product's webpage for details: www.logicpd.com.

3.1 Mechanical Specifications

All three SOM-LV modules use the same physical J1 and J2 connectors to mate to a baseboard. As is evidenced in Table 3.1 above, the physical size of each module varies; as such, special care should be taken when designing your platform to mate with different SOM-LV Types. Appendix A, at the conclusion of this document, shows the recommended baseboard footprint for all three SOM-LV modules, including the different mounting hole locations. See *White Paper 340: SOM-LV Mechanical Interface Specification* for more detail information about the connectors and physical sizes of the SOM-LV form factor.

Notes: The mounting hole dimension may differ between the SOMs; however, all production-level SOM-LVs will have the same hole diameter of 2.70 mm. Please refer to each respective SOM-LV *Product Change Notification* (PCN) document to determine when the change was made for each product. (The i.MX31 SOM-LV has always had mounting hole diameters at 2.70 mm.)

4 Pin Comparison

Tables comparing pin usage between the i.MX27, i.MX31, and the OMAP35x SOM-LVs can be found in the Appendices of this document; Appendix B compares pins for the J1 connector, Appendix C compares pins for the J2 connector.

5 PMIC Information

Throughout this document, the power management and audio codec components may be referred to by their common names as specified in Table 5.1 below.

Table 5.1: SOM-LV PMICs

Mfg Part #	Common Name	Description
MC13783	Atlas	Integrated power management and audio codec used on the i.MX31 and i.MX27 SOM-LVs
TPS65950	Triton2	Integrated power management and audio codec used on the OMAP35x SOM-LV

6 Detailed Interface Descriptions

The specific interfaces discussed in this document have been grouped into the following categories:

- Power/Reset/Clock/PWM Control Signals
- Memory Interfaces
- Removable Media Interfaces
- Communication Interfaces
- Graphic Interfaces

Notes about the tables used within this document:

1. Every attempt has been made to keep the tables readable at the default page magnification level. However, some tables will require you to use the Adobe Acrobat magnifying feature to properly view all the information.

2. Certain signals covered in this document may operate at different reference voltages on each SOM-LV module; therefore, these different voltages need to be called out within the tables describing those signals. To achieve this, signals are listed below the voltage domain in which they are located. Please see Table 6.1 below for an example of a table describing two signals in two different voltage domains. Notice that the CSPI3_SCLK and CSPI3_SS1 signals on the i.MX31 SOM-LV are on two different voltage domains (1.8V_NVCC10 and 2.7V_NVCC5/NVCC8 respectively). However, also notice that the similar signals on the i.MX27, CSPI3_SCLK and CSPI3_SS, both exist on the same voltage domain, VMMC1; this is indicated by the voltage domain field for the CSPI3_SS stating “same as above”.

Table 6.1: Example of Signals in Different Voltage Domains

		i.MX31 SOM-LV					i.MX27 SOM-LV			
SPI Signal	SOM-LV Signal	i.MX31 Signal	Primary	J1/J2 Pin	Voltage	SOM-LV Signal	i.MX27 signal	Primary	J1/J2 Pin	Voltage
Reference Voltage Reg / Domain	-	SW2BOUT (BUCK) / 1.8V_NVCC10	-	-	-	-	VMMC1(LDO) / VMMC1	-	J2.138	-
SCLK	uP_UARTC_CTS	CSPI3_SCLK	Alternate	J1.122	1.8	SD1_CLK	CSPI3_SCLK	Alternate	J2.136	-
Reference Voltage Reg / Domain	-	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	J1.152, J2.96	2.7	-	same as above	-	-	-
CS0	-	-	-	-	-	SD1_DATA3	CSPI3_SS	Alternate	J2.124	-
CS1	uP_CSPI2_SS1	CSPI3_SS1	Alternate	J2.89	2.7	-	-	-	-	-

6.1 Power/Reset/Clock/PWM Control Signals

The i.MX31, i.MX27, and the OMAP35x SOM-LVs all use the nSTANDBY, nSUSPEND, and 3.3_nEN control signals for power. All modules also have the same RESET control signals, such as uP_SW_nRESET, RESET_nOUT, and MSTR_nRST, with the same functionality. There are some control signals that are made available and are different from each module. See Table 6.2 for detailed differences.

Table 6.2: SOM-LV Power/Reset/Clock/PWM Interface

PWR/RST/CLK Control Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		SOM-LV Signal	Voltage	SOM-LV Signal	Voltage	SOM-LV Signal	Voltage
Power Control Signals							
PWR_ON	J1.30	PWR_ON	2.7	PWR_ON	2.7	-	-
nSTANDBY	J1.17	nSTANDBY	2.7	nSTANDBY	2.7	nSTANDBY	1.8
nSUSPEND	J1.15	nSUSPEND	2.7	nSUSPEND	2.7	nSUSPEND	1.8
3.3V_nEN	J1.49	3.3_nEN	2.7	3.3_nEN	2.7	3.3_nEN (DGND)	1.8 [3]
VIBRA_M	J2.75	-	-	-	-	VIBRA_M	MAIN_BATT
VIBRA_P	J2.77	-	-	-	-	VIBRA_P	MAIN_BATT
RFID_EN	J2.89	different function[1]	2.7	-	-	RFID_EN	Variable[4]
VAUX3	J2.175	different function[2]	max 5.5	different function[2]	max 5.5	VAUX3	Variable[5]
T2_REGEN	J2.193	different function[2]	max 5.5	different function[2]	max 5.5	T2_REGEN	MAIN_BATT
Reset Control Signals							
uP_SW_nRESET	J1.223	uP_SW_nRESET	2.7	uP_SW_nRESET	1.8	uP_SW_nRESET	1.8
RESET_nOUT	J1.225	RESET_OUT	1.8	RESET_OUT	1.8	RESET_OUT	1.8
MSTR_nRST	J1.227	MSTR_nRST	1.8	MSTR_nRST	1.8	MSTR_nRST	1.8
Clock Signals							
uP_AUX_CLK	J1.28	uP_AUX_CLK	1.8	uP_AUX_CLK	1.8	-	-
uP_CLKOUT1_26MHz	J2.233	-	-	-	-	uP_CLKOUT1_26MHz	1.8
TWL_32K_CLK_OUT	J2.234	-	-	-	-	TWL_32K_CLK_OUT	1.8
PWM Signal							
PWM0	J1.168	PWM0	2.7	PWM0	1.8	PWM0	1.8

Note(s):
1. i.MX31/RFID_EN - Signal name is uP_CSPI2_SS1 and can function as CSPI1_SS3 or CSPI3_SS1.
2. i.MX31/27 (J2.177/175) - Signal function is LED Drive
3. OMAP35x/3.3_nEN signal input is in the 1.8 voltage domain but its input is tied to DGND.
4. OMAP35x/RFID_EN connects to the PMIC VMMC2.OUT Level
5. OMAP35x/VAUX3 connects to the PMIC VAUX3.OUT Level

6.2 Memory Interfaces

The available memory interfaces are the static memory bus interface and the ATA interface.

6.2.1 Static Memory Bus Interface

The i.MX31, i.MX27, and OMAP35x SOM-LVs route the 16-bit data bus with 25 address pins to the J1 connector. On the i.MX31 and i.MX27 SOM-LVs, the data bus (D15–D0) and the upper address lines (A24–A13) route directly to the processors, but the lower address lines (MA12–MA0) are buffered on both SOMs. On the OMAP35x SOM-LV, address lines (A16–A1) are latched using uP_nADV_ALE, while the remaining upper address lines (A26–A17) route directly to the processor.

The chip selects on all three SOMs have similarly defined functionality and have been routed to the same pins on the connectors.

The i.MX31 and OMAP35x SOM-LVs have two external DMA request pins. The i.MX27 SOM-LV does not support external DMA requests.

The OMAP35x general-purpose memory controller (GPMC) is the OMAP2 unified memory controller (UMC) dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices;
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices;
- NAND flash;
- Pseudo-SRAM devices.

The i.MX27 and i.MX31 Wireless External Interface Memory Controller (WEIM) supports the following:

- 16-bit SRAM memories;
- 16-bit PSRAM (up to 133 MHz) memories;
- 16-bit NOR flash memories.

Table 6.3: SOM-LV Memory Interface

Memory Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
		SOM-LV Signal	i.MX31 Signal	Voltage	SOM-LV Signal	i.MX27 signal	Voltage	SOM-LV Signal	OMAP35x Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: - i.MX27S: J1.183, J2.96, J2.122 OMAPS: J1:110,144,152 / J2:54,96,122	SW2BOUT (BUCK) / 1.8V_NVCC10	NVCC10	-	SW2BOUT (REG) / DVDD_1.8V	NVDD1	1.8	VIO.SW (REG) / VIO_1V8	vdds vdds_mem	1.8
BOOT_nCS	J2.172	BOOT_nCS	CS0 [1]	1.8	BOOT_nCS	CS0 [1]	1.8	BOOT_nCS	GPMC_nCS2 [1]	1.8
FLASH_nCS/NOR_nCS	on board flash	FLASH_nCS	CS0 [1]	1.8	FLASH_nCS	CS0 [1]	1.8	NOR_nCS	GPMC_nCS2 [1]	1.8
EXT_BOOT_nSELECT	J2.168	EXT_BOOT_nSELECT	-	1.8	EXT_BOOT_nSELECT	-	1.8	EXT_BOOT_nSELECT	-	1.8
SLOW_nCS/uP_nCS_A_EXT	J1.145	SLOW_nCS	CS5	1.8	SLOW_nCS	CS5	1.8	uP_nCS_B_EXT	GPMC_nCS5	1.8
BUFF_nOE_DATA	J1.121	BUFF_nOE_DATA	-	1.8	BUFF_nOE_DATA	-	1.8	-	-	-
BUFF_DIR_DATA	J1.123	BUFF_DIR_DATA	-	1.8	BUFF_DIR_DATA	-	1.8	BUFF_DIR_DATA	GPMC_IODIR	1.8
D0	J1.40	uP_D0	D0	1.8	uP_D0	D0	1.8	uP_D0	GPMC_D0	1.8
D1	J1.42	uP_D1	D1	1.8	uP_D1	D1	1.8	uP_D1	GPMC_D1	1.8
D2	J1.44	uP_D2	D2	1.8	uP_D2	D2	1.8	uP_D2	GPMC_D2	1.8
D3	J1.46	uP_D3	D3	1.8	uP_D3	D3	1.8	uP_D3	GPMC_D3	1.8
D4	J1.48	uP_D4	D4	1.8	uP_D4	D4	1.8	uP_D4	GPMC_D4	1.8
D5	J1.50	uP_D5	D5	1.8	uP_D5	D5	1.8	uP_D5	GPMC_D5	1.8
D6	J1.54	uP_D6	D6	1.8	uP_D6	D6	1.8	uP_D6	GPMC_D6	1.8
D7	J1.56	uP_D7	D7	1.8	uP_D7	D7	1.8	uP_D7	GPMC_D7	1.8
D8	J1.58	uP_D8	D8	1.8	uP_D8	D8	1.8	uP_D8	GPMC_D8	1.8
D9	J1.60	uP_D9	D9	1.8	uP_D9	D9	1.8	uP_D9	GPMC_D9	1.8
D10	J1.62	uP_D10	D10	1.8	uP_D10	D10	1.8	uP_D10	GPMC_D10	1.8
D11	J1.64	uP_D11	D11	1.8	uP_D11	D11	1.8	uP_D11	GPMC_D11	1.8
D12	J1.66	uP_D12	D12	1.8	uP_D12	D12	1.8	uP_D12	GPMC_D12	1.8
D13	J1.68	uP_D13	D13	1.8	uP_D13	D13	1.8	uP_D13	GPMC_D13	1.8
D14	J1.70	uP_D14	D14	1.8	uP_D14	D14	1.8	uP_D14	GPMC_D14	1.8
D15	J1.74	uP_D15	D15	1.8	uP_D15	D15	1.8	uP_D15	GPMC_D15	1.8
uP_nADV_ALE	J2.87	different function [4]	-	-	-	-	-	uP_nADV_ALE	GPMC_nADV_ALE	1.8
uP_WP	J2.85	different function [6]	-	-	-	-	-	uP_WP	GPMC_nWP	1.8
Reference Voltage Reg / Domain	i.MX31S: J1.110 i.MX27S: J2.122 OMAPS: J1:110,144,152 / J2:54,96,122	SW2AOUT (BUCK) / 1.8V_DDR	NVCC2 NVCC22	1.8	same as above	NVDD2/NVDD3	1.8	same as above	vdds vdds_mem	1.8
uP_nCS_A_EXT	J1.143	uP_nCS_A_EXT	CS1	1.8	uP_nCS_A_EXT	CS1_B	1.8	uP_nCS_A_EXT	GPMC_nCS4	1.8
uP_nCS_B_EXT	J1.141	uP_nCS_B_EXT	CS3	1.8	uP_nCS_B_EXT	CS3_B/CSD1	1.8	uP_nCS_B_EXT	GPMC_nCS5	1.8
FAST_nCS/uP_nCS_A_EXT	J1.147	FAST_nCS	CS4 [2]	1.8	FAST_nCS	CS4_B/ETMTRACESYNC	1.8	uP_nCS_A_EXT	GPMC_nCS4	1.8
WRLAN_nCS	on board wrlan	WRLAN_nCS	CS4 [2]	1.8	-	-	-	uP_nCS1/uP_nMCS1	GPMC_nCS1	1.8
EB0	J1.137	uP_EB0	EB0	1.8	uP_nEB0	EB0_B	1.8	uP_nBE0	GPMC_nBE0_CLE	1.8
EB1	J1.139	uP_EB1	EB1	1.8	uP_nEB1	EB1_B	1.8	uP_nBE1	GPMC_nBE1	1.8
OE	J1.125	uP_OE	OE	1.8	uP_nOE	OE_B	1.8	uP_nOE	GPMC_nOE	1.8
RW	J1.127	uP_RnW	RW	1.8	uP_RnW	RW_B	1.8	uP_nWE	GPMC_nWE	1.8
LBA	J2.14	uP_nLBA	LBA	1.8	uP_nLBA	LBA_B	1.8	different function [5]	-	1.8
BCLK	J1.131	uP_BUS_CLK	BCLK	1.8	uP_BUS_CLK	BCLK	1.8	uP_BUS_CLK	GPMC_CLK	1.8
ECB/WAIT	J1.109	uP_nWAIT	ECB	1.8	uP_nWAIT	ECB_B	1.8	uP_nWAIT	GPMC_WAIT1	1.8
A0	J1.53	DGND	DGND	DGND	DGND	DGND	DGND	DGND	-	DGND
A1	J1.55	uP_MA0	A0	1.8	uP_MA0	A0 [3]	1.8	uP_LA1	GPMC_D0	1.8
A2	J1.57	uP_MA1	A1	1.8	uP_MA1	A1 [3]	1.8	uP_LA2	GPMC_D1	1.8
A3	J1.59	uP_MA2	A2	1.8	uP_MA2	A2 [3]	1.8	uP_LA3	GPMC_D2	1.8
A4	J1.61	uP_MA3	A3	1.8	uP_MA3	A3 [3]	1.8	uP_LA4	GPMC_D3	1.8
A5	J1.63	uP_MA4	A4	1.8	uP_MA4	A4 [3]	1.8	uP_LA5	GPMC_D4	1.8
A6	J1.65	uP_MA5	A5	1.8	uP_MA5	A5 [3]	1.8	uP_LA6	GPMC_D5	1.8
A7	J1.67	uP_MA6	A6	1.8	uP_MA6	A6 [3]	1.8	uP_LA7	GPMC_D6	1.8

Table 6.3: SOM-LV Memory Interface (continued)

Memory Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
		SOM-LV Signal	i.MX31 Signal	Voltage	SOM-LV Signal	i.MX27 signal	Voltage	SOM-LV Signal	OMAP35x Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: J1.110 i.MX27S: J2.122 OMAPS: J1:110,144,152 / J2:54,96,122	SW2AOUT (BUCK) / 1.8V_DDR	NVCC2 NVCC22	1.8	same as above	NVDD2/NVDD3	1.8	same as above	vdds vdds_mem	1.8
A8	J1.69	uP_MA7	A7	1.8	uP_MA7	A7 [3]	1.8	uP_LA8	GPMC_D7	1.8
A9	J1.73	uP_MA8	A8	1.8	uP_MA8	A8 [3]	1.8	uP_LA9	GPMC_D8	1.8
A10	J1.75	uP_MA9	A9	1.8	uP_MA9	A9 [3]	1.8	uP_LA10	GPMC_D9	1.8
A11	J1.77	uP_MA10	A10	1.8	uP_MA10	A10 [3]	1.8	uP_LA11	GPMC_D10	1.8
A12	J1.79	uP_MA11	A11	1.8	uP_MA11	A11 [3]	1.8	uP_LA12	GPMC_D11	1.8
A13	J1.81	uP_MA12	A12	1.8	uP_MA12	A12 [3]	1.8	uP_LA13	GPMC_D12	1.8
A14	J1.83	uP_A13	A13	1.8	uP_A13	A13 [3]	1.8	uP_LA14	GPMC_D13	1.8
A15	J1.85	uP_A14	A14	1.8	uP_A14	A14 [3]	1.8	uP_LA15	GPMC_D14	1.8
A16	J1.87	uP_A15	A15	1.8	uP_A15	A15 [3]	1.8	uP_LA16	GPMC_D15	1.8
A17	J1.89	uP_A16	A16	1.8	uP_A16	A16 [3]	1.8	uP_A1	GPMC_A1	1.8
A18	J1.93	uP_A17	A17	1.8	uP_A17	A17 [3]	1.8	uP_A2	GPMC_A2	1.8
A19	J1.95	uP_A18	A18	1.8	uP_A18	A18 [3]	1.8	uP_A3	GPMC_A3	1.8
A20	J1.97	uP_A19	A19	1.8	uP_A19	A19 [3]	1.8	uP_A4	GPMC_A4	1.8
A21	J1.99	uP_A20	A20	1.8	uP_A20	A20 [3]	1.8	uP_A5	GPMC_A5	1.8
A22	J1.101	uP_A21	A21	1.8	uP_A21	A21 [3]	1.8	uP_A6	GPMC_A6	1.8
A23	J1.103	uP_A22	A22	1.8	uP_A22	A22 [3]	1.8	uP_A7	GPMC_A7	1.8
A24	J1.105	uP_A23	A23	1.8	uP_A23	A23 [3]	1.8	uP_A8	GPMC_A8	1.8
A25	J1.107	uP_A24	A24	1.8	uP_A24	A24 [3]	1.8	uP_A9	GPMC_A9	1.8
A26	J2.56	uP_A25	A25	1.8	uP_A25	A25 [3]	1.8	uP_A10	GPMC_A10	1.8
D16	J1.76	-	-	-	-	-	-	-	-	-
D17	J1.78	-	-	-	-	-	-	-	-	-
D18	J1.80	-	-	-	-	-	-	-	-	-
D19	J1.82	-	-	-	-	-	-	-	-	-
D20	J1.84	-	-	-	-	-	-	-	-	-
D21	J1.86	-	-	-	-	-	-	-	-	-
D22	J1.88	-	-	-	-	-	-	-	-	-
D23	J1.90	-	-	-	-	-	-	-	-	-
D24	J1.94	-	-	-	-	-	-	-	-	-
D25	J1.96	-	-	-	-	-	-	-	-	-
D26	J1.98	-	-	-	-	-	-	-	-	-
D27	J1.100	-	-	-	-	-	-	-	-	-
D28	J1.102	-	-	-	-	-	-	-	-	-
D29	J1.104	-	-	-	-	-	-	-	-	-
D30	J1.106	-	-	-	-	-	-	-	-	-
D31	J1.108	-	-	-	-	-	-	-	-	-
Reference Voltage Reg / Domain	i.MX31: J1.183 OMAPS: J1:110,144,152 / J2:54,96,122	VIOLO (Reg) / 1.8V_NVCC7	NVCC7	1.8	-	-	-	same as above	vdds vdds_mem	1.8
uP_DREQ0	J1.133	uP_DREQ0	EXTDMA_0		-	-	-	uP_DREQ0	SYS_nDMAREQ3	1.8
uP_DREQ1	J1.135	uP_DREQ1	EXTDMA_1		-	-	-	uP_DREQ1	SYS_nDMAREQ1	1.8

Note(s):
1. See information on EXT_BOOT_nSELECT in the *SOM-LV Hardware Specification Manual* for select of nCS.
2. See information on FAST_nCS and WRLAN_nCS in the *i.MX31 SOM-LV Hardware Specification Manual.*
3. Signal is buffered.
4. i.MX31/uP_nADV_ALE - Signal function is CSPI2_SS2/I2C3_SDA/IPU_FLS_STRB and voltage domain for this signal is 2.7V_NVCC5/NVCC8.
5. OMAP35x Signal Function is uP_nOE. This is the same function with regards to the PCMCIA/CF, but does not function as the LBA as on the i.MX31.
6. i.MX31/uP_WP - Signal function is uP_CSPI2_RDY, not useful for the i.MX31.

6.2.2 ATA Interface

The ATA interface is muxed behind different interfaces on the i.MX31 and i.MX27 processors; the OMAP35x does not have an ATA controller. On the i.MX31 SOM-LV, the ATA interface is shared with the camera interface, PWM0, Keypad, and I2C port 1; on the i.MX27 SOM-LV, the ATA interface is shared with the Ethernet MAC interface to the PHY and the PCMCIA control signals. This sharing makes these interfaces mutually exclusive on the SOMs. See Table 6.4 below for the ATA interface common pins on the SOMs.

Table 6.4: SOM-LV ATA Interface

ATA Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV		
		SOM-LV Signal	uP Signal	Voltage	SOM-LV Signal	uP Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: J2.54, J2.80 i.MX27S: J1.183, J2.96, J2.122	VMMC2 (LDO) / NVCC3	NVCC3	2.8	SW2BOUT (REG) / DVDD_1.8V	NVDD5	1.8
ATA_RESET	J2.59	ATA_RESET	ATA_RESET_B	2.8	uP_PCC_RESET/ATA_nRESET	ATA_RESET_B	1.8
ATA_DIOR	J2.65	CSI_D2	ATA_DIOR	2.8	uP_PCC_CD1/ATA_DIOR	ATA_DIOR	1.8
ATA_DIOW	J2.63	CSI_D3	ATA_DIOW	2.8	uP_PCC_CD2/ATA_DIOW	ATA_DIOW	1.8
ATA_CS1	J2.67	CSI_D1	ATA_CS1	2.8	uP_PCC_nWAIT/ATA_CS1	ATA_CS1	1.8
ATA_CS0	J2.69	CSI_D0	ATA_CS0	2.8	uP_PCC_RDYA/ATA_CS0	ATA_CS0	1.8
ATA_DMACK	J2.61	ATA_DMACK	ATA_DMACK	2.8	uP_PCC_BVD2_DMACK	ATA_DMACK	1.8
ATA_IORDY	J2.57	PWM0	ATA_IORDY	2.8	uP_PCC_RESET/ATA_nRESET	ATA_IORDY	1.8
Reference Voltage Reg / Domain	i.MX31: J2.122 i.MX27S: J1.183, J2.96, J2.122	VRF1 (REG) / 2.7V_NVCC6/NVCC9	NVCC6	2.7	same as above	NVDD5	1.8
ATA_DA2	J2.93	PCC_PCMCIA_nEN[2]	ATA_DA2	2.7	PC_PWRON/ATA_DA2	ATA_DA2	1.8
ATA_DA1	J2.95	KEY_COL6	ATA_DA1	2.7	uP_PCC_VS1/ATA_DA1	ATA_DA1	1.8
ATA_DA0	J2.97	KEY_COL5	ATA_DA0	2.7	uP_PCC_VS2/ATA_DA0	ATA_DA0	1.8
ATA_DMARQ	J2.99	KEY_COL4	ATA_DMARQ	2.7	uP_PCC_BVD1/ATA_DMARQ	ATA_DMARQ	1.8
ATA_INTRQ	J2.113	KEY_ROW6	ATA_INTRQ	2.7	uP_PCC_nIOIS16/ATA_INTRQ	ATA_INTRQ	1.8
ATA_BUFFER_DIR[1]	J2.109	KEY_ROW7	ATA_BUF_EN	2.7	uP_PC_POE/ATA_BUFFER_EN	ATA_BUFFER_EN	1.8
Reference Voltage Reg / Domain	i.MX31S: J1.144, J2.173 i.MX27S: J1.183, J2.96, J2.122	VCAM (REG) / NVCC4	NVCC4	2.8	same as above	NVDD6	1.8
ATA_DATA0	J2.55	CSI_D6	ATA_D0	2.8	uP_ATA_D0	ATA_D0	1.8
ATA_DATA1	J2.53	CSI_D7	ATA_D1	2.8	uP_ATA_D1	ATA_D1	1.8
ATA_DATA2	J2.49	CSI_D8	ATA_D2	2.8	uP_ATA_D2	ATA_D2	1.8
ATA_DATA3	J2.47	CSI_D9	ATA_D3	2.8	uP_ATA_D3	ATA_D3	1.8
ATA_DATA4	J2.45	CSI_D10	ATA_D4	2.8	uP_ATA_D4	ATA_D4	1.8
ATA_DATA5	J2.43	CSI_D11	ATA_D5	2.8	uP_ATA_D5	ATA_D5	1.8
ATA_DATA6	J2.41	CSI_D12	ATA_D6	2.8	uP_ATA_D6	ATA_D6	1.8
ATA_DATA7	J2.39	CSI_D13	ATA_D7	2.8	uP_ATA_D7	ATA_D7	1.8
ATA_DATA8	J2.37	CSI_D14	ATA_D8	2.8	uP_ATA_D8	ATA_D8	1.8
ATA_DATA9	J2.35	CSI_D15	ATA_D9	2.8	uP_ATA_D9	ATA_D9	1.8
ATA_DATA10	J2.33	CSI_MCLK	ATA_D10	2.8	uP_ATA_D10	ATA_D10	1.8
ATA_DATA11	J2.29	CSI_VSYNC	ATA_D11	2.8	uP_ATA_D11	ATA_D11	1.8
ATA_DATA12	J2.27	CSI_HSYNC	ATA_D12	2.8	uP_ATA_D12	ATA_D12	1.8
ATA_DATA13	J2.25	CSI_PCLK	ATA_D13	2.8	uP_ATA_D13	ATA_D13	1.8
ATA_DATA14	J2.23	I2C1_CLK	ATA_D14	2..8	uP_ATA_D14	ATA_D14	1.8
ATA_DATA15	J2.21	I2C1_DATA	ATA_D15	2.8	uP_ATA_D15	ATA_D15	1.8

Note(s):
1. An optional 74xxx245 bus transceiver can be placed between the host side of the data bus and the device side of the data bus. If the transceiver is used, its enable should be tied low (always enable) and its direction pin should be tied to ATA_BUFFER_EN in such a way that it drives from host to device when ATA_BUFFER_EN is high and drives from device to host when ATA_BUFFER_EN is low.
2. ATA and PCMCIA/CF cannot co-exist.

6.3 Removable Media Interfaces

Three removable media interface types exist for each SOM-LV: PCMCIA/CF, MMC/SD, and SIM. The following sections will cover these interfaces in more detail.

6.3.1 PCMCIA/CF Card Interface

The i.MX31 and i.MX27 SOM-LVs bring all the PCMCIA/CF control signals down to the baseboard and support I/O, memory, and attribute accesses to PCMCIA and CompactFlash cards. Both SOMs can support simultaneous use of PCMCIA and CompactFlash cards, as long as only one card requires access to memory-only space.

The OMAP35x SOM-LV only supports memory-only accesses to a single PCMCIA or CompactFlash card.

The host controller for the i.MX31 and i.MX27 supports the following specifications:

- PCMCIA
  - Support for PCMCIA Rel 2.1
  - CompactFlash
  - PC Card
  - TrueID Mode

Below is a table that shows the routing of the signals required depending on the desired card and the desired access of the target card being used.

Table 6.5: SOM-LV PCMCIA/CompactFlash Card Interface

CF Signals	SOM-LV J1/J2 Pin	PCMCIA/CF (I/O & Memory) i.MX Only	PCMCIA/CF (Memory Only) i.MX Only	PCMCIA/CF (Memory Only) OMAP35x	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
					SOM-LV Signal	uP Signal	Voltage	SOM-LV Signal	uP Signal	Voltage	SOM-LV Signal	uP Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: J2.54, J2.80 i.MX27S: J1.110 OMAPS: J1:110,144,152 / J2:54,96,122	-	-	-	VMMC2 (LDO) / NVCC3	NVCC3	2.8	SW2AOUT (REG) / 1.8V_DDR	NVDD5	1.8	VIO.SW (REG) / VIO_1V8	vdds vdds_mem	1.8
PCC_nDRV_nEN	J2.36	Yes	-	Yes	uP_PC_POE	PC_POE	2.8	uP_PC_POE	PC_POE	1.8	uP_nCS3	GPMC_nCS3	1.8
uP_PCC_CD1	J2.26	Yes	-	Yes	uP_PCC_CD1	PC_CD1_B	2.8	uP_PCC_CD1	PC_CD1_B	1.8	uP_PCC_CD1	GPIO_154	1.8
uP_PCC_CD2	J2.24	Yes	-	Yes	uP_PCC_CD2	PC_CD2_B	2.8	uP_PCC_CD2	PC_CD2_B	1.8	uP_PCC_CD1	GPIO_154	1.8
PCC_RESET	J2.34	Yes	Yes	Yes	uP_PCC_RESET	PC_RST	2.8	uP_PCC_RESET	PC_RST	1.8	uP_PCC_RESET	GPIO_6	1.8
READY	J2.16	Yes	-	-	uP_PCC_RDYA	PC_READY	2.8	uP_PCC_RDYA	PC_READY	1.8	-	-	1.8
nIOIS16	J2.46	Yes	-	-	uP_PCC_nIOIS16	IOIS16	2.8	uP_PCC_nIOIS16	IOIS16	1.8	-	-	1.8
BVD1	J2.22	Yes	-	-	uP_PCC_BVD1	PC_BVD1	2.8	uP_PCC_BVD1	PC_BVD1	1.8	-	-	1.8
BVD2	J2.20	Yes	-	-	uP_PCC_BVD2	PC_BVD	2.8	uP_PCC_BVD2	PC_BVD2	1.8	-	-	1.8
VS1	J2.28	Yes	-	-	uP_PCC_VS1	PC_VS1	2.8	uP_PCC_VS1	PC_VS1	1.8	-	-	1.8
VS2	J2.30	Yes	-	-	uP_PCC_VS2	PC_VS2	2.8	uP_PCC_VS2	PC_VS2	1.8	-	-	1.8
nWAIT	J2.18	Yes	Yes[1]	Yes	uP_PCC_nWAIT	PC_WAIT	2.8	uP_PCC_nWAIT	PC_WAIT_B	1.8	uP_PCC_nWAIT	GPMC_WAIT2	1.8
Reference Voltage Reg / Domain	i.MX31S: J1.110 i.MX27S: J1.110 OMAPS: J1:110,144,152 / J2:54,96,122	-	-	-	SW2AOUT (BUCK) / 1.8V_DDR	NVCC2 NVCC22	1.8	same as above	NVDD4 NVDD2	1.8	same as above	vdds_mem	1.8
nOE	J2.14	Yes	-	Yes	uP_nLBA	LBA	1.8	uP_nLBA	LBA_B	1.8	uP_nOE	GPMC_nOE	1.8
nWE	J2.40	Yes	-	Yes	uP_RnW	RW	1.8	uP_RnW	RW_B	1.8	uP_nWE	GPMC_nWE	1.8
REG	J2.44	Yes	-	-	uP_nEB0	EB0	1.8	uP_nEB0	EB0_B	1.8	-	-	1.8
nIORD	J2.42	Yes	-	-	uP_nEB1	EB1	1.8	uP_nEB1	EB1_B	1.8	-	-	1.8
nIOWD	J2.38	Yes	-	-	uP_nOE	OE	1.8	uP_nOE	OE_B	1.8	-	-	1.8
nCE1	J2.48	Yes	-	Yes	uP_MSDBA1	SDBA1	1.8	uP_MSDBA1	CE1	1.8	uP_nCS3	GPMC_nCS3	1.8
nCE2	J2.50	Yes	-	Yes	uP_MSDBA0	SDBA0	1.8	uP_MSDBA0	CE0	1.8	uP_nCS3	GPMC_nCS3	1.8
A0	J1.55	Yes	Yes	Yes	uP_MA0	A0	1.8	uP_MA0	A0	1.8	uP_LA1	GPMC_D0	1.8
A1	J1.57	Yes	Yes	Yes	uP_MA1	A1	1.8	uP_MA1	A1	1.8	uP_LA2	GPMC_D1	1.8
A2	J1.59	Yes	Yes	Yes	uP_MA2	A2	1.8	uP_MA2	A2	1.8	uP_LA3	GPMC_D2	1.8
A3	J1.61	Yes	Yes	Yes	uP_MA3	A3	1.8	uP_MA3	A3	1.8	uP_LA4	GPMC_D3	1.8
A4	J1.63	Yes	Yes	Yes	uP_MA4	A4	1.8	uP_MA4	A4	1.8	uP_LA5	GPMC_D4	1.8
A5	J1.65	Yes	Yes	Yes	uP_MA5	A5	1.8	uP_MA5	A5	1.8	uP_LA6	GPMC_D5	1.8
A6	J1.67	Yes	Yes	Yes	uP_MA6	A6	1.8	uP_MA6	A6	1.8	uP_LA7	GPMC_D6	1.8
A7	J1.69	Yes	Yes	Yes	uP_MA7	A7	1.8	uP_MA7	A7	1.8	uP_LA8	GPMC_D8	1.8
A8	J1.73	Yes	Yes	Yes	uP_MA8	A8	1.8	uP_MA8	A8	1.8	uP_LA9	GPMC_D8	1.8
A9	J1.75	Yes	Yes	Yes	uP_MA9	A9	1.8	uP_MA9	A9	1.8	uP_LA10	GPMC_D9	1.8
A10	J1.77	Yes	Yes	Yes	uP_MA10	A10	1.8	uP_MA10	A10	1.8	uP_LA11	GPMC_D10	1.8
A11	J1.79	PCMCIA only	PCMCIA only	PCMCIA only	uP_MA11	A11	1.8	uP_MA11	A11	1.8	uP_LA12	GPMC_D11	1.8
A12	J1.81	PCMCIA only	PCMCIA only	PCMCIA only	uP_MA12	A12	1.8	uP_MA12	A12	1.8	uP_LA13	GPMC_D12	1.8
A13	J1.83	PCMCIA only	PCMCIA only	PCMCIA only	uP_A13	A13	1.8	uP_A13	A13	1.8	uP_LA14	GPMC_D13	1.8
A14	J1.85	PCMCIA only	PCMCIA only	PCMCIA only	uP_A14	A14	1.8	uP_A14	A14	1.8	uP_LA15	GPMC_D14	1.8
A15	J1.87	PCMCIA only	PCMCIA only	PCMCIA only	uP_A15	A15	1.8	uP_A15	A15	1.8	uP_LA16	GPMC_D15	1.8
A16	J1.89	PCMCIA only	PCMCIA only	PCMCIA only	uP_A16	A16	1.8	uP_A16	A16	1.8	uP_A1	GPMC_A1	1.8
A17	J1.93	PCMCIA only	PCMCIA only	PCMCIA only	uP_A17	A17	1.8	uP_A17	A17	1.8	uP_A2	GPMC_A2	1.8
A18	J1.95	PCMCIA only	PCMCIA only	PCMCIA only	uP_A18	A18	1.8	uP_A18	A18	1.8	uP_A3	GPMC_A3	1.8
A19	J1.97	PCMCIA only	PCMCIA only	PCMCIA only	uP_A19	A19	1.8	uP_A19	A19	1.8	uP_A4	GPMC_A4	1.8
A20	J1.99	PCMCIA only	PCMCIA only	PCMCIA only	uP_A20	A20	1.8	uP_A20	A20	1.8	uP_A5	GPMC_A5	1.8
A21	J1.101	PCMCIA only	PCMCIA only	PCMCIA only	uP_A21	A21	1.8	uP_A21	A21	1.8	uP_A6	GPMC_A6	1.8
A22	J1.103	PCMCIA only	PCMCIA only	PCMCIA only	uP_A22	A22	1.8	uP_A22	A22	1.8	uP_A7	GPMC_A7	1.8
A23	J1.105	PCMCIA only	PCMCIA only	PCMCIA only	uP_A23	A23	1.8	uP_A23	A23	1.8	uP_A8	GPMC_A8	1.8

Table 6.5: SOM-LV PCMCIA/CompactFlash Card Interface (continued)

CF Signals	SOM-LV J1/J2 Pin	(I/O & Memory) i.MX Only	(Memory Only) i.MX Only	(Memory Only) OMAP35x	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
					SOM-LV Signal	uP Signal	Voltage	SOM-LV Signal	uP Signal	Voltage	SOM-LV Signal	uP Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: J1.110 i.MX27S: J2.96, J2.122 OMAPS: J1:110,144,152 / J2:54,96,122	-	-	-	same as above	NVCC2	1.8	SW2BOUT (REG) / DVDD_1.8V	NVDD4 NVDD2	1.8	-	-	1.8
CF_nOE	J1.118	-	Yes	-	uP_nOE	OE	1.8	uP_nOE	OE_B	1.8	-	-	1.8
CF_nWE	J1.116	-	Yes	-	uP_nEB0	EB0	1.8	uP_nEB0	EB0_B	1.8	-	-	1.8
CF_nCE connects to CE1 and CE2	J1.114	-	Yes	-	SLOW_nCS	CS5	1.8	SLOW_nCS	uP_nCS5 & A23	1.8	-	-	1.8
nCHRDY	J1.120	-	Yes[1 3]	-	nCHRDY	ECB[2]	1.8 [4]	nCHRDY	ECB_B[2]	1.8	-	-	-
Reference Voltage Reg / Domain	i.MX31S: - i.MX27S: J2.96, J2.122 OMAPS: J1:110,144,152 / J2:54,96,122	-	-	-	SW2BOUT (BUCK) / 1.8V_NVCC10	NVCC10	1.8	same as above	NVDD1	1.8	same as above	vdds_mem	1.8
uP_D0	J1.40	Yes	Yes	Yes	uP_D0	D0	1.8	uP_D0	D0	1.8	uP_D0	GPMC_D0	1.8
uP_D1	J1.42	Yes	Yes	Yes	uP_D1	D1	1.8	uP_D1	D1	1.8	uP_D1	GPMC_D1	1.8
uP_D2	J1.44	Yes	Yes	Yes	uP_D2	D2	1.8	uP_D2	D2	1.8	uP_D2	GPMC_D2	1.8
uP_D3	J1.46	Yes	Yes	Yes	uP_D3	D3	1.8	uP_D3	D3	1.8	uP_D3	GPMC_D3	1.8
uP_D4	J1.48	Yes	Yes	Yes	uP_D4	D4	1.8	uP_D4	D4	1.8	uP_D4	GPMC_D4	1.8
uP_D5	J1.50	Yes	Yes	Yes	uP_D5	D5	1.8	uP_D5	D5	1.8	uP_D5	GPMC_D5	1.8
uP_D6	J1.54	Yes	Yes	Yes	uP_D6	D6	1.8	uP_D6	D6	1.8	uP_D6	GPMC_D6	1.8
uP_D7	J1.56	Yes	Yes	Yes	uP_D7	D7	1.8	uP_D7	D7	1.8	uP_D7	GPMC_D7	1.8
uP_D8	J1.58	Yes	Yes	Yes	uP_D8	D8	1.8	uP_D8	D8	1.8	uP_D8	GPMC_D8	1.8
uP_D9	J1.60	Yes	Yes	Yes	uP_D9	D9	1.8	uP_D9	D9	1.8	uP_D9	GPMC_D9	1.8
uP_D10	J1.62	Yes	Yes	Yes	uP_D10	D10	1.8	uP_D10	D10	1.8	uP_D10	GPMC_D10	1.8
uP_D11	J1.64	Yes	Yes	Yes	uP_D11	D11	1.8	uP_D11	D11	1.8	uP_D11	GPMC_D11	1.8
uP_D12	J1.66	Yes	Yes	Yes	uP_D12	D12	1.8	uP_D12	D12	1.8	uP_D12	GPMC_D12	1.8
uP_D13	J1.68	Yes	Yes	Yes	uP_D13	D13	1.8	uP_D13	D13	1.8	uP_D13	GPMC_D13	1.8
uP_D14	J1.70	Yes	Yes	Yes	uP_D14	D14	1.8	uP_D14	D14	1.8	uP_D14	GPMC_D14	1.8
uP_D15	J1.74	Yes	Yes	Yes	uP_D15	D15	1.8	uP_D15	D15	1.8	uP_D15	GPMC_D15	1.8
BUFF_DIR_DATA	J1.123	Yes	Yes	Yes	BUFF_DIR_DATA	-	1.8	BUFF_DIR_DATA	-	1.8	BUFF_DIR_DATA	GPMC_IODIR	1.8
Reference Voltage Reg / Domain		-	-	-	VMMC2 (LDO) / NVCC3	NVCC3	2.8	same as above	NVDD5	1.8	same as above	vdds vdds_mem	1.8
PC_PWRON	J2.213	Optional	Optional	-	PC_PWRON	PC_PWRON	2.8	PC_PWRON	PC_PWRON	1.8	different function[7]	GPIO_174	1.8
Reference Voltage Reg / Domain	i.MX31: J2.122 i.MX27S: J2.96, J2.122 OMAPS: J2.138	-	-	-	VRF1 (REG) / 2.7V_NVCC6/NVCC9	NVCC6	2.7	same as above	NVDD10	1.8	VDDS_SIM (LDO) / VSIM	vdds_sim	1.8
PCC_PCMCIA_nEN	J2.15	Yes	Yes	Yes	PCC_PCMCIA_nEN	MCU2_25	2.7	PCC_PCMCIA_nEN	PC17	1.8	SIM0_VEN	GPIO_128	1.8
Reference Voltage Reg / Domain	i.MX31: J1.183 i.MX27S: J2.96, J2.122 OMAPS: J2.138	-	-	-	VIOLO (Reg) / 1.8V_NVCC7	NVCC7	1.8	same as above	NVDD10	1.8	same as above	vdds_sim	1.8
PCC_POWER_nEN	J2.13	Yes	Yes	Yes	PCC_POWER_nEN	MCU3_24	1.8	PCC_POWER_nEN	PC16	1.8	SIM0_VEN	GPIO_128	1.8
PCC_POWER_nEN	J2.152	Yes	Yes	Yes	PCC_POWER_nEN	MCU3_24	1.8	PCC_POWER_nEN	PC16	1.8	different function[5]	-	1.8 [6]

Note(s):

1. Either use nCHRDY or nWAIT signal to extend bus cycle to memory mode CompactFlash cards.
2. The on board mosfets allows for compact flash cards that have push/pull outputs on the nCHRDY pins to maintain open drain assertion of the nWAIT signal.
3. The baseboard should provide a pull-up on hte nCHRDY to the voltage of the CF Card being used.
4. While the signal into the i.MX31 is on the 1.8V_NVCC10, the nCHRDY signal is pulled up to 3.3V on the module.
5. OMAP35x/PCC_POWER_nEN - Signal function is uP_GPIO_2
6. OMAP35x/PCC_POWER_nEN - Power reference is VIO_1V8
7. OMAP35x (J2.213) - Signal function is either GPIO_174 or MCSPI1_SIMO

6.3.2 MMC/SD Card Interface

All three SOM-LVs support 1- or 4-bit transfer modes for MMC, SD, and SDIO cards on each of the available MMC/SD/SDIO interfaces. In addition, the OMAP35x SOM-LV supports 8-bit transfer modes for MMC cards on each of the available MMC/SD/SDIO interfaces.

The i.MX SOM-LV modules each have two MMC/SD card controllers, while the OMAP35x SOM-LV module has three MMC/SD card controllers. Each controller only has one interface; this means the i.MX SOM-LVs only have the primary and secondary interfaces available, while the OMAP35x SOM-LV has all three interfaces available.

Voltages shown in the tables below indicate the capabilities of each SOM-LV. Please refer to the specific *MMC/SD-Memory Card Specification* for target interface voltages required within your specific design.

The OMAP35x host controller supports the following specifications:

- Full compliance with MMC command/response sets as defined in the *Multimedia Card System Specification v4.2*, including high-capacity (size greater than 2 GB) cards HC MMC.
- Full compliance with SD command/response sets as defined in the *SD Memory Card Specification v2.0*, including high-capacity (size greater than 2 GB) cards HC MMC.
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the *SDIO Simplified Specification v1.10.*
- Compliance with sets as defined in the *SD Host Controller Simplified Specification v1.00*
- Full compliance with MMC bus testing procedure as defined in the *Multimedia Card System Specification v4.2*
- Full compliance with CE-ATA command/response sets as defined in the *CE-ATA Standard Specification*
- Full compliance with *ATA on MMC Specification*

The i.MX31 and i.MX27 host controllers supports the following specifications:

- Full compatibility with the *Multimedia Card System Specification v3.2*
- Compatibility with the *SD Memory Card Specification v1.01* and *SDIO Simplified Specification v1.10* with ¼ channel(s)

6.3.2.1 Primary MMC/SD Card Interface

The primary MMC/SD card interface for the i.MX31, i.MX27, and OMAP35x SOM-LVs is on the following pins: J2.82, J2.84, J2.86, J2.88, J2.90, and J2.94. On the i.MX31 SOM-LV, these pins are routed to the SD1 port; on the i.MX27 SOM-LV, these pins are routed to the SD2 port; on the OMAP35x SOM-LV these pins are routed to MMC/SD/SDIO1 host controller interface.

The OMAP35x SOM-LV has an additional four signals available for supporting 8-bit MMC cards, which are on the following pins: J2.132, J2.128, J2.124, and J2.136. See Table 6.6 below for details.

Table 6.6: SOM-LV Primary MMC/SD Card Interface

MMC/SD Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		uP Signal	Voltage	uP Signal	Voltage	uP Signal	Voltage
Reference Voltage Reg / Domain	J2.80	VMMC2 (LDO) / NVCC3	2.8 (Variable[1])	VMMC2 (LDO) / VMMC2	1.8 (Variable[2])	MMC1.OUT (LDO) / VMMC1	3.0 (Variable[3])
MMC/SD_CLK	J2.94	SD1_CLK	2.8 (Variable[1])	SD2_CLK	1.8 (Variable[2])	MMC1_CLK	3.0 (Variable[3])
MMC/SD_CMD	J2.90	SD1_CMD	2.8 (Variable[1])	SD2_CMD	1.8 (Variable[2])	MMC1_CMD	3.0 (Variable[3])
MMC/SD_DATA0	J2.88	SD1_DATA0	2.8 (Variable[1])	SD2_DATA0	1.8 (Variable[2])	MMC1_DAT0	3.0 (Variable[3])
MMC/SD_DATA1	J2.86	SD1_DATA1	2.8 (Variable[1])	SD2_DATA1	1.8 (Variable[2])	MMC1_DAT1	3.0 (Variable[3])
MMC/SD_DATA2	J2.84	SD1_DATA2	2.8 (Variable[1])	SD2_DATA2	1.8 (Variable[2])	MMC1_DAT2	3.0 (Variable[3])
MMC/SD_DATA3	J2.82	SD1_DATA3	2.8 (Variable[1])	SD2_DATA3	1.8 (Variable[2])	MMC1_DAT3	3.0 (Variable[3])
Reference Voltage Reg / Domain	J2.138					VSIM.OUT (LDO) / VSIM	1.8
MMC_DATA4	J2.132	-	-	-	-	MMC1_DAT4	1.8
MMC_DATA5	J2.128	-	-	-	-	MMC1_DAT5	1.8
MMC_DATA6	J2.124	-	-	-	-	MMC1_DAT6	1.8
MMC_DATA7	J2.136	-	-	-	-	MMC1_DAT7	1.8

Note(s):
1. VMMC2 LDO on the i.MX31 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8/2.9/3.0) and meet NVCC3 specification. Not all voltages may meet the physical layer specifications of the card interface. NVCC3 is the reference voltage for various other IO signal. Special care must be taken if the VMMC2 LDO voltage is changed.
2. VMMC2 LDO on the i.MX27 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8) and meet NVCC15 specification. Not all voltages may meet the physical layer specifications of the card interface.
3. MMC1.OUT LDO on the OMAP35x SOM-LV can be programmed to any of the following voltages (1.85: 1.8V mode) and (2.85, 3.00, 3.15: 3V mode) and meet vdds_mmc1 specification.

6.3.2.2 Secondary MMC/SD Card Interface

A secondary MMC/SD card interface is routed to the baseboard on all three SOM-LV modules; however, the ports are on different pins because of pin-muxing on the i.MX31, i.MX27, and OMAP35x processors. Table 6.7 below describes how the second SD card interface is routed off each respective SOM-LV module.

Note: This secondary port is SD2 on the i.MX31 SOM-LV, SD1 on the i.MX27 SOM-LV, and the MMC/SD/SDIO2 host controller interface on the OMAP35x SOM-LV.

Table 6.7: SOM-LV Secondary MMC/SD Card Interface

MMC/SD Signal	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
	uP Signal	J1/J2 Pin	Voltage	uP Signal	J1/J2 Pin	Voltage	uP Signal	J1/J2 Pin	Voltage
Reference Voltage Reg / Domain	VMMC2 (LDO) / NVCC3	J2.80	2.8 (Variable[1])	VMMC1(LDO) / VMMC1	J2.138	1.8 (Variable[2])	VIO.SW (REG) / VIO_1V8 [3]	J1:110,144,152 / J2:54,96,122	1.8
MMC/SD_CLK	SD2_CLK	J2.24	2.8 (Variable[1])	SD1_CLK	J2.136	1.8 (Variable[2])	MMC2_CLK	J1.228	1.8
MMC/SD_CMD	SD2_CMD	J2.26	2.8 (Variable[1])	SD1_CMD	J2.134	1.8 (Variable[2])	MMC2_CMD	J1.226	1.8
MMC/SD_DATA0	SD2_D0	J2.18	2.8 (Variable[1])	SD1_DATA0	J2.132	1.8 (Variable[2])	MMC2_DAT0	J1.224	1.8
MMC/SD_DATA1	SD2_D1	J2.16	2.8 (Variable[1])	SD1_DATA1	J2.128	1.8 (Variable[2])	MMC2_DAT1	J1.218	1.8
MMC/SD_DATA2	SD2_D2	J2.28	2.8 (Variable[1])	SD1_DATA2	J2.126	1.8 (Variable[2])	MMC2_DAT2	J1.220	1.8
MMC/SD_DATA3	SD2_D3	J2.213	2.8 (Variable[1])	SD1_DATA3	J2.124	1.8 (Variable[2])	MMC2_DAT3	J1.222	1.8
MMC_DATA4	-	-	-	-	-	-	MMC2_DAT4	J2.203	1.8
MMC_DATA5	-	-	-	-	-	-	MMC2_DAT5	J2.201	1.8
MMC_DATA6	-	-	-	-	-	-	MMC2_DAT6	J2.199	1.8
MMC_DATA7	-	-	-	-	-	-	MMC2_DAT7	J2.197	1.8
Additional Signal Options									
MMC_DATA4	-	-	-	-	-	-	MMC2_DATA4	J2.211	1.8
MMC_DATA5	-	-	-	-	-	-	MMC2_DATA5	J2.213	1.8
MMC_DATA6	-	-	-	-	-	-	MMC2_DATA6	J2.191	1.8
MMC_DATA7	-	-	-	-	-	-	MMC2_DATA7	J2.215	1.8
MMC_DIR_DAT0	-	-	-	-	-	-	MMC2_DIR_DAT0 [5, 6]	J2.203	1.8
MMC_DIR_DAT1	-	-	-	-	-	-	MMC2_DIR_DAT1 [5, 7]	J2.201	1.8
MMC_DIR_DAT2	-	-	-	-	-	-	MMC2_DIR_DAT2 [8]	J2.34	1.8
MMC_DIR_DAT3	-	-	-	-	-	-	MMC2_DIR_DAT3 [9]	J1.156	1.8
MMC_DIR_CMD	-	-	-	-	-	-	MMC2_DIR_CMD [5]	J2.199	1.8

Note(s):

1. VMMC2 LDO on the i.MX31 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8/2.9/3.0) and meet NVCC3 specification. Not all voltages may meet the physical layer specifications of the card interface. NVCC3 is the reference voltage for various other IO signal. Special care must be taken if the VMMC2 LDO voltage is changed.
2. VMMC1 LDO on the i.MX27 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8/2.9/3.0) and meet the NVDD8 specification. NVDD8 is the reference voltage for various other IO signal. Special care must be taken if the VMMC1 LDO voltage is changed.
3. VMMC2 on J1.231 is not the reference voltage for MMC2. VMMC2 is an extra LDO output from TPS65950 available to the user.
4. The MMC/SD/SDIO2 host controller interface can support 3V with signals from a 4-bit external transceiver using the MMC_DIR_CMD and MMC_DIR_DAT signals.
5. Signals are shared with the 802.11 wireless interface. The 802.11 wireless chipset must be removed to use the MMC2 SDIO/MMC transceiver control signals.
6. MMC2_DIR_DAT0 is the direction control for mmc2_dat0 signal when an external transceiver is used (high when transmit and low when receive).
7. MMC2_DIR_DAT1 is the direction control for mmc2_dat1 and mmc2_dat3 signal when an external transceiver is used (high when transmit and low when receive).
8. MMC2_DIR_DAT2 is the direction control for mmc2_dat2 signal when an external transceiver is used (high when transmit and low when receive).
9. MMC2_DIR_DAT3 is the direction control for mmc2_dat[7:4] signal when an external transceiver is used (high when transmit and low when receive).

6.3.2.3 Third MMC/SD Card Interface

The third MMC/SD card interface is only routed to the baseboard on the OMAP35x SOM-LV. The MMC3 signals are muxed with high-speed USB signals used on the ETM adapter board (connects at reference designator J5). The ETM adapter board must remain unconnected when using the third MMC/SD card interface on the OMAP35x SOM-LV. See Table 6.8 below for details.

Table 6.8: SOM-LV Third MMC/SD Card Interface

MMC/SD Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		uP Signal	Voltage	uP Signal	Voltage	uP Signal	Voltage
Reference Voltage	J1:110,144,152/J2:54,96,122	-	-	-	-	VIO.SW (REG) / VIO_1V8	1.8
MMC/SD_CLK	J2.207	-	-	-	-	MMC3_CLK[1]	1.8
MMC/SD_CMD	J2.205	-	-	-	-	MMC3_CMD[1]	1.8
MMC/SD_DATA0	J2.203	-	-	-	-	MMC3_DAT0[1]	1.8
MMC/SD_DATA1	J2.201	-	-	-	-	MMC3_DAT1[1]	1.8
MMC/SD_DATA2	J2.199	-	-	-	-	MMC3_DAT2[1]	1.8
MMC/SD_DATA3	J2.197	-	-	-	-	MMC3_DAT3[1]	1.8
MMC_DATA4	J2.41	-	-	-	-	MMC3_DAT4	1.8
MMC_DATA5	J2.35	-	-	-	-	MMC3_DAT5	1.8
MMC_DATA6	J2.39	-	-	-	-	MMC3_DAT6	1.8
MMC_DATA7	J2.25	-	-	-	-	MMC3_DAT7	1.8
Additional Signal Options							
MMC/SD_CLK	J2.37	-	-	-	-	MMC3_CLK	1.8
MMC/SD_CMD	J2.33	-	-	-	-	MMC3_CMD	1.8
MMC/SD_DATA0	J2.23	-	-	-	-	MMC3_DAT0	1.8
MMC/SD_DATA1	J2.21	-	-	-	-	MMC3_DAT1	1.8
MMC/SD_DATA2	J2.19	-	-	-	-	MMC3_DAT2	1.8
MMC/SD_DATA3	J2.17	-	-	-	-	MMC3_DAT3	1.8

Note(s):
1. MMC3 is shared with the 802.11 wireless interface. The 802.11 wireless chipset must be removed to use the MMC3 SDIO/MMC interface.

6.3.3 SIM Card Interface

The i.MX31 SOM-LV offers a SIM card interface to the module connector. The i.MX27 and OMAP35x SOM-LVs do not have a SIM card interface.

The i.MX31 SOM-LV SIM interface is muxed with the second SD card interface. See the SD Card section for more details on the muxing options. See Table 6.9 below for voltage details.

Table 6.9: SOM-LV SIM Card Interface

SIM Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		i.MX31 signal	Voltage	i.MX27 signal	Voltage	OMAP35x signal	Voltage
Reference Voltage Reg / Domain	J2.138	VRF1 (REG) / 2.7V_NVCC6/NVCC9	2.7	-	-	-	-
SIM0_CLK	J2.128	SCLK0	2.7	-	-	-	-
SIM0_IO/TX	J2.132	STX0	2.7	-	-	-	-
SIM0_RX	J2.134	SRX0	2.7	-	-	-	-
SIM0_VEN	J2.124	SVEN0	2.7	-	-	-	-
SIM0_nRESET	J2.136	SRST0	2.7	-	-	-	-
SIM0_nDETECT	J2.126	SIMPD0	2.7	-	-	-	-

6.4 Communication and Control Interfaces

6.4.1 1-Wire

The 1-wire signal is available on J1.221 for all three SOM-LVs; however, the muxing in each processor is different. On the i.MX31 SOM-LV, this signal is routed to the BATT_LINE/MCU2_17

pin on the i.MX31 processor; on the i.MX27 SOM-LV, this signal is routed to the RTCK/OWIRE pin on the i.MX27 processor; and on the OMAP35x SOM-LV, this signal is routed to the HDQ_SIO/SYS_ALTCLK/I2C2_SCCBE/I2C3_SCCBE/GPIO_170 pin on the processor.

6.4.2 UART Interfaces

The i.MX31, i.MX27, and OMAP35x SOM-LVs all have three UARTs with hardware flow control. On both i.MX SOM-LVs, UARTA is mapped to UART1, UARTB is mapped to UART2, and UARTC is mapped to UART3. On the OMAP35x SOM-LV UARTA is mapped to UART1, but UARTB is mapped to UART3, and UARTC is mapped to UART2.

The UARTs are powered differently on the SOM-LV modules. On the i.MX31 SOM-LV, all UART interfaces are approximately 2.8V. On the i.MX27 and OMAP35x SOM-LVs, UART interfaces are 1.8V.

All UARTs on both i.MX SOM-LVs are IrDA-compatible (up to 115.2 kbit/s). The OMAP35x SOM-LV can be configured to support IrDA 1.4 SIR (up to 115.2 kbit/s), MIR (up to 1,152 kbit/s), FIR (up to 4,000 kbit/s), or CIR. See Table 6.10 below for details.

Table 6.10: SOM-LV UARTA, UARTB, and UARTC Interfaces

UART Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		i.MX31 signal	Voltage	i.MX27 signal	Voltage	OMAP35x signal	Voltage
Reference Voltage Reg / Domain	J1.152	VRF1 (REG) / 2.7V_NVCC5/NVCC8	2.7	SW2BOUT (REG) / DVDD_1.8V	1.8	VIO.SW (REG) / VIO_1V8	1.8
Primary UART							
uP_UARTA_RX	J1.158	RXD1	2.7	RXD1	1.8	UART1_RX	1.8
uP_UARTA_TX	J1.160	TXD1	2.7	TXD1	1.8	UART1_TX	1.8
uP_UARTA_RTS	J1.164	CTS1[2]	2.7	CTS1[2]	1.8	UART1_RTS	1.8
uP_UARTA_CTS	J1.162	RTS1[2]	2.7	RTS1[2]	1.8	UART1_CTS	1.8
uP_UARTA_DTR	J1.156	DTR_DTE1	2.7	PC19	1.8	GPIO_7	1.8
uP_UARTA_DSR	J1.154	DSR_DTE1	2.7	PC18	1.8	GPIO_159	1.8
Secondary UART							
uP_UARTB_RX	J1.132	RXD2	2.7	RXD2	1.8	UART3_RX_IRRX	1.8
uP_UARTB_TX	J1.134	TXD2	2.7	TXD2	1.8	UART3_TX_IRTX	1.8
uP_UARTB_RTS	J1.138	CTS2[2]	2.7	CTS2[2]	1.8	UART3_RTS_SD	1.8
uP_UARTB_CTS	J1.136	RTS2[2]	2.7	RTS2[2]	1.8	UART3_CTS_RCTX	1.8
Reference Voltage Reg / Domain	OMAPS: J1.152 i.MX27S: J1.152 i.MX31S: J2.80	VMMC2 (LDO) / NVCC3	2.8 (Variable[1])	same as above	1.8	same as above	1.8
Third UART							
uP_UARTC_RX	J1.126	RXD3	2.8	RXD3	1.8	UART2_RX	1.8
uP_UARTC_TX	J1.128	TXD3	2.8	TXD3	1.8	UART2_TX	1.8
uP_UARTC_RTS	J1.124	CTS3[2]	2.8	CTS3[2]	1.8	UART2_RTS	1.8
uP_UARTC_CTS	J1.122	RTS3[2]	2.8	RTS3[2]	1.8	UART2_CTS	1.8

Note(s):
1. VMMC2 LDO on the i.MX31 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8/2.9/3.0) and meet NVCC3 specification. Not all voltages may meet the physical layer specifications of the card interface. NVCC3 is the reference voltage for various other IO signal. Special care must be taken if the VMMC2 LDO voltage is changed.
2. CTS and RTS signals were swapped due to the fact that the i.MX processors assume DCE functionality while Logic treats all UART signals as if the SOM-LV will be in a device acting in DTE transfer mode.

6.4.3 I2S/AC97/PCM

All three SOM-LVs route the primary I2S port to the same pins on the J2 connector. The i.MX31 has four SSI ports, but only one (port 4) is pinned out to the module connector (ports 3 and 6 are not available to the module connector due to other required functionality for those signals; port 5 connects to I2S interface port 2 of the Atlas component). The i.MX31 SSI port 4 and i.MX27 SSI port 1 both connect directly to the Atlas component and are pinned out to the SOM-LV J2 connector. On the OMAP35x, the I2S port connects to the TPS65950 power management component with integrated audio codec and is pinned out to the SOM-LV J2 connector.

Both i.MX SOM-LV SSI ports support I2S and AC97 interface protocols, while the OMAP35x SOM-LV supports I2S and PCM interface protocols.

The SOM-LV modules offer alternative connections to external codec devices; however, some of the ports are hidden behind other functions. Details are shown in Table 6.11 below. Contact Logic for assistance in selecting an appropriate audio codec for your application.

Table 6.11: SOM-LV I2S/AC97/PCM Interface

Audio Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV							i.MX27 SOM-LV						OMAP35x SOM-LV [1]					
		SOM-LV Signal	i.MX31 Signal	AC97	I2S	PCM	Voltage	SOM-LV Signal	i.MX27 signal	AC97	I2S	PCM	Voltage	SOM-LV Signal	OMAP35x signal	AC97	I2S	PCM	Voltage
Reference Voltage Reg / Domain	i.MX31S: J1.152, J2.96 i.MX27S J1.183, J2.96, J2.122 OMAPS: J1.110, J1.144	-	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	-	-	2.7	-	SW2BOUT (REG) / DVDD_1.8V	-	-	-	1.8	-	VIO.SW (REG) / VIO_1V8	-	-	-	1.8
Primary Audio Interface																			
TX	J2.227	uP_SRXD4 [3]	STXD4	Y	Y	-	2.7	uP_STXD1 [3]	SSI1_RXDAT	Y	Y	-	1.8	MCBSP2_DX [3]	McBSP2_DX	-	Y	Y	1.8
RX	J2.225	uP_STXD4 [3]	SRXD4	Y	Y	-	2.7	uP_STRX1 [3]	SSI1_TXDAT	Y	Y	-	1.8	MCBSP2_DR [3]	McBSP2_DR	-	Y	Y	1.8
FRAME	J2.223	uP_SFS [3]	SFS4	Y	Y	-	2.7	uP_SFS1 [3]	SSI1_FS	Y	Y	-	1.8	MCBSP2_FSX [3]	McBSP2_FSX	-	Y	Y	1.8
CLK	J2.221	uP_SCK [3]	SCK4	Y	Y	-	2.7	uP_SCK1 [3]	SSI1_CLK	Y	Y	-	1.8	MCBSP2_CLKX [3]	McBSP2_CLKX	-	Y	Y	1.8
i.MX27 Synchronous Serial Interface 2																			
SSI2_CLK	J1.163	-	-	Y	Y	-	-	LCD_BACKLIGHT_PWR	SSI2_CLK	Y	Y	-	1.8	-	-	-	-	-	-
SSI2_TXDAT	J1.216	-	-	Y	Y	-	-	uP_GPIO_1 [2]	SSI2_TXDAT	Y	Y	-	1.8	-	-	-	-	-	-
SSI2_RXDAT	J1.218	-	-	Y	Y	-	-	uP_GPIO_0 [2]	SSI2_RXDAT	Y	Y	-	1.8	-	-	-	-	-	-
SSI2_FS	J1.142	-	-	Y	Y	-	-	uP_GPIO_3	SSI2_FS	Y	Y	-	1.8	-	-	-	-	-	-
i.MX27 Synchronous Serial Interface 4																			
SSI4_CLK	J1.156	-	-	Y	Y	-	-	uP_UARTA_DTR	SSI4_CLK	Y	Y	-	1.8	-	-	-	-	-	-
SSI4_TXDAT	J1.154	-	-	Y	Y	-	-	uP_UART_DSR	SSI4_TXDAT	Y	Y	-	1.8	-	-	-	-	-	-
SSI4_RXDAT	J2.15	-	-	Y	Y	-	-	PCC_PCMCIA_nEN	SSI4_RXDAT	Y	Y	-	1.8	-	-	-	-	-	-
SSI4_FS	J2.13	-	-	Y	Y	-	-	PCC_POWER_nEN	SSI4_FS	Y	Y	-	1.8	-	-	-	-	-	-
OMAP35x Multi-Channal Buffered Serial Port 1																			
MCBSP1_CLKR	J1.158	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTA_RX	MCBSP1_CLKR	-	Y	Y	1.8
MCBSP1_CLKR	J2.126	-	-	-	-	-	-	-	-	-	-	-	-	SiM0_nDETECT	MCBSP1_CLKR	-	Y	Y	1.8
MCBSP1_CLKX	J1.15	-	-	-	-	-	-	-	-	-	-	-	-	nSUSPEND	MCBSP1_CLKX	-	Y	Y	1.8
MCBSP1_FSR	J2.232	-	-	-	-	-	-	-	-	-	-	-	-	BT_IRQ	MCBSP1_FSR	-	Y	Y	1.8
MCBSP1_FSX	J1.17	-	-	-	-	-	-	-	-	-	-	-	-	nSTANDBY	MCBSP1_FSX	-	Y	Y	1.8
MCBSP_DR	J1.154	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTA_DSR	McBSP1_DR	-	Y	Y	1.8
MCBSP_DX	J1.23	-	-	-	-	-	-	-	-	-	-	-	-	USB1_nOC	McBSP1_DX	-	Y	Y	1.8
OMAP35x Multi-Channal Buffered Serial Port 3																			
MCBSP3_DX	J1.122	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTC_CTS	MCBSP3_DX	-	Y	Y	1.8
MCBSP3_DX	J2.158	-	-	-	-	-	-	-	-	-	-	-	-	PCM_DR	MCBSP3_DX	-	Y	Y	1.8
MCBSP3_DX	J1.23	-	-	-	-	-	-	-	-	-	-	-	-	USB1_nOC	MCBSP3_DX	-	Y	Y	1.8
MCBSP3_DR	J1.124	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTC_RTS	MCBSP3_DR	-	Y	Y	1.8
MCBSP3_DR	J1.162	-	-	-	-	-	-	-	-	-	-	-	-	PCM_DX	MCBSP3_DR	-	Y	Y	1.8
MCBSP3_DR	J1.154	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTA_DSR	MCBSP3_DR	-	Y	Y	1.8
MCBSP3_FSX	J1.126	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTC_RX	MCBSP3_FSX	-	Y	Y	1.8
MCBSP3_FSX	J2.160	-	-	-	-	-	-	-	-	-	-	-	-	BT_PCM_VFS	MCBSP3_FSX	-	Y	Y	1.8
MCBSP3_CLKX	J1.166	-	-	-	-	-	-	-	-	-	-	-	-	uP_UARTC_TX	MCBSP3_CLKX	-	Y	Y	1.8
MCBSP3_CLKX	J1.128	-	-	-	-	-	-	-	-	-	-	-	-	BT_PCM_CLK	MCBSP3_CLKX	-	Y	Y	1.8
MCBSP3_CLKX	J1.15	-	-	-	-	-	-	-	-	-	-	-	-	nSUSPEND	MCBSP3_CLKX	-	Y	Y	1.8
OMAP35x Multi-Channal Buffered Serial Port 4																			
MCBSP4_CLKX	J1.147	-	-	-	-	-	-	-	-	-	-	-	-	uP_nCS_A_EXT	MCBSP4_CLKX	-	Y	Y	1.8
MCBSP4_FSX	J1.161	-	-	-	-	-	-	-	-	-	-	-	-	LCD_PANEL_PWR	MCBSP4_FSX	-	Y	Y	1.8
MCBSP4_DR	J1.145	-	-	-	-	-	-	-	-	-	-	-	-	uP_nCS_B_EXT	MCBSP4_DR	-	Y	Y	1.8
MCBSP4_DR	J1.232	-	-	-	-	-	-	-	-	-	-	-	-	TOUCH_nIRQ	MCBSP4_DR	-	Y	Y	1.8
MCBSP4_DX	J2.24, J2.26	-	-	-	-	-	-	-	-	-	-	-	-	uP_PCC_CD1	MCBSP4_DX	-	Y	Y	1.8
MCBSP4_DX	J1.133	-	-	-	-	-	-	-	-	-	-	-	-	uP_DREQ0	MCBSP4_DX	-	Y	Y	1.8
OMAP35x Multi-Channal Buffered Serial Port 5																			
MCBSP5_CLKX	J2.37	-	-	-	-	-	-	-	-	-	-	-	-	HSUSB1_STP	MCBSP5_CLKX	-	Y	Y	1.8
MCBSP5_FSX	J1.161	-	-	-	-	-	-	-	-	-	-	-	-	HSUSB1_D5	MCBSP5_FSX	-	Y	Y	1.8
MCBSP5_DR	J2.23	-	-	-	-	-	-	-	-	-	-	-	-	HSUSB1_D4	MCBSP5_DR	-	Y	Y	1.8
MCBSP5_DX	J2.19	-	-	-	-	-	-	-	-	-	-	-	-	HSUSB1_D6	MCBSP5_DX	-	Y	Y	1.8

Note(s):

1. Recommended usage from TI for the McBSP modules on the OMAP35x SOM-LV are as follows: McBSP1: Digital Baseband data; McBSP2: Audio Data with buffer; McBSP3: Bluethooth Voice Data; McBSP4: Digital baseband Voice Data; and McBSP5: Midi Data (Audio).
2. uP_GPIO_0 and uP_GPIO_1 signals are used by LogicLoader as STATUS0 and STATUS1 LED signals respectively.
3. This I2S link serial interface is a connection between the processor and the CODEC on the SOM-LV module. The I2S interface is a TDM slot-based serial interface that is dedicated to transferring serial data.

6.4.4 SPI Interfaces

Each SOM-LV has available primary and secondary SPI interfaces. The primary SPI interface for each SOM-LV is available on the same pins of the J1 and J2 connectors. The secondary SPI interface is hidden behind other functionality and is found on different pins of the J1 and J2 connectors for each SOM-LV. The tables available in the sub-sections below show a comparison of the SOM-LV signals, SOC signals, voltages, and primary function.

Some signals may be listed in the primary interface table but are noted as an alternate signal. This only occurs if there is an alternate signal that was not intended as the primary signal for that interface, but can be used in place of the primary target signal.

Both the i.MX31 and i.MX27 SOM-LV have components that must co-exist on some of the SPI ports. Both SOM-LVs use an SPI port to talk to the Atlas chip: the i.MX31 SOM-LV uses CSPI2, SS0 and the i.MX27 SOM-LV uses CSPI1, SS0. The i.MX31 SOM-LV interfaces to an EEPROM using CSP1, CS2.

6.4.4.1 Primary SPI Interface

On the primary SPI interface, each SOM-LV routes SPI1 to the baseboard through the same pins on the J1 and J2 connectors using a 1.8V interface. The i.MX31 and OMAP35x SOM-LV each route two chip selects (CS0 and CS1) to the baseboard, whereas the i.MX27 SOM-LV only routes one chip select (SS1) to the baseboard. See Table 6.12 below for details.

6.4.4.2 Secondary SPI Interface

All three SOM-LVs allow access to a second SPI interface port, but through different pins on the connectors and hidden behind other functionality. See Table 6.13 below for the pin mapping and details.

Table 6.12: SOM-LV Primary SPI Interface

	i.MX31 SOM-LV					i.MX27 SOM-LV					OMAP35x SOM-LV				
SPI Signal	SOM-LV Signal	i.MX31 Signal	Primary	J1/J2 Pin	Voltage	SOM-LV Signal	i.MX27 signal	Primary	J1/J2 Pin	Voltage	SOM-LV Signal	OMAP35x signal	Primary	J1/J2 pin	Voltage
Reference Voltage Reg / Domain	-	SW2BOUT (BUCK) / 1.8V_NVCC10	-	-	-	-	VMMC1(LDO) / VMMC1	-	J2.138	1.8 (Variable[1])	-	VIO.SW (REG) / VIO_1V8	-	-	1.8
CLK	uP_SPI_SCLK	CSPI1_SCLK	Yes	J1.228	1.8	uP_CSPI1_SCLK	CSPI1_SCLK	Yes	J1.228	1.8 (Variable[1])	uP_SPI_SCLK	McSPI3_CLK	Yes	J1.228	1.8
CS0	uP_SPI_CS0	CSPI1_SS0	Yes	J1.222	1.8	uP_CSPI1_SS0	CSPI1_SS0	Yes	-[2]	-	uP_SPI_CS0	McSPI3_CS0	Yes	J1.222	1.8
CS1	uP_SPI_CS1	CSPI1_SS1	Yes	J1.220	1.8	uP_CSPI1_SS1	CSPI1_SS1	Yes	J1.220	1.8 (Variable[1])	uP_SPI_CS1	McSPI3_CS1	Yes	J1.220	1.8
CS2	uP_SPI_CS2	CSPI1_SS2	Yes	-[3]	1.8	-	-	-	-	-	-	-	-	-	-
TX	uP_SPI_TX	CSPI1_MOSI	Yes	J1.226	1.8	uP_CSPI1_MOSI	CSPI1_MOSI	Yes	J1.226	1.8 (Variable[1])	uP_SPI_SIMO	McSPI3_SIMO	Yes	J1.226	1.8
RX	uP_SPI_RX	CSPI1_MISO	Yes	J1.224	1.8	uP_CSPI1_MISO	CSPI1_MISO	Yes	J1.224	1.8 (Variable[1])	uP_SPI_SOMI	McSPI3_SOMI	Yes	J1.224	1.8
RDY	uP_CSPI1_RDY	CSPI1_SPI_RDY	Yes	J2.83	1.8	uP_CSPI1_RDY	CSPI1_RDY	Yes	J2.83	1.8 (Variable[1])	-	-	-	-	1.8
Reference Voltage Reg / Domain	-	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	J1.152, J2.96	2.7	-	-	-	-	-	-	-	-	-	-
CLK	uP_SW_nRESET	CSPI1_SCLK	Alternate	J2.93	2.7	-	-	-	-	-	-	-	-	-	-
CS3	uP_CSPI2_SS1	CSPI1_SS3	Alternate	J2.89	2.7	-	-	-	-	-	-	-	-	-	-
CS3	uP_nIRQD	CSPI1_SS3	Alternate	J1.113	2.7	-	-	-	-	-	-	-	-	-	-
RDY	uP_GPIO_2	CSPI1_RDY	Alternate	J1.166	2.7	-	-	-	-	-	-	-	-	-	-
RX	uP_UARTA_DSR	CSPI1_MISO	Alternate	J1.154	2.7	-	-	-	-	-	-	-	-	-	-
TX	uP_UARTA_DTR	CSPI1_MOSI	Alternate	J1.156	2.7	-	-	-	-	-	-	-	-	-	-

Note(s):
1. VMMC1 LDO on the i.MX27 SOM-LV can be programmed to any of the following voltages (1.8/2.0/2.6/2.7/2.8/2.9/3.0) and meet the NVDD8 specification. NVDD8 is the reference voltage for various other IO signal. Special care must be taken if the VMMC1 LDO voltage is changed.
2. On the iMX27 SOM-LV CSP1, CS0 is used to access the Atlas (U15) MC13783 LPD#1004401
3. On the iMX31 SOM-LV CSPI1, CS2 is used to access the onboard EEPROM U41-AT93C66A-10TU-1.8 LPD#1005389

Table 6.13: SOM-LV Secondary SPI Interface

	i.MX31 SOM-LV					i.MX27 SOM-LV					OMAP35x SOM-LV				
SPI Signal	SOM-LV Signal	i.MX31 Signal	Primary	J1/J2 Pin	Voltage	SOM-LV Signal	i.MX27 signal	Primary	J1/J2 Pin	Voltage	SOM-LV Signal	OMAP35x signal	Primary	J1/J2 pin	Voltage
Reference Voltage Reg / Domain	-	SW2BOUT (BUCK) / 1.8V_NVCC10	-	-	-	-	VMMC1(LDO) / VMMC1	-	J2.138	-	-	VIO.SW (REG) / VIO_1V8	-	-	1.8
SCLK	uP_UARTC_CTS	CSPI3_SCLK	Alternate	J1.122	1.8	SD1_CLK	CSPI3_SCLK	Alternate	J2.136	-	MCSPI1_CLK[1]	McSPI1_CLK	Alternate	J2.211	1.8
Reference Voltage Reg / Domain	-	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	J1.152, J2.96	2.7	-	same as above	-	-	-	-	same as above	-	-	1.8
CS0	-	-	-	-	-	SD1_DATA3	CSPI3_SS	Alternate	J2.124	-	MCSPI1_CS0[1]	McSPI1_CS0	Alternate	J2.215	1.8
CS1	uP_CSPI2_SS1	CSPI3_SS1	Alternate	J2.89	2.7	-	-	-	-	-	WLAN_MMC3_CMD[2]	McSPI1_CS1	Alternate	J2.205	1.8
CS2	-	-	-	-	-	-	-	-	-	-	WLAN_MMC3_CLK[2]	McSPI1_CS2	Alternate	J2.207	1.8
Reference Voltage Reg / Domain	-	VMMC2 (LDO) / NVCC3	-	J2.80	-	-	same as above	-	-	-	-	same as above	-	-	1.8
TX	uP_UARTC_RX	CSPI3_MOSI	Alternate	J1.126	2.8	SD1_CMD	CSPI3_MOSI	Alternate	J2.134	-	MCSPI1_SIMO[1]	McSPI1_SIMO	Alternate	J2.213	1.8
RX	uP_UARTC_TX	CSPI3_MISO	Alternate	J1.128	2.8	SD1_DATA0	CSPI3_MISO	Alternate	J2.132	-	MCSPI1_SOMI[1]	McSPI1_SOMI	Alternate	J2.191	1.8
RDY	uP_UARTC_RTS	CSPI3_SPI_RDY	Alternate	J1.124	2.8	-	-	-	-	-	-	-	-	-	1.8

Note(s):
1. MCSPI1 is shared with the Bluetooth interface. The Bluetooth chipset must be removed to use this signal.
2. MCSP1_CS0 is shared with the 802.11 interface. The 802.11 chipset must be removed to use this signal.

6.4.5 USB Interfaces

Each SOM-LV module supports two independent USB interfaces. One USB interface connects to the On-the-Go (OTG) controller and the other interface is tied to the USB high-speed port of the target SOC. Both ports support transfer rates up to 480 Mbit/sec.

6.4.5.1 USB1

USB1 is tied to the USB OTG port on the i.MX31, i.MX27, and OMAP35x SOM-LVs, but each SOM uses a different transceiver. The i.MX31 SOM-LV uses the NXP ISP1504 transceiver; the i.MX27 SOM-LV uses the SMSC USB3311 transceiver; and the OMAP35x SOM-LV uses the TPS65950 built-in PHY to support the USB1 interface.

6.4.5.2 USB2

USB2 is tied to the USB high-speed host port on the i.MX31, i.MX27, and OMAP35x SOM-LVs, but each SOM uses a different transceiver. The i.MX31 SOM-LV uses the NXP ISP1504 transceiver; the i.MX27 SOM-LV uses the SMSC USB3311 transceiver; and the OMAP35x SOM-LV uses the NXP ISP170x transceiver.

The over-current and power-enable pins for both USB1 and USB2 interfaces are routed differently on each SOM. See Table 6.14 below for details of how the signals are routed on each SOM.

6.4.6 Ethernet

All three SOM-LVs have the option for 10/100Mbps Wired-LAN Ethernet support. In addition to the Wired-LAN, the OMAP35x module supports IEEE 802.11b/g Wireless-LAN Ethernet using the CSR UF1050x-IC-E on-module component.

Even though all three SOM-LVs support Ethernet, there are also supporting component requirements for the baseboard. The off-module signals associated with the Wired- and Wireless-LAN are shown in Table 6.15 below.

The i.MX31 SOM-LV uses the SMSC LAN9117-MT MAC/PHY; the i.MX27 SOM-LV uses the integrated Ethernet MAC in the i.MX27 processor with the LAN8700 PHY; and the OMAP35x SOM-LV uses the SMSC LAN9211-ABZJ MAC/PHY for the Wired-LAN support. Routing requirements on the baseboard are similar for each SOM-LV.

Table 6.14: SOM-LV USB Interface

USB Signal	J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV				OMAP35x SOM-LV				
		SOM-LV Signal	ISP1504	Voltage	SOM-LV Signal	USB3311	SOC	Voltage	SOM-LV Signal	TPS65950	SOC Pin	ISP1702	Voltage
Reference Voltage Reg / Domain	i.MX31S, i.MX27S: J1.180, J1.182, J1.184 OMAPS: -	3.3V_IN / 3.3V_PHY	VCC	3.3	3.3V_IN / 3.3V	VBAT	-	3.3	-	VUSB3V1 (Internal)	-	-	3.1
USB OTG													
USB1_D+	J1.27	USB1_D+	U17.DP	3.3	USB1_D+	U17.DP	-	3.3	USB1_D+	U1B.DP	-	-	3.1 [2]
USB1_D-	J1.29	USB1_D-	U17.DM	3.3	USB1_D-	U17.DM	-	3.3	USB1_D-	U1B.DN	-	-	3.1 [2]
USB1_ID	J1.19	USB1_ID	U17.ID	3.3	USB1_ID	U17.ID	-	3.3	USB1_ID	U1B.ID	-	-	3.1 [2]
Reference Voltage Reg / Domain	i.MX31S, i.MX27S: J1.180, J1.182, J1.184 OMAPS: J1:110,144,152 / J2:54,96,122	same as above	VCC	3.3	same as above	VBAT	-	3.3	VIO.SW (REG) / VIO_1V8	-	-	-	1.8
USB1_nOC	J1.23	USB1_nOC	U17.FAULT	3.3 [2]	USB1_nOC	-	USB_OC_B	3.3	USB1_nOC	-	GPIO_158	-	1.8
USB1_PWR_nEN	J1.25	USB1_PWR_nEN	U17.PSW_N	3.3 [1]	USB1_PWR_nEN	-	PB28	3.3	USB1_PWR_nEN	GPIO.13	-	-	1.8
USB1_VBUS	J1.21	USB1_VBUS	U17.VBUS	5.0	USB1_VBUS	U17.VBUS	-	5.0	USB1_VBUS	U1B.VBUS	-	-	5 [3]
USB HOST													
Reference Voltage Reg / Domain	i.MX31S, i.MX27S: J1.180, J1.182, J1.184 OMAPS: -	same as above	VCC	3.3	same as above	VBAT	-	3.3	VAUX1.OUT (LDO) / VAUX1_3V0	VAUX1.OUT	-	-	3.0
USB2_D+	J1.33	USB2_D+	U16.DP	3.3	USB2_D+	U16.DP	-	3.3	USB2_D+	-	-	DP	3.0
USB2_D-	J1.35	USB2_D-	U16.DM	3.3	USB2_D-	U16.DM	-	3.3	USB2_D-	-	-	DM	3.0
USB2_nOC	J1.37	USB2_nOC	U16.FAULT	3.3 [2]	USB2_nOC	-	USB_OC_B	3.3	USB2_nOC	-	-	FAULT	3.0
USB2_PWR_nEN	J1.39	USB2_PWR_nEN	U16.PSW_N	3.3 [1]	USB2_PWR_nEN	-	USB_PWR	3.3	USB2_PWR_nEN	-	-	PSW_N	3.0 [1]

Note(s):
1. Open Drain, 5V tolerant
2. 5V tolerant
3. 6V maximum if VBUS_CHRG bit is low within the TPS65950

Table 6.15: SOM-LV Ethernet Interface

Ethernet Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		SOM-LV Signal	Voltage	SOM-LV Signal	Voltage	SOM-LV Signal	Voltage
Wired LAN							
VREF_ETHERNET	J1.26	VREF_ETHERNET	3.3	VREF_ETHERNET	3.3	VREF_ETHERNET	3.3
ACT_nLNK_LED/LAN_LED2	J1.22	ACT_nLNK_LED/LAN_LED2	3.3	ACT_nLNK_LED/LAN_LED2	3.3	ACT_nLNK_LED/LAN_LED2	3.3
SPD_LED_n100M_10M/LAN_LED1	J1.24	SPD_LED_n100M_10M/LAN_LED1	3.3	SPD_LED_n100M_10M/LAN_LED1	3.3	SPD_LED_n100M_10M/LAN_LED1	3.3
ETHER_RX-	J1.20	ETHER_RX-	3.3	ETHER_RX-	3.3	ETHER_RX-	3.3
ETHER_RX+	J1.18	ETHER_RX+	3.3	ETHER_RX+	3.3	ETHER_RX+	3.3
ETHER_TX-	J1.16	ETHER_TX-	3.3	ETHER_TX-	3.3	ETHER_TX-	3.3
ETHER_TX+	J1.14	ETHER_TX+	3.3	ETHER_TX+	3.3	ETHER_TX+	3.3
Wireless LAN							
RF_LED0	J2.81	different function [1]		different function [1]		RF_LED0	3.0
RF_LED1	J2.83	different function [2]		different function [2]		RF_LED1	3.0

Note(s):
1. MC13783 CDCOUT signal on the i.MX27 and the i.MX31
2. uP_CSP1_RDY signal on the i.MX27 and the i.MX31

6.4.6.1 Ethernet Resistor Population

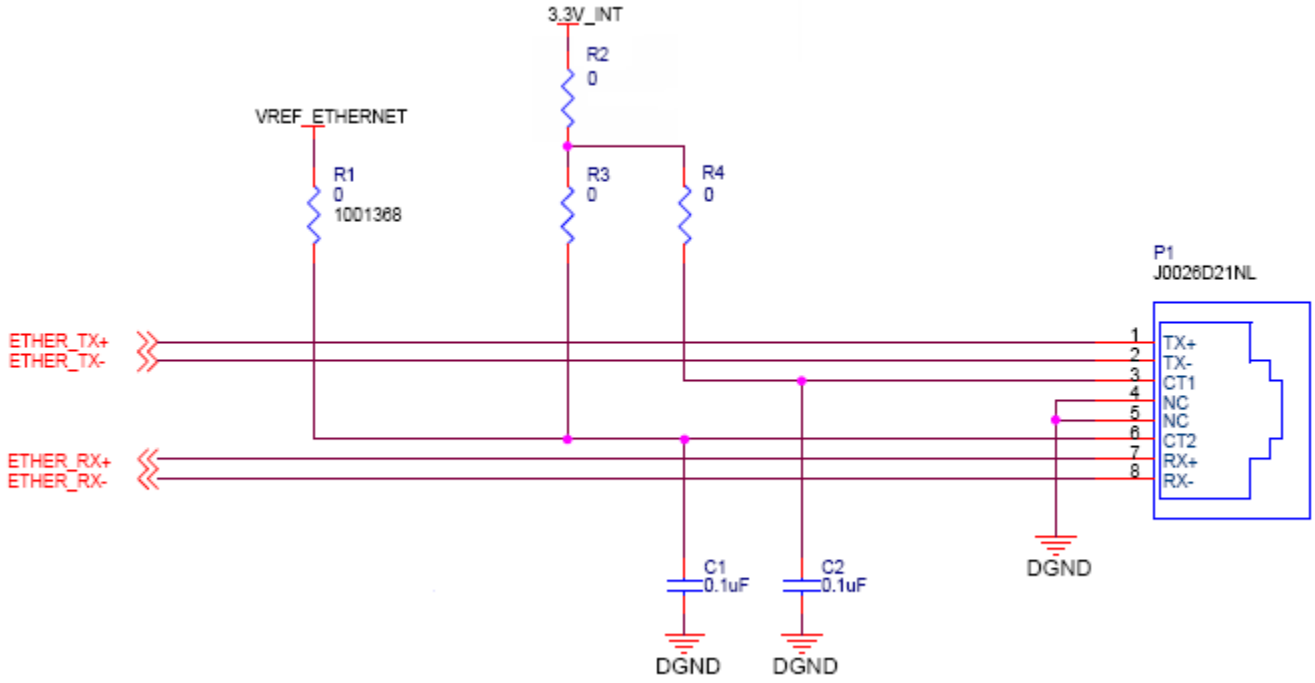
For designs targeting EMI constrained environments, use four 15pF 50V 5% caps in the design to reduce EMI noise. Connect one capacitor for each signal (ETHER_TX+, ETHER_TX-, ETHER_RX+, and ETHER_RX-) to ground.

Table 6.16 and Figure 6.1 below show the baseboard requirements if you design to support 10/100Mbps Ethernet for all three SOM-LVs. Resistors R1, R3, and R4 in Figure 6.1 correspond with the resistors shown in the *SDK2-APP-10 Baseboard Schematics* document.

Table 6.16: Ethernet Resistor Population Requirements

Resistors	i.MX31 SOM-LV	i.MX27 SOM-LV	OMAP35x SOM-LV
R1	Yes	Yes	No
R2	Yes	Yes	10_Ohm 1/8W 1% TOL
R3	No	No	Yes
R4	Yes	Yes	Yes
C1	Yes	Yes	0.022uF 0805
C2	Yes	Yes	No

Figure 6.1: Ethernet Reference Schematic



6.4.7 IRQ Routing

The IRQ signals on the three SOM-LVs are routed to different pins for each processor; see Table 6.17 below for details. Both the i.MX31 and i.MX27 SOM-LVs have on-module pull-ups. The OMAP35x SOM-LV requires software to enable internal pull-ups within the OMAP35x when using these signals for active low interrupts.

Voltage references for each interrupt are routed to different pins on the J1 and J2 module connectors, which are also shown in detail in Table 6.17 below.

6.4.8 Keypad

All three SOM-LVs support keypad functionality. The i.MX31 and OMAP35x SOM-LVs both support a keypad up to a 7x7 matrix; the i.MX27 SOM-LV supports a keypad up to a 4x4 matrix. All available pins are common on the J2 interface. See Table 6.18 below for details.

Table 6.17: SOM-LV IRQ Routing

IRQ Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
		i.MX31 signal	On-Module Pull-up	Voltage	i.MX27 signal	On-Module Pull-up	Voltage	OMAP35x signal	On-Module Pull-up	Voltage
Reference Voltage Reg / Domain	i.MX31S J1.183 i.MX27S J2.96, J2.122, J2.183 OMAPS J1.110, J1.144	VIOLO (Reg) / 1.8V_NVCC1	-	1.8	SW2BOUT (Reg) / DVDD_1.8V	-	1.8	VIO.SW (REG) / VIO_1V8	-	1.8
uP_nIRQA	J1.119	GPIO1_4	Yes, 1.8V_NVCC1	1.8	USBH1_OE_B	Yes, DVDD_1.8V	1.8	CAM_FLD/CAM_GLOBAL_RESET/GPIO_98	no[1]	1.8
uP_nIRQC	J1.115	GPIO1_6	Yes, 1.8V_NVCC1	1.8	USBH1_RCV	Yes, DVDD_1.8V	1.8	CAM_STROBE/GPIO_126	no[1]	1.8
Reference Voltage Reg / Domain	i.MX31S J1.144, J2.173 i.MX27S J2.96, J2.122, J2.183 OMAPS J1.110, J1.144	VCAM (REG) / NVCC4	-	2.8	same as above	-	1.8	same as above	-	1.8
uP_nIRQB	J1.117	GPIO3_0	Yes, 1.8V_NVCC1[3]	1.8	USBH1_FS	Yes, DVDD_1.8V	1.8	CAM_WEN/CAM_SHUTTER/GPIO_167	no[1]	1.8
Reference Voltage Reg / Domain	i.MX31S J1.152, J2.96 i.MX27S J2.96, J2.122, J2.183 OMAPS J1.110, J1.144	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	2.7	same as above	-	1.8	same as above	-	1.8
uP_nIRQD	J1.113	DCD_DCE1	Yes, 2.7V_NVCC5/NVCC8	2.7	USBH1_SUSP	Yes, DVDD_1.8V	1.8	CAM_D11/GPIO_110[2]	no[1]	1.8

Note(s):
1. External IRQs require CPU internal pull-up selection and activation.
2. uP_nIRQD is not available if module is used with a camera sensor requiring CSI_D11 signal.
3. Bug #0003904 has been filed to have this pull-up removed.

Table 6.18: SOM-LV Keypad Interface

Keypad Signal	Same J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
		SOM-LV Signal	uP_Signal	Voltage	SOM-LV Signal	uP_Signal	Voltage	SOM-LV Signal	TPS65950 Signal	Voltage
Reference Voltage Reg / Domain	i.MX31S: J2.122 i.MX27S: J1.152 OMAPS: J1:110,144,152 / J2:54,96,122	VRF1 (REG / 2.7V_NVCC6/NVCC9	-	2.7	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	1.8	VIO.SW (REG) / VIO_1V8	-	1.8
KEY_COL0	J2.107	KEY_COL0	KEY_COL0	2.7	KEY_COL0	KP_COL0	1.8	KEY_COL0	KPD.C0	1.8
KEY_COL1	J2.105	KEY_COL1	KEY_COL1	2.7	KEY_COL1	KP_COL1	1.8	KEY_COL1	KPD.C1	1.8
KEY_COL2	J2.103	KEY_COL2	KEY_COL2	2.7	KEY_COL2	KP_COL2	1.8	KEY_COL2	KPD.C2	1.8
KEY_COL3	J2.101	KEY_COL3	KEY_COL3	2.7	KEY_COL3	KP_COL3	1.8	KEY_COL3	KPD.C3	1.8
KEY_COL4	J2.99	KEY_COL4	KEY_COL4	2.7	different function	-	1.8	KEY_COL4	KPD.C4	1.8
KEY_COL5	J2.97	KEY_COL5	KEY_COL5	2.7	different function	-	1.8	KEY_COL5	KPD.C5	1.8
KEY_COL6	J2.95	KEY_COL6	KEY_COL6	2.7	different function	-	1.8	KEY_COL6	KPD.C6	1.8
KEY_COL7	J2.93	KEY_COL7	KEY_COL7	2.7	different function	-	1.8	KEY_COL7	KPD.C7	1.8
KEY_ROW0	J2.125	KEY_ROW0	KEY_ROW0	2.7	KEY_ROW0	KP_ROW0	1.8	KEY_ROW0	KPD.R0	1.8
KEY_ROW1	J2.123	KEY_ROW1	KEY_ROW1	2.7	KEY_ROW1	KP_ROW1	1.8	KEY_ROW1	KPD.R1	1.8
KEY_ROW2	J2.121	KEY_ROW2	KEY_ROW2	2.7	KEY_ROW2	KP_ROW2	1.8	KEY_ROW2	KPD.R2	1.8
KEY_ROW3	J2.119	KEY_ROW3	KEY_ROW3	2.7	KEY_ROW3	KP_ROW3	1.8	KEY_ROW3	KPD.R3	1.8
KEY_ROW4	J2.117	uP_GPIO_6	KEY_ROW4	2.7	different function	-	1.8	KEY_ROW4	KPD.R4	1.8
KEY_ROW5	J2.115	uP_GPIO_7	KEY_ROW5	2.7	different function	-	1.8	KEY_ROW5	KPD.R5	1.8
KEY_ROW6	J2.113	KEY_ROW6	KEY_ROW6	2.7	different function	-	1.8	KEY_ROW6	KPD.R6	1.8
KEY_ROW7	J2.109	KEY_ROW7	KEY_ROW7	2.7	different function	-	1.8	KEY_ROW7	KPD.R7	1.8

6.4.9 Touch Screen

Each of the three SOM-LVs has a single touch interface input for LCD panels equipped with 4-wire resistive touch screens.

The i.MX31 and i.MX27 SOM-LVs use the MC13783 integrated touch screen controller. The controller includes a 13-bit analog-to-digital converter (ADC), supports standard 4-wire resistive touch panels, and has six A/D signals that are available externally through the J1 and J2 connectors. The device is connected to the CPU by the CSPI interface.

The OMAP35x SOM-LV uses TI's TSC2004 touch screen controller. The controller includes a 12-bit ADC, supports standard 4-wire resistive touch panels, and has five A/D signals that are available externally through the J1 and J2 connectors. The device is connected to the CPU by the OMAP I2C3 interface. Table 6.19 below shows the connection to each SOM-LV.

Table 6.19: SOM-LV Touch Screen Interface

		i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
USB Signal	**J1/J2 Pin**	**SOM-LV Signal**	**MC13783**	**SOM-LV Signal**	**MC13783**	**SOM-LV Signal**	**TSC2004**
TOUCH_TOP	J1.194	TOUCH_TOP	TSY2	TOUCH_TOP	TSY2	TOUCH_TOP	X-
TOUCH_BOTTOM	J1.192	TOUCH_BOTTOM	TSY1	TOUCH_BOTTOM	TSY1	TOUCH_BOTTOM	X+
TOUCH_RIGHT	J1.188	TOUCH_RIGHT	TSX2	TOUCH_RIGHT	TSX1	TOUCH_RIGHT	Y-
TOUCH_LEFT	J1.186	TOUCH_LEFT	TSX1	TOUCH_LEFT	TSX2	TOUCH_LEFT	Y+

6.4.10 CODEC Line-In/Out

The i.MX31 and i.MX27 processors have a Synchronous Serial Interface (SSI) controller that can support AC97 and I2S formats. This SSI controller implements a 5-pin serial interface to the I2S audio codec, in this case the Freescale MC13783. These signals are available through the J1 and J2 connectors.

The OMAP35x processor has several Multi-channel Buffered Serial Port (McBSP) interfaces that support PCM and I2S formats. Both PCM and I2S serial paths drive the TPS65950 with audio codec.

The codec for all three SOM-LVs performs up to full-duplex codec functions and supports variable sample rates from 8–96k samples per second. For all three SOM-LVs, the outputs are CODEC_OUTL and CODEC_OUTR, and are available through the J1 and J2 connectors.

Table 6.20: SOM-LV Audio Interface

Audio Signal	J1/J2 Pin	i.MX31 SOM-LV SOM-LV Signal	i.MX27 SOM-LV SOM-LV Signal	OMAP35x SOM-LV SOM-LV Signal
Line In/Out Interface				
CODEC_OUTL	J2.226	CODEC_OUTL	CODEC_OUTL	CODEC_OUTL
CODEC_OUTR	J2.228	CODEC_OUTR	CODEC_OUTR	CODEC_OUTR
CODEC_INL	J2.222	CODEC_INL	CODEC_INL	CODEC_INL
CODEC_INR	J2.224	CODEC_INR	CODEC_INR	CODEC_INR
Microphone/Headphone				
MIC_IN	J2.212	MIC_IN	MIC_IN	MIC_IN
MIC_INR/MIC_SUB_M	J2.214	MIC_INR	MIC_INR	MIC_SUB_M
MIC_INL/MIC_SUB_P	J2.216	MIC_INL	MIC_INL	MIC_SUB_P
HP_OUTL/MIC_MAIN_M	J2.218	HP_OUTL	HP_OUTL	MIC_MAIN_M
HP_OUTR/MIC_MAIN_P	J2.220	HP_OUTR	HP_OUTR	MIC_MAIN_P
MICBIAS1	J2.219	different function	different function	MICBIAS1
MICBIAS2	J2.217	different function	different function	MICBIAS2
HSLDET	J2.211	HSLDET	HSLDET	different function
Hands-free Speaker Output				
IHF_LEFT_M	J2.206	different function	different function	IHF_LEFT_M
IHF_LEFT_P	J2.208	different function	different function	IHF_LEFT_P
IHF_RIGHT_M	J2.202	different function	different function	IHF_RIGHT_M
IHF_RIGHT_P	J2.204	different function	different function	IHF_RIGHT_P

6.4.11 I2C Interfaces

The i.MX31, i.MX27, and OMAP35x SOM-LVs each have two I2C ports routed to the baseboard. The i.MX31 and i.MX27 have I2C ports 1 and 2 of the SOC processors routed to the baseboard for the primary and secondary I2C interfaces, respectively. The OMAP35x SOM-LV routes I2C port 2 to the primary I2C interface and I2C port 3 to the secondary I2C interface on the module.

Both I2C ports on the i.MX31 SOM-LV are approximately 2.7V. The i.MX27 and OMAP35x SOM-LVs I2C ports are routed to a 1.8V power plane.

The voltage reference for the primary I2C port (VREF_I2C1) is routed to J1.144. The secondary I2C reference voltages (VREF_I2C2) are routed to J2.96. See Table 6.21 below for availability of the primary and secondary I2C interfaces on all three SOM-LVs.

Table 6.21: SOM-LV I2C Interface

I2C Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV			i.MX27 SOM-LV			OMAP35x SOM-LV		
		i.MX31 signal	On-Module Pull-up	Voltage	i.MX27 signal	On-Module Pull-up	Voltage	OMAP35x signal	On-Module Pull-up	Voltage
Primary I2C Port										
Reference Voltage Reg / Domain	J1.144	VCAM (Reg) / NVCC4	-	2.8	SW2BOUT (Reg) / DVDD_1.8V	-	1.8	VIO.SW (REG) / VIO_1V8	-	1.8
I2C1_CLK	J1.148	I2C1_SCL[3]	Yes, 2.2K to NVCC4	2.8	I2C1_CLK	yes, 4.7K DVDD_1.8V	1.8	uP_I2C2_SCL	yes, 4.7K VIO_1V8	1.8
I2C1_DATA	J1.146	I2C1_SDA[3]	Yes, 2.2K to NVCC4	2.8	I2C1_DATA	yes, 4.7K DVDD_1.8V	1.8	uP_I2C2_SDA	yes, 4.7K VIO_1V8	1.8
Secondary I2C Port										
Reference Voltage Reg / Domain	J2.96	VRF1 (REG) / 2.7V_NVCC5/NVCC8	-	2.7	same as above	-	1.8	same as above	-	1.8
I2C2_CLK[1]	J2.98	I2C1_SCL	Yes, 2.2K to 2.7V_NVCC5/NVCC8	2.7 [2]	I2C2_CLK	yes, 4.7K DVDD_1.8V	1.8 [2]	uP_I2C3_SCL[4]	yes, 4.7K VIO_1V8	1.8 [2]
I2C2_DATA[1]	J2.100	I2C1_SCL	Yes, 2.2K to 2.7V_NVCC5/NVCC8	2.7 [2]	I2C2_DATA	yes, 4.7K DVDD_1.8V	1.8 [2]	uP_I2C3_SDA[4]	yes, 4.7K VIO_1V8	1.8 [2]

Note(s):
1. The secondary I2C bus has a Product ID chip connect to the I2C bus on all SOM-LV modules. Some slave addresses will be reserved as a result of the Product ID component. Check the SOM-LV Hardware Specification Manual for the slave addresses that are reserved for the SOM-LV Product ID component.
2. I2C voltage translator on the baseboard may be required when supporting multiply SOM-LV modules on a single baseboard for I2C port 2.
3. On the i.MX31 SOM-LV, I2C1_CLK and I2C1_DATA signals are muxed with ATA module signals (ATA_D14 and ATA D15 respectively).
4. In addition to the Product ID component, the OMAP35x SOM-LV secondary I2C bus is also connected to the TSC2004 touch component. Check the SOM-LV Hardware Specification Manual for the slave addresses that are reserved for the TSC2004 touch component.

6.4.12 ADC Interface

Each SOM-LV has a minimum of four analog-to-digital signals available for use. The OMAP35x SOM-LV has an additional four signals available. See Table 6.22 below for details of the available analog-to-digital signals.

Table 6.22: SOM-LV ADC Interface

ADC Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		SOM-LV Signal	Voltage	SOM-LV Signal	Voltage	SOM-LV Signal	Voltage
A/D4	J1.196	A/D4	max 2.7	A/D4	max 2.7	A/D4	max 2.7
A/D3	J1.198	A/D3	max 2.7	A/D3	max 2.7	A/D3	max 2.7
A/D2	J1.200	A/D2	max 2.7	A/D2	max 2.7	A/D2	max 2.7
A/D1	J1.202	A/D1	max 2.7	A/D1	max 2.7	A/D1	max 3.0
ADCIN6	J2.195	different function[1]	-	different function[1]	-	ADCIN6	max 2.7
ADCIN2	J2.196	different function[2]	-	different function[2]	-	ADCIN2	max 2.7
ADCIN1	J2.198	different function[3]	-	different function[3]	-	ADCIN1	max 2.7
ADCIN0	J2.200	different function[4]	-	different function[4]	-	ADCIN0	max 2.7
START_ADC	J2.79	-	-	-	-	START_ADC	1.8

Note(s):
1. iMX31/27 (J2.195) - Signal function is LED drive.
2. iMX31/27 (J2.196) - Signal function is LSPL, See MC13783 data sheet for more information.
3. iMX31/27 (J2.198) - Signal function is SPM, See MC13783 data sheet for more information.
4. iMX31/27 (J2.198) - Signal function is SPP, See MC13783 data sheet for more information.

6.4.13 Control Signals and GPIO Signals

Table 6.23 below describes the GPIO signals that are available for each SOM-LV. Several GPIO signals are available on each module; however, they also may be muxed with other functionality. Please note that some signals are GPO rather than GPIO.

Table 6.23: Available SOM-LV GPOs/GPIOs

GPO/GPIO Signal	SOM-LV J1/J2 Pin	i.MX31 SOM-LV				i.MX27 SOM-LV				OMAP35x SOM-LV			
		SOM-LV Signal	MC13783	SOC Pin	Voltage	SOM-LV Signal	MC13783	SOC Pin	Voltage	SOM-LV Signal	TPS65950	SOC Pin	Voltage
GPO	J2.219	ATLAS_GPO1	GPO1	-	2.7	ATLAS_GPO1	GPO1	-	2.7	different function	MICBIAS1.OUT/ VMIC1.OUT	-	bias
GPO	J2.217	ATLAS_GPO2	GPO2	-	2.7	ATLAS_GPO2	GPO2	-	2.7	different function	MICBIAS2.OUT/ VMIC2.OUT	-	bias
GPO/GPIO	J2.215	ATLAS_GPO3	GPO3	-	2.7	ATLAS_GPO3	GPO3	-	2.7	MCSPI1_CS0[7]	-	GPIO_174	1.8
GPIO	J1.34	uP_GPIO_7 [2]	-	MCU2_19	2.7	different function	-	TOUT1	1.8	uP_GPIO_7	GPIO.2	-	1.8
GPIO	J2.115	uP_GPIO_7 [2]	-	MCU2_19	2.7	-	-	-	-	different function	KPD.R5	-	1.8
GPIO	J1.36	uP_GPIO_6 [3]	-	MCU2_18	2.7	different function	-	TIN	1.8	uP_GPIO_6	GPIO.15	-	1.8
GPIO	J2117	uP_GPIO_6 [3]	-	MCU2_18	2.7	-	-	-	-	different function	KPD.R4	-	1.8
GPIO	J1.38	uP_GPIO_5	-	MCU1_29	2.7	different function	-	OE_ACD	1.8	uP_GPIO_5	GPIO.7	-	1.8
GPIO	J1.140	uP_GPIO_4	-	MCU1_30	2.7	-	-	-	-	uP_GPIO_4	GPIO.0	-	1.8
GPIO	J1.142	uP_GPIO_3	-	MCU1_31	2.7	uP_GPIO19	-	SSI2_FS	1.8	uP_GPIO_3	-	GPIO_111	1.8
GPIO	J1.166	uP_GPIO_2		MCU2_10	2.7	uP_GPIO18	-	SSI2_RXDAT	1.8	uP_GPIO_2	-	GPIO_31	1.8
GPIO	J2.17	-	-	-	-	-	-	-	-	HSUSB1_D7 [1]	-	GPIO_17	1.8
GPIO	J2.19	-	-	-	-	-	-	-	-	HSUSB1_D6 [1]	-	GPIO_20	1.8
GPIO	J2.152	different function[4]	-	LCS1/MCU3_24	1.8	different function	-	SSI4_FS_PC16	1.8	uP_GPIO_2	-	GPIO_31	1.8
GPIO	J2.154	different function[5]	-	LCS0/DISPB_BCLK/ MCU3_23	1.8	-	-	-	-	uP_GPIO_1	-	GPIO_111	1.8
GPIO	J2.156	different function	-	CONTRAST	1.8	different function	-	CONTRAST	1.8	BT_PCM_DX[7]	GPIO.17	-	1.8
GPIO	J2.158	different function[8]	-	WRITE	1.8	-	-	-	-	BT_PCM_DR[7]	GPIO.16	-	1.8
GPIO	J2.177	different function	LEDG3	-	max 5.5	different function	LEDG3	-	max 5.5	TWL_CLK256FS	CLKK_256FS	GPIO_160 [10]	1.8
GPIO	J2.191	different function	LEDG1	-	max 5.5	different function	LEDG1	-	max 5.5	MCSP1_SOMI[7]	-	GPIO_173	1.8
GPIO	J2.197	different function	LEDAD2	-	max 5.5	different function	LEDAD2	-	max 5.5	WLAN_MMC3_DATA3 [9]	-	GPIO_139	1.8
GPIO	J2.199	different function	LEDAD1	-	max 5.5	different function	LEDAD1	-	max 5.5	WLAN_MMC3_DATA2 [9]	-	GPIO_138	1.8
GPIO	J2.201	different function	LEDMD4	-	max 5.5	different function	LEDMD4	-	max 5.5	WLAN_MMC3_DATA1 [9]	-	GPIO_137	1.8
GPIO	J2.203	different function	LEDMD3	-	max 5.5	different function	LEDMD3	-	max 5.5	WLAN_MMC3_DATA0 [9]	-	GPIO_136	1.8
GPIO	J2.205	different function	LEDMD2	-	max 5.5	different function	LEDMD2	-	max 5.5	WLAN_MMC3_CMD[9]	-	GPIO_175	1.8
GPIO	J2.207	different function	LEDMD1	-	max 5.5	different function	LEDMD1	-	max 5.5	WLAN_MMC3_CLK[9]	-	GPIO_176	1.8
GPIO	J2.211	different function	-	HSLDET	2.7	different function	HSLDET	-	2.7	MCSPI1_CLK[7]	-	GPIO_171	1.8
GPIO	J2.213	different function	-	PC_PWRON/ SD2_D3/MSHC2_D2	2.8	different function	-	PC_PWRON/ATA_DA2	1.8	MCSPI1_SIMO[7]	-	GPIO_172	1.8
GPIO	J1.216	uP_GPIO_1 [6]	-	CAPTURE/ ATA_D14/CMP2/ MCU1_7	1.8	uP_GPIO17 [6]	-	SSI2_TXDAT	1.8	uP_GPIO_1 [6]	-	GPIO_11	1.8
GPIO	J1.218	uP_GPIO_0 [6]	-	COMPARE/ ATA_D15/CAP2/ CMP3/MCU1_8	1.8	-	-	-	-	uP_GPIO_0 [6]	-	GPIO_133	1.8
GPIO	J2.232	-	-	-	-	-	-	-	-	BT_IRQ[7]	-	GPIO_157	1.8

Note(s):

1. J2.17, J219 - Available as GPIO signal. Must not be driven when use of a ETM adapter board is required for debug of the SOM-LV.
2. J1.34, J2.115 - Reserved if keypad row 5 signal is requried.
3. J1.36, J2.117 - Reserved if keypad row 4 signal is required.
4. i.MX31/27 (J1.152) - Signal function is PCC_POWER_EN.
5. i.MX31 (J2.154) - Signal function is LCD_LCS0.
6. J1.216, J1.218 - Not recommended for general use. Used by LogicLoader as status LEDs.
7. J2.156:158:191:211:213 - OMAP35x signals are shared with the Bluetooth interface. The Bluetooth chipset must be removed to use this signal.
8. i.MX31 (J2.158) - Signal function is LCD_WRITE.
9. OMAP35x signal is shared with the Wireless LAN component. If wireless 802.11 is populated, do not connect.
10. J2.177 - CLK256FS on the TPS65950 must be disabled to use this signal as a GPIO.

6.5 Graphic Interfaces

This section discusses the camera sensor, LCD, and TV interface possibilities.

6.5.1 Camera Sensor Interface

The i.MX31 SOM-LV supports up to a 16-bit camera sensor interface (CSI), while the i.MX27 SOM-LV only supports an 8-bit CSI. On the i.MX31 SOM-LV, the most significant bits are used when connecting an 8-bit camera sensor to the SOM. This means that the upper data lines CSI[15:8] are used when connecting an 8-bit camera sensor. To accommodate this signal mapping for the i.MX31 SOM-LV, the i.MX27 SOM-LV routes the 8-bit CSI to the same pins on the J2 connector.

The OMAP35x SOM-LV can use the ITU mode to support image sensors using ITU-R BT 656-compatible data. Connect signals CAM_D[9:0] to the ITU-R BT.656 camera modules to use ITU-R BT modules. In SYNC mode, the OMAP35x SOM-LV supports 8-, 10-, 11-, and 12-bit data using the horizontal and vertical synchronization signals for the parallel interface.

The voltage is specific to each SOM-LV when interfacing to the various CSI controllers. The i.MX31 SOM-LV interface voltage is 2.8V, the OMAP35x SOM-LV voltage is 1.8V, and the i.MX27 SOM-LV voltage is 1.8V by default but can be set to variable by software without affecting any other interface signals.

If your baseboard design needs to support the same sensor on all three SOM-LVs, special care must be taken when determining the muxing of the data signals. See Table 6.24 below for details.

Table 6.24: SOM-LV Camera Sensor Interface

			i.MX31 SOM-LV			i.MX27 SOM-LV		OMAP35x SOM-LV				
CSI Signal	**SOM-LV J1/J2 Pin**	**SOM-LV Signal**	**uP Signal**	**Voltage**	**SOM-LV Signal**	**uP Signal**	**Voltage**	Parallel SYNC Mode	Parallel ITU Mode	**SOM-LV Signal**	**uP Signal**	**Voltage**
Reference Voltage Reg / Domain	i.MX31S: J1.144, J2.173 i.MX27S: J2.173 OMAPS: J1.110, J1.144	VCAM (REG) / NVCC4	NVCC4	2.8	VCAM (REG) / VCAM	NVDD11	1.8 (Variable[3])			VIO.SW (REG) / VIO_1V8	VDDS	**1.8**
CSI_HSYNC	J2.127	CSI_HSYNC	CSI_HSYNC	2.8	CSI_HSYNC	CSI_HSYNC	1.8 (Variable[3])	Yes	Yes	CSI_HSYNC	CAM_HS	1.8
CSI_VSYNC	J2.131	CSI_VSYNC	CSI_VSYNC	2.8	CSI_VSYNC	CSI_VSYNC	1.8 (Variable[3])	Yes	Yes	CSI_VSYNC	CAM_VS	1.8
CSI_D2	J2.137	CSI_D2	CSI_D2	2.8	-	-	-	Yes	Yes	CSI_D2	CAM_D2	1.8
CSI_D3	J2.139	CSI_D3	CSI_D3	2.8	-	-	-	Yes	Yes	CSI_D3	CAM_D3	1.8
CSI_D4	J2.141	CSI_D4	CSI_D4	2.8	-	-	-	Yes	Yes	CSI_D4	CAM_D4	1.8
CSI_D5	J2.143	CSI_D5	CSI_D5	2.8	-	-	-	Yes	Yes	CSI_D5	CAM_D5	1.8
CSI_D6	J2.145	CSI_D6	CSI_D6	2.8	-	-	-	Yes	Yes	CSI_D6	CAM_D6	1.8
CSI_D7	J2.147	CSI_D7	CSI_D7	2.8	-	-	-	Yes	Yes	CSI_D7	CAM_D7	1.8
CSI_D8	J2.151	CSI_D8	CSI_D8	2.8	CSI_D0	CSI_D0	1.8 (Variable[3])	Yes	Yes	CSI_D8	CAM_D8	1.8
CSI_D9	J2.153	CSI_D9	CSI_D9	2.8	CSI_D1	CSI_D1	1.8 (Variable[3])	Yes	Yes	CSI_D9	CAM_D9	1.8
CSI_D10	J2.155	CSI_D10	CSI_D10	2.8	CSI_D2	CSI_D2	1.8 (Variable[3])	Yes	GND	CSI_D10	CAM_D10	1.8
CSI_D11	J2.157	CSI_D11	CSI_D11	2.8	CSI_D3	CSI_D3	1.8 (Variable[3])	Yes	GND	CSI_D11	CAM_D11	1.8
CSI_D12	J2.159	CSI_D12	CSI_D12	2.8	CSI_D4	CSI_D4	1.8 (Variable[3])	-	-	-	-	-
CSI_D13	J2.161	CSI_D13	CSI_D13	2.8	CSI_D5	CSI_D5	1.8 (Variable[3])	-	-	-	-	-
CSI_D14	J2.163	CSI_D14	CSI_D14	2.8	CSI_D6	CSI_D6	1.8 (Variable[3])	-	-	-	-	-
CSI_D15	J2.165	CSI_D15	CSI_D15	2.8	CSI_D7	CSI_D7	1.8 (Variable[3])	-	-	-	-	-
CSI_MCLK	J2.167	CSI_MCLK	CSI_MCLK	2.8	CSI_MCLK	CSI_MCLK	1.8 (Variable[3])	Optional	Optional	CSI_MCLK	CAM_XCLKA	1.8
CSI_PCLK	J2.171	CSI_PCLK	CSI_PIXCLK	2.8	CSI_PCLK	CSI_PIXCLK	1.8 (Variable[3])	Yes	Yes	CSI_PCLK	CAM_PCLK	1.8
CAM_FLD	J1.119	-	-	-	-	-	-	Optional	-	uP_nIRQA	CAM_FLD	1.8
CAM_WEN	J1.117	-	-	-	-	-	-	Optional	-	uP_nIRQB	CAM_WEN	1.8
CAM_STROBE	J1.115	-	-	-	-	-	-	Optional	Optional	uP_nIRQC	CAM_STROBE	1.8
CAM_SHUTTER	J2.199	-	-	-	-	-	-	Optional	Optional	WLAN_MMC3_DATA2	CAM_SHUTTER/	1.8
CAM_SHUTTER	J1.117	-	-	-	-	-	-	Optional	Optional	uP_nIRQB	CAM_SHUTTER/	1.8
CAM_GLOBAL_RESET	J2.201	-	-	-	-	-	-	Optional	Optional	WLAN_MMC3_DATA1	CAM_GLOBAL_RESET	1.8
CAM_GLOBAL_RESET	J1.119	-	-	-	-	-	-	Optional	Optional	uP_nIRQA	CAM_GLOBAL_RESET	1.8
CAM_GLOBAL_RESET	J2.232 [4]	-	-	-	-	-	-	Optional	Optional	BT_IRQ	CAM_GLOBAL_RESET	1.8
Reference Voltage Reg / Domain	i.MX31S: J1.144, J2.173 OMAPS: -	-	same as above	2.8	-	-	-			VAUX4.OUT[1] (Reg) / VAUX4	CSI2_VDDS	1.8
CSI_D0	J2.133	CSI_D0	CSI_D0	2.8	-	-	-	Yes	Yes	CSI_D0	CAM_D0	1.8
CSI_D1	J2.135	CSI_D1	CSI_D1	2.8	-	-	-	Yes	Yes	CSI_D1	CAM_D1	1.8
Reference Voltage Reg / Domain	i.MX31S: J2.173 i.MX27S: J2.173 OMAPS: J1.183, J2.173	-	same as above	2.8	-	same as above	1.8 (Variable)			VPLL2.OUT[2] (REG) / VPLL2	VDDS_SDI	1.8
VREF_CSI	J2.173	VCAM	NVCC4	2.8	VCAM	NVDD11	1.8 (Variable)	Optional	Optional	VPLL2	-	1.8

Note(s):

1. OMAP35x/VAUX4.OUT - VAUX4.OUT must be programmed to the same voltage potential as VIO.SW when using CSI interface.
2. OMAP35x/VPLL2.OUT2 - REF#0003812: Changed to VIO_1V8 on schematics 1009917 Rev A and later.
3. i.MX27/NVDD11 - VCAM can be programmed to 1.8/2.5/2.55/2.6/2.75/2.8 volts and still meet the voltage requirements of NVDD11.
4. CAM_GLOBAL_RESET/J2.232 - Muxed with Bluetooth component. Bluetooth component (U12) must be depopulated.

To provide power for the camera interface signals, the i.MX31 and i.MX27 SOM-LVs use the VCAM regulator and the OMAP354x SOM-LV uses the VPLL2 regulator. A CSI reference voltage is also provided on J2.173.

6.5.2 LCD Interface

The i.MX31, i.MX27, and OMAP35x SOM-LVs all route the primary LCD control signals and the RGB signals in 5:6:5 configurations. All three SOM-LVs support active-matrix TFT color and mono configurations, as well as passive-matrix STN (color and mono). The i.MX27 and i.MX31 SOM-LVs support LCD panels using CPU I/Fs and Sharp HR-TFT like interfaces. The OMAP35x is the only SOM-LV that supports displays that require an RFBI mode interface. Please be aware that some control signals are common between the different SOM-LV modules and some are no connects. See Table 6.25 below for the routing of these signals.

Table 6.25: SOM-LV LCD Interface

		Signals for Display Support						i.MX31 SOM-LV	i.MX27 SOM-LV	OMAP35x SOM-LV
LCD Signal	SOM-LV J1/J2 Pin	Active TFT color/mono	Sharp HR-TFT[3]	Passive STN/CSTN[2]	Serial CPU I/F[9]	8/16-bit CPU I/F[6]	RFBI[4]	uP Signal	uP Signal	uP Signal
Reference Voltage Reg / Domain	i.MX31S: J1.183 i.MX27S: J2.96, J2.122, J1.183 OMAPS: J1.110, J1.144							VIOLO (Reg) / 1.8V_NVCC7	SW2BOUT (Reg) / DVDD_1.8V	VIO.SW (REG) / VIO_1V8
LCD_VSYNC	J1.167	Yes	-	Yes	-	-	Yes	VSYNC3	VSYNC	DSS_VSYNC
LCD_HSYNC	J1.165	Yes	-	Yes	-	-	Yes	HSYNC	HSYNC	DSS_HSYNC
LCD_DCLK	J1.171	Yes	-	Yes	-	-	Yes	DISPB_BCLK	LSCLK	DSS_PCLK
LCD_PANEL_PWR	J1.161	-	-	-	SD_D_CLK	-	-	MCU3_22	PB31	GPIO_155
LCD_BACKLIGHT_PWR	J1.163	-	-	-	SD_D_I	-	-	MCU3_20	PC27	GPIO_8
LCD_MDISP	J1.175	Yes	-	Yes	-	-	Yes	DRDY0	SLCDC1_CS	DSS_ACBIAS
LCD_G1	J1.199	Yes	Yes	Yes	-	Yes	Yes	LD7	LD7	DSS_D6
LCD_G2	J1.201	Yes	Yes	Yes	-	Yes[7]	Yes	LD8	LD8	DSS_D7
LCD_G3	J1.203	Yes	Yes	Yes	-	Yes[7]	Yes	LD9	LD9	DSS_D8
LCD_G4	J1.205	Yes	Yes	Yes	-	Yes[7]	Yes	LD10	LD10	DSS_D9
LCD_D16	J2.188	-	-	-	-	-	Yes	-	-	DSS_D16
LCD_D17	J2.186	-	-	-	-	-	Yes	-	-	DSS_D17
LCD_D18	J2.184	-	-	-	-	-	Yes[5]	-	-	DSS_D18
LCD_D19	J2.182	-	-	-	-	-	Yes[5]	-	-	DSS_D19
LCD_D20	J2.180	-	-	-	-	-	Yes[5]	-	-	DSS_D20
LCD_D21	J2.178	-	-	-	-	-	-	-	-	DSS_D21
Reference Voltage Reg / Domain	i.MX31S J1.183 i.MX27S J2.96, J2.122, J1.183 OMAPS J1.183, J2.173							same as above	same as above	VPLL2.OUT[1] (REG) / VPLL2
LCD_G0	J1.197	Yes	Yes	Yes	-	Yes	Yes	LD6	LD6	DSS_D5
LCD_G5	J1.207	Yes	Yes	Yes	-	Yes[7]	Yes	LD11	LD11	DSS_D10
LCD_B1	J1.211	Yes	Yes	Yes	-	Yes	Yes	LD1	LD1	DSS_D0
LCD_B2	J1.213	Yes	Yes	Yes	-	Yes	Yes	LD2	LD2	DSS_D1
LCD_B3	J1.215	Yes	Yes	Yes	-	Yes	Yes	LD3	LD3	DSS_D2
LCD_B4	J1.217	Yes	Yes	Yes	-	Yes	Yes	LD4	LD4	DSS_D3
LCD_B5	J1.219	Yes	Yes	Yes	-	Yes	Yes	LD5	LD5	DSS_D4
LCD_R1	J1.185	Yes	Yes	Yes	-	Yes[7]	Yes	LD13	LD13	DSS_D11
LCD_R2	J1.187	Yes	Yes	Yes	-	Yes[7]	Yes	LD14	LD14	DSS_D12
LCD_R3	J1.191	Yes	Yes	Yes	-	Yes[7]	Yes	LD15	LD15	DSS_D13
LCD_R4	J1.193	Yes	Yes	Yes	-	-	Yes	LD16	LD16	DSS_D14
LCD_R5	J1.195	Yes	Yes	Yes	-	-	Yes	LD17	LD17	DSS_D15
LCD_B0	J2.182	Yes	Yes	Yes	-	Yes	-	LD0	LD0	-
LCD_R0	J2.188	Yes	Yes	Yes	-	Yes[7]	-	LD12	LD12	-
LCD_CLS	J1.155	-	Yes	-	-	-	-	D3_CLS	CLS	-
LCD_PSAVE	J1.177	-	Yes	-	-	-	-	DRDY0	PS	-
LCD_REV	J1.173	-	Yes	-	-	-	-	D3_REV	REV	-
LCD_SPL	J1.151	-	Yes	-	-	-	-	D3_SPL	SPL_SPR	-
LCD_HRLP	J1.159	-	Yes	-	-	-	-	HSYNC	-	-
LCD_SPS	J1.157	-	Yes	-	-	-	-	VSYNC3	-	-

Table 6.25: SOM-LV LCD Interface (continued)

LCD Signal	SOM-LV J1/J2 Pin	Signals for Display Support						i.MX31 SOM-LV	i.MX27 SOM-LV	OMAP35x SOM-LV
		Active TFT color/mono	Sharp HR-TFT[3]	Passive STN/CSTN[2]	Serial CPU I/F[9]	8/16-bit CPU I/F[6]	RFBI[4]	uP Signal	uP Signal	uP Signal
Reference Voltage Reg / Domain	i.MX31S J1.183 i.MX27S J2.96, J2.122, J1.183 OMAPS J1.183, J2.173							same as above	same as above	VPLL2.OUT[1] (REG) / VPLL2
LCD_DON	J1.153	-	-	-	SD_D_IO	-	-	MCU3_21	PB30	GPIO.1 (TPSG5950 signal)
LCD_LCS0	J2.154	-	-	-	-	Yes	-	LCS0	-	-
LCD_PAR_RS	J2.164	-	-	-	-	Yes	-	PAR_RS	-	-
LCD_READ	J2.160	-	-	-	-	Yes	-	READ	-	-
LCD_SER_RS	J1.166	-	-	-	SD_SER_RS	-	-	SER_RS	-	-
LCD_VSYNC0	J2.162	-	-	-	-	Yes	-	VSYNC0	-	-
LCD_WRITE	J2.158	-	-	-	-	Yes	-	WRITE	-	-
LCD_CONTRAST	J2.156	-	-	-	-	-	-	CONTRAST	CONTRAST	-
LCD_OE_ACD	J1.38	-	-	-	-	-	-	-	OE_ACD	-
LCD_D22	J2.176	-	-	-	-	-	-	-	-	DSS_D22
LCD_D23	J2.174	-	-	-	-	-	-	-	-	DSS_D23
LCD_CLK_RETURN	J1.179	-	-	-	-	-	-	-	-	-
LCD_LCS1	J2.135	-	-	-	DISPB_D1_CS[10]	-	-	LCS1		
LCD_MOD	J1.181	-	-	-	-	-	-	-	-	-
Reference Voltage Reg / Domain	i.MX31S: J1.183 i.MX27S: J2.96, J2.122, J1.183 OMAPS: J2.122							VRF1 (REG) / 2.7V_NVCC6/NVCC9		
LCD_SER_D2_CS	J2.126	-	-	-	SD_D2_CS[8, 10]	-	-	SRST0	-	-
LCD_SER_VSYNC	J2.132	-	-	-	SD_D12_VSYNC[8]	-	-	SVEN0	-	-

Note(s):
1. VPLL2.OUT must remain programmed to the same voltage potential as VIO.SW when using LCD interface.
2. STN (mono/color) displays will typically use 4 or 8 data signals, meaning all of the data signals would not be used.
3. The Sharp HR-TFT displays using the typical HR-TFT interface are supported directly with the i.MX27 and i.MX31 SOM-LV modules. This interface is also seen on some AD-TFT LCD panels.
4. Supported only by the OMAP35x SOM-LV.
5. Signals required only when using a second LCD panel.
6. Both system 80 and system 68k asynchronous interfaces are supported by the i.MX31 SOM-LV. Refer to the MCIMX31 Datasheet and Technical Reference Manual for more information.
7. Required only for 16-bit interface.
8. Voltage translators will be required on baseboard for 1.8V interface to LCD.
9. 3-, 4-, and 5-wire asynchronous serial interfaces are supported by the i.MX31 SOM-LV. Refer to the MCIMX31 Datasheet and Technical Reference Manual for more information.
10. Only one chip select signal is required between DISPB_D1_CS and SD_D2_CS when using the serial interface.

6.5.3 TV Display Interface

The OMAP35x SOM-LV supports interfacing to TV displays using an integrated TV OUT Encoder module within the OMAP35x SOC. The TV OUT Encoder module can connect in either S-Video mode or composite mode. See Table 6.26 below for details.

Table 6.26: SOM-LV TV Display Interface

TV Signal	S-Video	Composite	J1/J2 Pin	i.MX31 SOM-LV	i.MX27 SOM-LV	OMAP35x SOM-LV	
				SOM-LV Signal	SOM-LV Signal	SOM-LV Signal	Voltage
Reference Voltage Reg / Domain	-	-	-	-	-	VDAC.OUT (LDO) / VDAC	1.8 [1]
TV_OUT1	Luminance Output	Composite Output	J2.194	-	-	TV_OUT1 [2,3]	1.8 [1]
TV_OUT2	Chrominance Output	-	J2.192	-	-	TV_OUT2 [2,3]	1.8 [1]

Note(s):
1. VDAC.OUT on the OMAP35x SOM-LV can be programmed to any of the following voltages (1.2 V, 1.3 V,1.8 V).
2. TV_OUT1 and TV_OUT2 are very high-frequency analog signals and must be routed with extreme care. As a result, the path of these signals should be as short as possible and as isolated as possible from other interfering signals.
3. The TV OUT pins must have a characteristic impedance of 75, starting from the closest possible location to the OMAP35x SOM-LV.

6.6 BDM/JTAG Interface

The BDM/JTAG interface provides access to on-chip debugging features in order to control and monitor the microcontroller. Access to the BDM/JTAG interface occurs through a 20-pin 100mil stake header. The specific pins are detailed in Table 6.27 below.

To access the BDM/JTAG interface on the i.MX31, i.MX27, and OMAP35x SOM-LVs, Logic uses Abatron BDI tools because of their robustness and feature-rich functionally. Details of Abatron BDI tools are available online at: http://www.abatron.ch/.

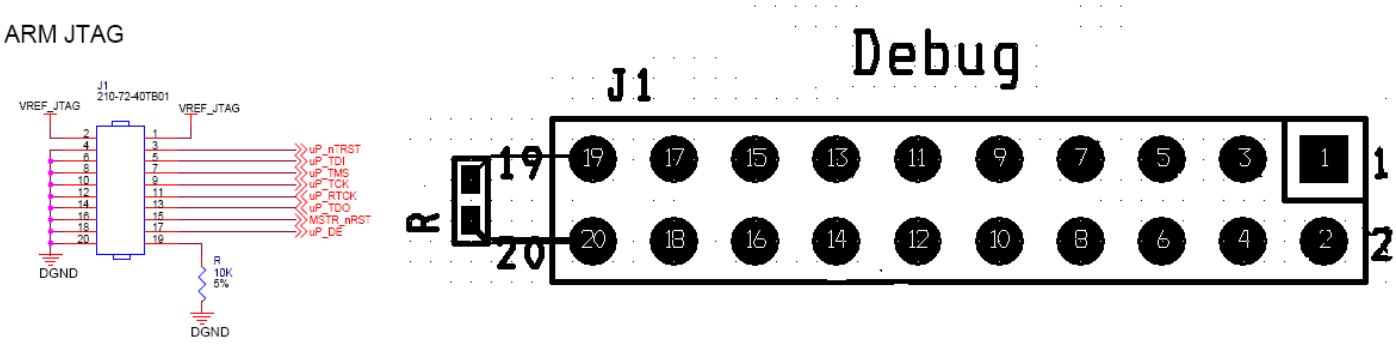
Table 6.27: SOM-LV JTAG Interface

Debug Signal	J1/J2 Pin	i.MX31 SOM-LV		i.MX27 SOM-LV		OMAP35x SOM-LV	
		SOM-LV Signal	i.MX31 Signal	SOM-LV Signal	i.MX27 Signal	SOM-LV Signal	OMAP35x Signal
Reference Voltage Reg / Domain	J2.122	VRF1 (REG) / 2.7V_NVCC6/NVCC9	NVCC6	SW2BOUT (REG) / DVDD_1.8V	NVDD8/NVDD13	VIO.SW (REG) / VIO_1V8	VDDS
nTRST	J2.116	uP_nTRST	TRSTB	uP_nTRST	TRST_B	uP_nTRST	JTAG_nTRST
TDI	J2.118	uP_TDI	TDI	uP_TDI	TDI	uP_TDI	JTAG_TDI
TMS	J2.108	uP_TMS	TMS	uP_TMS	TMS	uP_TMS	JTAG_TMS_TMSC
TCK	J2.110	uP_TCK	TCK	uP_TCK	TCK	uP_TCK	JTAG_TCK
RTCK	J2.120	uP_RTCK	RTCK	uP_RTCK/1WIRE	RTCK/OWIRE	uP_RTCK	JTAG_RTCK
TDO	J2.114	uP_TDO	TDO	uP_TDO	TDO	uP_TDO	JTAG_TDO
MSTR_nRST	J1.227	MSTR_nRST	POR_B	POWER_ON_RESET	POWER_ON_RESET	MSTR_nRST	SYS_nRESPWRON
DE	J1.106	uP_DE	DE_B	-	-	-	-
uP_TEST1	J2.102	uP_TEST1	SJC_MOD	-	-	-	-
uP_TEST2	J2.104	uP_TEST2	CE_CONTROL	-	-	-	-
uP_DE	J2.106	uP_DE	DE_B	-	-	-	-
EMU0	J2.154	-	-	-	-	uP_GPIO_1	JTAG_EMU0
EMU1	J2.152	-	-	-	-	uP_GPIO_2	JTAG_EMU1

The baseboard design for all three SOM-LV modules must have a 10K pull-down to ground as shown in Figure 6.2 below.

The recommended schematic connection and layout for the JTAG interface can be seen in Figure 6.2 below. The layout is a top view of the recommended 100mil connector.

Figure 6.2: Recommended JTAG Interface Connection

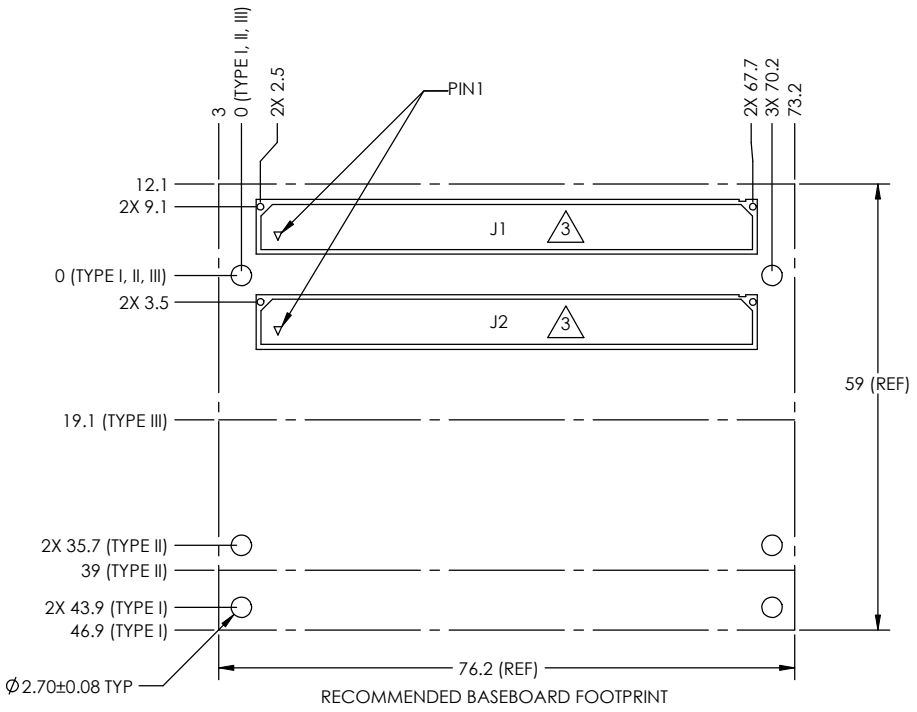


7 Summary

This Application Note attempts to explain the differences between the i.MX31, i.MX27, and the OMAP35x SOM-LVs to help in creating a mutually compatible baseboard design. However, designers should take great care when attempting to use any combination of modules with the same baseboard, as tradeoffs may be necessary for a successful design.

Appendix A: SOM-LV Baseboard Footprint Drawing

REVISIONS			
REV.	ECO NUMBER	DESCRIPTION	DATE
A	-	INITIAL RELEASE	08.07.08



RECOMMENDED BASEBOARD FOOTPRINT

NOTES:

1. WITHIN LAYOUT AREA OF SOM-LV, MAXIMUM COMPONENT HEIGHT ON APPLICATION BASEBOARD IS 1.0 MM
2. SOM-LV TYPE III USES ONLY TWO HOLES
3. BASEBOARD CONNECTOR SPECIFICATION: SAMTEC BSH-120-01-L-D-A
4. DO NOT SCALE DRAWING

THIS DRAWING PREPARED IN ACCORDANCE WITH ASME Y14.5-2000

ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED
X ± 0.5
X.X ± 0.2
X.XX ± 0.1
X° ± 1°

THIRD ANGLE PROJECTION

ENG KAG	DATE 08.07.08	LOGIC 411 N. Washington Ave. Suite 400 Minneapolis, MN 55401 T:612.672.8485 F:612.672.8489 I:www.logicpd.com	SIZE C	TITLE SOM-LV Form Factor Footprint	REV A
CHECK JPS	DATE 08.07.08				
MGR PMH	DATE 08.07.08		SCALE 2:1	DWG NO 1010581	SHEET 1 OF 1
MANF -	DATE -				

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
1	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
2	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
3	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
4	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
5	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
6	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
7	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
8	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
9	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
10	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
11	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
12	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
13	uP_nWAKEUP	I	1.8V	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 10K pull-up.	uP_nWAKEUP	I	1.8V	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 10K pull‑up.	uP_nWAKEUP	I	MAIN_BATTERY	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 4.75K pull‑up.	This signals should only be driven low from the baseboard for compatiability for all 3 SOM-LV cards.
14	ETHER_TX+	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-). Requires external magnetics. See example SDK baseboard designs for reference components.	ETHER_TX+	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-). Requires external magnetics. See example LV‑Baseboard designs for reference components.	ETHER_TX+	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX-. Requires external magnetics. See example LV‑Baseboard design for reference components.	Layout your baseboard identical to the LITEKIT baseboard LPD#1005441 with R1, R4, C1, and C2 populated will be compatiable with all 3 SOM-LV cards.
15	nSUSPEND	I	2.7V	Active low. Software can use this signal to enter low power states from RUN mode. Software is required for correct operation. This signal has a 10K pull-up.	nSUSPEND	I	2.7V	Active low. Software can use this signal to enter low power states from RUN mode. Software is required for correct operation. This signal has a 10K pull-up.	nSUSPEND	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.	Same on i.MX31, i.MX27 and OMAP35x.
16	ETHER_TX-	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+). Requires external magnetics. See example SDK baseboard designs for reference components.	ETHER_TX-	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+). Requires external magnetics. See example LV-Baseboard designs for reference components.	ETHER_TX-	O	3.3V	This output pair drives 10/100 Mb/s data to the transmit lines. Route as differential pair with ETHER_TX+. Requires external magnetics. See example LV-Baseboard design for reference components.	Layout your baseboard identical to the LITEKIT baseboard LPD#1005441 with R1, R4, C1, and C2 populated will be compatiable with all 3 SOM-LV cards.
17	nSTANDBY	I	2.7V	Active low. Software can use this signal to enter low power states from RUN mode. Software is required for correct operation. This signal has a 10K pull-up.	nSTANDBY	I	2.7V	Active low. Software can use this signal to enter low power states from RUN mode. Software is required for correct operation. This signal has a 10K pull-up.	nSTANDBY	I	1.8V	Software can use this signal to enter low power states from RUN mode. Software is required for correct operation.	Same on i.MX31, i.MX27 and OMAP35x.
18	ETHER_RX+	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-). Requires external magnetics. See example SDK baseboard designs for reference components.	ETHER_RX+	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-). Requires external magnetics. See example LV‑Baseboard designs for reference components.	ETHER_RX+	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX-. Requires external magnetics. See example LV‑Baseboard design for reference components.	Lay out your baseboard identical to the LITEKIT baseboard LPD#1005441 with R1, R4, C1, and C2 populated will be compatiable with all 3 SOM-LV cards.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
19	USB1_ID	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example SDK baseboard designs for reference components.	USB1_ID	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example LV-Baseboard designs for reference components.	USB1_ID	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example LV-Baseboard design for reference components.	See USB section for compatibility information.
20	ETHER_RX-	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+). Requires external magnetics. See example SDK baseboard designs for reference components.	ETHER_RX-	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+). Requires external magnetics. See example LV-Baseboard designs for reference components.	ETHER_RX-	I	3.3V	This input pair receives 10/100 Mb/s data from the receive lines. Route as differential pair with ETHER_RX+. Requires external magnetics. See example LV‑Baseboard design for reference components.	Lay out your baseboard identical to the LITEKIT baseboard LPD#1005441 with R1, R4, C1, and C2 populated will be compatiable with all 3 SOM-LV cards.
21	USB1_VBUS	I	5.0V	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected as well as provides power to USB Device peripherals. See example SDK baseboard designs for reference components.	USB1_VBUS	I	5.0V	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected as well as provides power to USB Device peripherals. See example LV-Baseboard designs for reference components.	USB1_VBUS	I/O	5.0V	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected or can provide power to USB Device peripherals. See example LV-Baseboard design for reference components.	See USB section for compatibility information.
22	ACT_nLNK_LED/LAN_LED2	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example SDK baseboard designs for reference components.	ACT_nLNK_LED/LAN_LED2	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example LV‑Baseboard designs for reference components.	ACT_nLNK_LED/LAN_LED2	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example LV‑Baseboard design for reference components.	LAN9117-MT on i.MX31, LAN8700 on i.MX27, LAN9211 on OMAP35x
23	USB1_nOC	I	3.3V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port.	USB1_nOC	I	3.3V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port.	USB1_nOC	I	1.8V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port.	See USB section for compatibility information.
24	SPD_LED_n100M_10M/LAN_LED1	O	3.3V	Active low. Asserts to indicate operation speed, either 10 Mb or 100 Mb connection. See example SDK baseboard designs for reference components.	SPD_LED_n100M_10M/LAN_LED1	O	3.3V	Active low. Asserts to indicate operation speed, either 10 Mb or 100 Mb connection. See example LV‑Baseboard designs for reference components.	SPD_LED_n100M_10M/LAN_LED1	O	3.3V	Active low. Asserts to indicate operation speed, either 10Mbs (high) or 100Mbs (low) connection. See example LV‑Baseboard design for reference components.	LAN9117-MT on i.MX31, LAN8700 on i.MX27, LAN9211 on OMAP35x
25	USB1_PWR_nEN	O	3.3V	Active low. USB OTG power enable. Enables power to the external USB power switch. See example SDK baseboard designs for reference components.	USB1_PWR_nEN	O	3.3V	Active low. USB OTG power enable. Enables power to the external USB power switch. See example LV‑Baseboard designs for reference components.	USB1_PWR_nEN	O	1.8V	Active low. USB OTG power enable. Enables power to the external USB power switch.	See USB section for compatibility information.
26	VREF_ETHERNET	O	3.3V	AC coupled to GND. Output from the SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example SDK baseboard designs for reference components.	3.3V	O	3.3V	AC coupled to GND. Output from the SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example LV‑Baseboard designs for reference components.	VREF_ETHERNET (3.3V_A)	O	3.3V	Output from the SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example LV‑Baseboard design for reference components.	Same on i.MX31, i.MX27 and OMAP35x, see ethernet section for detail information.
27	USB1_D+	I/O	3.3V	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB1_D+	I/O	Variable	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB1_D+	I/O	Variable	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	See USB section for compatibility information.
28	uP_AUX_CLK	O	1.8V	Processor's CLKO output.	uP_AUX_CLK	O	1.8V	Processor's CLKO output.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pwr/clk/rst section for more information
29	USB1_D-	I/O	3.3V	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB1_D-	I/O	Variable	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB1_D-	I/O	Variable	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	See USB section for compatibility information.
30	PWR_ON	I	2.7V	Active high. Software can use this signal to enter RUN from low power modes. Software is required for correct operation. This signal has a 10K pull-up.	PWR_ON	I	2.7V	Active high. Software can use this signal to enter RUN from low power modes. Software is required for correct operation. This signal has a 10K pull-up.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31 and i.MX27. Signal is routed to Altas on both SOMs, RFU on OMAP35x
31	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
32	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
33	USB2_D+	I/O	3.3V	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB2_D+	I/O	Variable	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB2_D+	I/O	Variable	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	See USB section for compatibility information.
34	uP_GPIO_7	I/O	2.7V (NVCC6)	Processor GPIO available to user.	uP_TIMER_OUT	O	1.8V	Processor GPIO available to user.	uP_GPIO_7	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.2.	See GPIO section for compatibility information
35	USB2_D-	I/O	3.3V	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB2_D-	I/O	Variable	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	USB2_D-	I/O	Variable	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.	See USB section for compatibility information.
36	uP_GPIO_6	I/O	2.7V (NVCC6)	Processor GPIO available to user.	uP_TIMER_IN	I	1.8V	Processor GPIO available to user.	uP_GPIO_6	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.15.	See GPIO section for compatibility information
37	USB2_nOC	I	3.3V	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.	USB2_nOC	I	3.3V	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.	USB2_nOC	I	3.3V	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.	See USB section for compatibility information.
38	uP_GPIO_5	I/O	2.7V (NVCC5)	Processor GPIO available to user.	LCD_OE_ACD	O	1.8V	Processor GPIO available to user.	uP_GPIO_5	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.7.	See GPIO section for compatibility information
39	USB2_PWR_nEN	O	5.0V	Active low. USB Host power enable. Enables power to the external USB power switch. See example SDK baseboard designs for reference components.	USB2_PWR_nEN	O	5.0V	Active low. USB Host power enable. Enables power to the external USB power switch. See example LV-Baseboard designs for reference components.	USB2_PWR_nEN	O	5.0V	Active low. USB Host power enable. Enables power to the external USB power switch. See example LV-Baseboard design for reference components.	See USB section for compatibility information.
40	uP_D0	I/O	1.8V	Processor Host bus (WEIM bus) data bit 0.	uP_D0	I/O	1.8V	Processor Host bus (WEIM bus) data bit 0.	uP_D0	O	1.8V	Processor GPMC bus data bit 0.	See memory section for compatibility information.
41	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
42	uP_D1	I/O	1.8V	Processor Host bus (WEIM bus) data bit 1.	uP_D1	I/O	1.8V	Processor Host bus (WEIM bus) data bit 1.	uP_D1	O	1.8V	Processor GPMC bus data bit 1.	See memory section for compatibility information.
43	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
44	uP_D2	I/O	1.8V	Processor Host bus (WEIM bus) data bit 2.	uP_D2	I/O	1.8V	Processor Host bus (WEIM bus) data bit 2.	uP_D2	O	1.8V	Processor GPMC bus data bit 2.	See memory section for compatibility information.
45	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
46	uP_D3	I/O	1.8V	Processor Host bus (WEIM bus) data bit 3.	uP_D3	I/O	1.8V	Processor Host bus (WEIM bus) data bit 3.	uP_D3	O	1.8V	Processor GPMC bus data bit 3.	See memory section for compatibility information.
47	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
48	uP_D4	I/O	1.8V	Processor Host bus (WEIM bus) data bit 4.	uP_D4	I/O	1.8V	Processor Host bus (WEIM bus) data bit 4.	uP_D4	O	1.8V	Processor GPMC bus data bit 4.	See memory section for compatibility information.
49	3.3V_nEN	O	2.7V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.	3.3V_nEN	O	2.7V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.	3.3V_nEN (DGND)	O	1.8V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.	Same on i.MX31, i.MX27 and OMAP35x.
50	uP_D5	I/O	1.8V	Processor Host bus (WEIM bus) data bit 5.	uP_D5	I/O	1.8V	Processor Host bus (WEIM bus) data bit 5.	uP_D5	O	1.8V	Processor GPMC bus data bit 5.	See memory section for compatibility information.
51	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
52	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
53	A0 (DGND)	O	GND	Processor Host bus (WEIM bus) address bit 0.	A0 (DGND)	O	GND	Processor Host bus (WEIM bus) address bit 0. (see note 1 at the end of this table)	A0 (DGND)	O	1.8V	Processor GPMC bus address bit 0.	Same on i.MX31, i.MX27 & OMAP35x
54	uP_D6	I/O	1.8V	Processor Host bus (WEIM bus) data bit 6.	uP_D6	I/O	1.8V	Processor Host bus (WEIM bus) data bit 6.	uP_D6	O	1.8V	Processor GPMC bus data bit 6.	See memory section for compatibility information.
55	A1 (uP_MA0)	O	1.8V	Processor Host bus (WEIM bus) address bit 1.	A1 (uP_MA0)	O	1.8V	Processor Host bus (WEIM bus) address bit 1.	A1 (uP_LA1)	O	1.8V	Latched Processor GPMC bus address bit 1.	See memory section for compatibility information.
56	uP_D7	I/O	1.8V	Processor Host bus (WEIM bus) data bit 7.	uP_D7	I/O	1.8V	Processor Host bus (WEIM bus) data bit 7.	uP_D7	O	1.8V	Processor GPMC bus data bit 7.	See memory section for compatibility information.
57	A2 (uP_MA1)	O	1.8V	Processor Host bus (WEIM bus) address bit 2.	A2 (uP_MA1)	O	1.8V	Processor Host bus (WEIM bus) address bit 2.	A2 (uP_LA2)	O	1.8V	Latched Processor GPMC bus address bit 2.	See memory section for compatibility information.
58	uP_D8	I/O	1.8V	Processor Host bus (WEIM bus) data bit 8.	uP_D8	I/O	1.8V	Processor Host bus (WEIM bus) data bit 8.	uP_D8	O	1.8V	Processor GPMC bus data bit 8.	See memory section for compatibility information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
59	A3 (uP_MA2)	O	1.8V	Processor Host bus (WEIM bus) address bit 3.	A3 (uP_MA2)	O	1.8V	Processor Host bus (WEIM bus) address bit 3.	A3 (uP_LA3)	O	1.8V	Latched Processor GPMC bus address bit 3.	See memory section for compatibility information.
60	uP_D9	I/O	1.8V	Processor Host bus (WEIM bus) data bit 9.	uP_D9	I/O	1.8V	Processor Host bus (WEIM bus) data bit 9.	uP_D9	O	1.8V	Processor GPMC bus data bit 9.	See memory section for compatibility information.
61	A4 (uP_MA3)	O	1.8V	Processor Host bus (WEIM bus) address bit 4.	A4 (uP_MA3)	O	1.8V	Processor Host bus (WEIM bus) address bit 4.	A4 (uP_LA4)	O	1.8V	Latched Processor GPMC bus address bit 4.	See memory section for compatibility information.
62	uP_D10	I/O	1.8V	Processor Host bus (WEIM bus) data bit 10.	uP_D10	I/O	1.8V	Processor Host bus (WEIM bus) data bit 10.	uP_D10	O	1.8V	Processor GPMC bus data bit 10.	See memory section for compatibility information.
63	A5 (uP_MA4)	O	1.8V	Processor Host bus (WEIM bus) address bit 5.	A5 (uP_MA4)	O	1.8V	Processor Host bus (WEIM bus) address bit 5.	A5 (uP_LA5)	O	1.8V	Latched Processor GPMC bus address bit 5.	See memory section for compatibility information.
64	uP_D11	I/O	1.8V	Processor Host bus (WEIM bus) data bit 11.	uP_D11	I/O	1.8V	Processor Host bus (WEIM bus) data bit 11.	uP_D11	O	1.8V	Processor GPMC bus data bit 11.	See memory section for compatibility information.
65	A6 (uP_MA5)	O	1.8V	Processor Host bus (WEIM bus) address bit 6.	A6 (uP_MA5)	O	1.8V	Processor Host bus (WEIM bus) address bit 6.	A6 (uP_LA6)	O	1.8V	Latched Processor GPMC bus address bit 6.	See memory section for compatibility information.
66	uP_D12	I/O	1.8V	Processor Host bus (WEIM bus) data bit 12.	uP_D12	I/O	1.8V	Processor Host bus (WEIM bus) data bit 12.	uP_D12	O	1.8V	Processor GPMC bus data bit 12.	See memory section for compatibility information.
67	A7 (uP_MA6)	O	1.8V	Processor Host bus (WEIM bus) address bit 7.	A7 (uP_MA6)	O	1.8V	Processor Host bus (WEIM bus) address bit 7.	A7 (uP_LA7)	O	1.8V	Latched Processor GPMC bus address bit 7.	See memory section for compatibility information.
68	uP_D13	I/O	1.8V	Processor Host bus (WEIM bus) data bit 13.	uP_D13	I/O	1.8V	Processor Host bus (WEIM bus) data bit 13.	uP_D13	O	1.8V	Processor GPMC bus data bit 13.	See memory section for compatibility information.
69	A8 (uP_MA7)	O	1.8V	Processor Host bus (WEIM bus) address bit 8.	A8 (uP_MA7)	O	1.8V	Processor Host bus (WEIM bus) address bit 8.	A8 (uP_LA8)	O	1.8V	Latched Processor GPMC bus address bit 8.	See memory section for compatibility information.
70	uP_D14	I/O	1.8V	Processor Host bus (WEIM bus) data bit 14.	uP_D14	I/O	1.8V	Processor Host bus (WEIM bus) data bit 14.	uP_D14	O	1.8V	Processor GPMC bus data bit 14.	See memory section for compatibility information.
71	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
72	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
73	A9 (uP_MA8)	O	1.8V	Processor Host bus (WEIM bus) address bit 9.	A9 (uP_MA8)	O	1.8V	Processor Host bus (WEIM bus) address bit 9.	A9 (uP_LA9)	O	1.8V	Latched Processor GPMC bus address bit 9.	See memory section for compatibility information.
74	uP_D15	I/O	1.8V	Processor Host bus (WEIM bus) data bit 15.	uP_D15	I/O	1.8V	Processor Host bus (WEIM bus) data bit 15.	uP_D15	O	1.8V	Processor GPMC bus data bit 15.	See memory section for compatibility information.
75	A10 (uP_MA9)	O	1.8V	Processor Host bus (WEIM bus) address bit 10.	A10 (uP_MA9)	O	1.8V	Processor Host bus (WEIM bus) address bit 10.	A10 (uP_LA10)	O	1.8V	Latched Processor GPMC bus address bit 10.	See memory section for compatibility information.
76	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D16 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
77	A11 (uP_MA10)	O	1.8V	Processor Host bus (WEIM bus) address bit 11.	A11 (uP_MA10)	O	1.8V	Processor Host bus (WEIM bus) address bit 11.	A11 (uP_LA11)	O	1.8V	Latched Processor GPMC bus address bit 11.	See memory section for compatibility information.
78	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D17 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
79	A12 (uP_MA11)	O	1.8V	Processor Host bus (WEIM bus) address bit 12.	A12 (uP_MA11)	O	1.8V	Processor Host bus (WEIM bus) address bit 12.	A12 (uP_LA12)	O	1.8V	Latched Processor GPMC bus address bit 12.	See memory section for compatibility information.
80	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D18 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
81	A13 (uP_MA12)	O	1.8V	Processor Host bus (WEIM bus) address bit 13.	A13 (uP_MA12)	O	1.8V	Processor Host bus (WEIM bus) address bit 13.	A13 (uP_LA13)	O	1.8V	Latched Processor GPMC bus address bit 13.	See memory section for compatibility information.
82	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D19 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
83	A14 (uP_A13)	O	1.8V	Processor Host bus (WEIM bus) address bit 14.	A14 (uP_A13)	O	1.8V	Processor Host bus (WEIM bus) address bit 14.	A14 (uP_LA14)	O	1.8V	Latched Processor GPMC bus address bit 14.	See memory section for compatibility information.
84	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D20 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
85	A15 (uP_A14)	O	1.8V	Processor Host bus (WEIM bus) address bit 15.	A15 (uP_A14)	O	1.8V	Processor Host bus (WEIM bus) address bit 15.	A15 (uP_LA15)	O	1.8V	Latched Processor GPMC bus address bit 15.	See memory section for compatibility information.
86	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D21 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
87	A16 (uP_A15)	O	1.8V	Processor Host bus (WEIM bus) address bit 16.	A16 (uP_A15)	O	1.8V	Processor Host bus (WEIM bus) address bit 16.	A16 (uP_LA16)	O	1.8V	Latched Processor GPMC bus address bit 16.	See memory section for compatibility information.
88	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D22 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
89	A17 (uP_A16)	O	1.8V	Processor Host bus (WEIM bus) address bit 17.	A17 (uP_A16)	O	1.8V	Processor Host bus (WEIM bus) address bit 17.	A17 (uP_A1)	O	1.8V	Processor GPMC bus address bit 17.	See memory section for compatibility information.
90	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D23 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
91	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
92	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
93	A18 (uP_A17)	O	1.8V	Processor Host bus (WEIM bus) address bit 18.	A18 (uP_A17)	O	1.8V	Processor Host bus (WEIM bus) address bit 18.	A18 (uP_A2)	O	1.8V	Processor GPMC bus address bit 18.	See memory section for compatibility information.
94	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D24 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
95	A19 (uP_A18)	O	1.8V	Processor Host bus (WEIM bus) address bit 19.	A19 (uP_A18)	O	1.8V	Processor Host bus (WEIM bus) address bit 19.	A19 (uP_A3)	O	1.8V	Processor GPMC bus address bit 19.	See memory section for compatibility information.
96	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D25 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
97	A20 (uP_A19)	O	1.8V	Processor Host bus (WEIM bus) address bit 20.	A20 (uP_A19)	O	1.8V	Processor Host bus (WEIM bus) address bit 20.	A20 (uP_A4)	O	1.8V	Processor GPMC bus address bit 20.	See memory section for compatibility information.
98	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D26 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
99	A21 (uP_A20)	O	1.8V	Processor Host bus (WEIM bus) address bit 21.	A21 (uP_A20)	O	1.8V	Processor Host bus (WEIM bus) address bit 21.	A21 (uP_A5)	O	1.8V	Processor GPMC bus address bit 21.	See memory section for compatibility information.
100	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D27 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
101	A22 (uP_A21)	O	1.8V	Processor Host bus (WEIM bus) address bit 22.	A22 (uP_A21)	O	1.8V	Processor Host bus (WEIM bus) address bit 22.	A22 (uP_A6)	O	1.8V	Processor GPMC bus address bit 22.	See memory section for compatibility information.
102	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D28 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
103	A23 (uP_A22)	O	1.8V	Processor Host bus (WEIM bus) address bit 23.	A23 (uP_A22)	O	1.8V	Processor Host bus (WEIM bus) address bit 23.	A23 (uP_A7)	O	1.8V	Processor GPMC bus address bit 23.	See memory section for compatibility information.
104	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D29 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
105	A24 (uP_A23)	O	1.8V	Processor Host bus (WEIM bus) address bit 24.	A24 (uP_A23)	O	1.8V	Processor Host bus (WEIM bus) address bit 24.	A24 (uP_A8)	O	1.8V	Processor GPMC bus address bit 24.	See memory section for compatibility information.
106	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D30 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
107	A25 (uP_A24)	O	1.8V	Processor Host bus (WEIM bus) address bit 25.	A25 (uP_A24)	O	1.8V	Processor Host bus (WEIM bus) address bit 25.	A25 (uP_A9)	O	1.8V	Processor GPMC bus address bit 25.	See memory section for compatibility information.
108	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	D31 (RFU)	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
109	uP_nWAIT	I	1.8V	Active low. Processor Host bus (WIEM bus) ECB signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 2.2K pull-up.	uP_nWAIT	I	1.8V	Active low. Processor Host bus (WIEM bus) ECB signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 2.2K pull-up.	uP_nWAIT	I	1.8V	Active low. Processor bus GPMC_WAIT1 signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 1K pull-up.	Same on i.MX31, i.MX27 & OMAP35x
110	VREF_DATA_BUS	O	1.8V	Voltage reference output created on SOM-LV for the data bus.	VREF_DATA_BUS	O	1.8V	Voltage reference output created on SOM-LV for the data bus.	VREF_DATA_BUS (VIO_1V8)	O	1.8V	Voltage reference output created on SOM-LV for the data bus.	Voltage Reference on all modules. (See IRQ routing section for additional information.)
111	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
112	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
113	uP_nIRQD	I	2.7V (NVCC8)	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQD	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQD (CSI_D11)	I	1.8V	Active low. Software can use as a hardware interrupt.	This signals should only be driven low from the baseboard for compatiability for all three SOM-LV cards. (See IRQ routing section for additional information.)

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
114	CF_nCE (SLOW_nCS)	O	1.8V	Active low. Memory mode only CompactFlash chip enable. (see note 2)	SLOW_nCS	O	1.8V	Active low. Memory mode only CompactFlash chip enable. (see note 2)	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
115	uP_nIRQC	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQC	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQC	I	1.8V	Active low. Software can use as a hardware interrupt.	This signals should only be driven low from the baseboard for compatiability for all three SOM-LV cards. (See IRQ routing section for additional information.)
116	CF_nWE (uP_nEB0)	O	1.8V	Active low. Memory mode CompactFlash write enable signal. Indicates the current SOM-LV bus transaction is writing data to the CompactFlash card. (see note 2)	CF_nWE (uP_nEB0)	O	1.8V	Active low. Memory mode CompactFlash write enable signal. Indicates the current SOM-LV bus transaction is writing data to the CompactFlash card. (see note 2)	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
117	uP_nIRQB	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQB	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQB	I	1.8V	Active low. Software can use as a hardware interrupt.	This signals should only be driven low from the baseboard for compatiability for all three SOM-LV cards. See IRQ routing section for additional information.
118	CF_nOE (uP_nOE)	O	1.8V	Active low. Memory mode CompactFlash read enable signal. Indicates the current SOM-LV bus transaction is reading data from the CompactFlash card. (see note 2)	CF_nOE (uP_nOE)	O	1.8V	Active low. Memory mode CompactFlash read enable signal. Indicates the current SOM-LV bus transaction is reading data from the CompactFlash card. (see note 2)	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
119	uP_nIRQA	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQA	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.	uP_nIRQA	I	1.8V	Active low. Software can use as a hardware interrupt.	This signals should only be driven low from the baseboard for compatiability for all three SOM-LV cards. (See IRQ routing section for additional information.)
120	nCHRDY	I	3.3V	Active low. CompactFlash nCHRDY signal used to extend bus cycle to memory mode CompactFlash cards. This signal has a 470K pull-up to 3.3V. Note: baseboard should provide a pull up on nCHRDY to the voltage of the CompactFlash card being used. (see note 2)	nCHRDY	I	3.3V	Active low. CompactFlash nCHRDY signal used to extend bus cycle to memory mode CompactFlash cards. This signal has a 470K pull-up to 3.3V. Note: baseboard should provide a pull up on nCHRDY to the voltage of the CompactFlash card being used. (see note 2)	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
121	BUFF_nOE_DATA	O	1.8V	Active low. When this signal is low, external devices can drive data onto the WEIM bus.	BUFF_nOE_DATA	O	1.8V	Active low. When this signal is low, external devices can drive data onto the WEIM bus.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31 and i.MX27. RFU on OMAP35x.
122	uP_UARTC_CTS	I	1.8V	Clear To Send signal for CSPI3 UART.	uP_UARTC_CTS	I	1.8V	Clear To Send signal for CSPI3 UART.	uP_UARTC_CTS	I	1.8V	Clear To Send signal for UART2.	See UART interface section for compatiability information.
123	BUFF_DIR_DATA	O	1.8V	When low, external buffers should drive data from external devices towards the SOM-LV. (SOM-LV is reading) When high, external buffers should drive data from the SOM-LV towards external devices. (SOM-LV is writing).	BUFF_DIR_DATA	O	1.8V	When low, external buffers should drive data from external devices towards the SOM-LV. (SOM-LV is reading) When high, external buffers should drive data from the SOM-LV towards external devices. (SOM-LV is writing).	BUFF_DIR_DATA	O	1.8V	When low, external buffers should drive data from external devices towards the SOM-LV. (SOM-LV is reading) When high, external buffers should drive data from the SOM-LV towards external devices. (SOM-LV is writing).	Same on i.MX31, i.MX27, & OMAP35x.
124	uP_UARTC_RTS	O	1.8V	Ready To Send signal for CSPI3 UART.	uP_UARTC_RTS	O	1.8V	Ready To Send signal for CSPI3 UART.	uP_UARTC_RTS	O	1.8V	Ready To Send signal for UART2.	See UART interface section for compatiability information.
125	uP_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices.	uP_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices.	uP_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices.	Same on i.MX31, i.MX27, & OMAP35x.
126	uP_UARTC_RX	I	1.8V	Serial Data Receive signal for CSPI3 UART.	uP_UARTC_RX	I	1.8V	Serial Data Receive signal for CSPI3 UART.	uP_UARTC_RX	I	1.8V	Serial Data Receive signal for UART2.	See UART interface section for compatiability information.
127	uP_RnW	O	1.8V	Low indicates processor is writing. High indicates processor is reading.	uP_RnW	O	1.8V	Low indicates processor is writing. High indicates processor is reading.	uP_nWE	O	1.8V	Low indicates processor is writing. High indicates processor is reading.	Same on i.MX31, i.MX27, & OMAP35x.
128	uP_UARTC_TX	O	1.8V	Serial Data Transmit signal for CSPI3 UART.	uP_UARTC_TX	O	1.8V	Serial Data Transmit signal for CSPI3 UART.	uP_UARTC_TX	O	1.8V	Serial Data Transmit signal for UART2.	See UART interface section for compatiability information.
129	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
130	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
131	uP_BUS_CLK	O	1.8V	Processor WEIM bus clock. Frequency varies based on software setup.	uP_BUS_CLK	O	1.8V	Processor WEIM bus clock. Frequency varies based on software setup.	uP_BUS_CLK	O	1.8V	Processor bus clock. Frequency varies based on software setup.	Same on i.MX31, i.MX27, & OMAP35x.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
132	uP_UARTB_RX (uP_UARTB_RX/IRDA_RX)	I	2.7V	Serial Data Receive signal for UART2.	uP_UARTB_RX	I	1.8V	Serial Data Receive signal for UART2.	uP_UARTB_RX	I	1.8V	Serial Data Receive signal for UART3.	See UART interface section for compatiability information.
133	uP_DREQ0	I	1.8V	External DMA request 0	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_DREQ0	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ3 of the OMAP35x0.	See static memory interface section for compatiability information.
134	uP_UARTB_TX (uP_UARTB_TX/IRDA_TX)	O	2.7V	Serial Data Transmit signal for UART2.	uP_UARTB_TX	O	1.8V	Serial Data Transmit signal for UART2.	uP_UARTB_TX	O	1.8V	Serial Data Transmit signal for UART3.	See UART interface section for compatiability information.
135	uP_DREQ1	I	1.8V	External DMA request 1	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_DREQ1	I	1.8V	DMA Request signal for DMA4. Connected to SYS_nDMAREQ1 of the OMAP35x0.	See static memory interface section for compatiability information.
136	uP_UARTB_CTS	I	2.7V	Clear To Send signal for UART2.	uP_UARTB_CTS	I	1.8V	Clear To Send signal for UART2.	uP_UARTB_CTS	I	1.8V	Clear To Send signal for UART3.	See UART interface section for compatiability information.
137	nBLE0 (uP_nEB0)	O	1.8V	Processor WEIM bus Byte Lane Enable 0 bits [7:0]	uP_nBLE0 (uP_nEB0)	O	1.8V	Processor WEIM bus Byte Lane Enable 0 bits [7:0]	uP_nBE0	O	1.8V	Processor bus Byte Lane Enable 0 bits [7:0]	Same on i.MX31, i.MX27 and OMAP35x
138	uP_UARTB_RTS	O	2.7V	Ready To Send signal for UART2.	uP_UARTB_RTS	O	1.8V	Ready To Send signal for UART2.	uP_UARTB_RTS	O	1.8V	Ready To Send signal for UART3.	See UART interface section for compatiability information.
139	nBLE1 (uP_nEB1)	O	1.8V	Processor WEIM bus Byte Lane Enable 1 bits [15:8]	uP_nBLE1 (uP_nEB1)	O	1.8V	Processor WEIM bus Byte Lane Enable 1 bits [15:8]	uP_nBE1	O	1.8V	Processor bus Byte Lane Enable 1 bits [15:8]	Same on i.MX31, i.MX27, & OMAP35x.
140	uP_GPIO_4	I/O	2.7V	Processor GPIO available to user.	RFU	RFU	NA	Reserved for future use. Do not connect.	uP_GPO_4	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.0. This signal has a 4.7K pull-down resistor.	See GPIO section for compatibility information
141	uP_nCS_B_EXT	O	1.8V	External Chip select available for customer use.	uP_nCS_B_EXT	O	1.8V	External Chip select available for customer use.	uP_nCS_B_EXT	O	1.8V	External Chip select available for customer use.	See static memory interface section for compatiability information.
142	uP_GPIO_3	I/O	2.7V	Processor GPIO available to user.	uP_GPIO19	I/O	1.8V	Processor GPIO available to user.	uP_GPIO_3	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_111.	See GPIO section for compatibility information
143	uP_nCS_A_EXT	O	1.8V	External Chip select available for customer use.	uP_nCS_A_EXT	O	1.8V	External Chip select available for customer use.	uP_nCS_A_EXT	O	1.8V	External Chip select available for customer use.	See static memory interface section for compatiability information.
144	VREF_I2C1 (NVCC4)	O	2.8V	Reference voltage output for I2C DATA and CLK signals	VREF_I2C1	O	1.8V	Reference voltage output for I2C DATA and CLK signals	VREF_I2C2 (VIO_1V8)	O	1.8V	Reference voltage output for I2C DATA and CLK signals.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.
145	SLOW_nCS	O	1.8V	External Chip select available for customer use.	SLOW_nCS	O	1.8V	External Chip select available for customer use.	SLOW_nCS (uP_nCS_B_EXT)	O	1.8V	External Chip select available for customer use.	See static memory interface section for compatiability information.
146	I2C1_DATA	I/O	2.8V	I2C channel 1 data signal. This signal has a pull-up to the reference voltage onboard.	I2C1_DATA	I/O	1.8V	I2C channel 1 data signal. This signal has a pull-up to the reference voltage onboard.	uP_I2C2_SDA	I/O	1.8V	I2C channel 2 data signal. This signal has a 4.7K pull-up to the reference voltage onboard.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.
147	FAST_nCS	O	1.8V	External Chip select available for customer use.	FAST_nCS	O	1.8V	External Chip select available for customer use.	FAST_nCS (uP_nCS_A_EXT)	O	1.8V	External Chip select available for customer use.	See static memory interface section for compatiability information.
148	I2C1_CLK	I/O	2.8V	I2C channel 1 clock signal. This signal has a pull-up to the reference voltage onboard.	I2C1_CLK	I/O	1.8V	I2C channel 1 clock signal. This signal has a pull-up to the reference voltage onboard.	uP_I2C2_SCL	I/O	1.8V	I2C channel 2 clock signal. This signal has a 4.7K pull-up to the reference voltage onboard.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.
149	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
150	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
151	LCD_SPL	O	1.8V	LCD Start Pulse Left signal.	LCD_SPL	O	1.8V	LCD Start Pulse Left signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.
152	VREF_UARTA (2.7V_NVCC5/NVCC8)	O	2.7V	Voltage reference output for UART1 signals.	VREF_UARTA	O	1.8V	Voltage reference output for UART1 signals.	VREF_UARTA (VIO_1V8)	O	1.8V	Voltage reference output for UART1 signals.	See UART interface section for compatiability information.
153	LCD_DON	O	1.8V	LCD Data On signal.	LCD_DON	O	1.8V	LCD Data On signal.	LCD_DON	I/O	1.8V	LCD Data On signal.	See LCD interface section for compatiability information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
154	uP_UARTA_DSR	O	2.7V	Data Set Ready signal for UART1.	uP_UARTA_DSR	I	1.8V	Data Set Ready signal for UART1.	uP_UARTA_DSR	I	1.8V	Data Set Ready signal for UART1.	See UART interface section for compatiability information.
155	LCD_CLS	O	1.8V	LCD CLS signal.	LCD_CLS	O	1.8V	LCD CLS signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.
156	uP_UARTA_DTR	O	2.7V	Data Terminal Ready signal for UART1.	uP_UARTA_DTR	O	1.8V	Data Terminal Ready signal for UART1.	uP_UARTA_DTR	O	1.8V	Data Terminal Ready signal for UART1.	See UART interface section for compatiability information.
157	SPS (LCD_VSYRFU/SPS)	O	1.8V	LCD SPS signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.
158	uP_UARTA_RX	I	2.7V	Data Receive signal for UART1.	uP_UARTA_RX	I	1.8V	Data Receive signal for UART1.	uP_UARTA_RX	I	1.8V	Data Receive signal for UART1.	See UART interface section for compatiability information.
159	HRLP (LCD_HSYRFU/HRLP)	O	1.8V	LCD HRLP signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.
160	uP_UARTA_TX	O	2.7V	Data Transmit signal for UART1.	uP_UARTA_TX	O	1.8V	Data Transmit signal for UART1.	uP_UARTA_TX	O	1.8V	Data Transmit signal for UART1.	See UART interface section for compatiability information.
161	LCD_PANEL_PWR	O	1.8V	LCD Panel Power signal.	LCD_PANEL_PWR	O	1.8V	LCD Panel Power signal.	LCD_PANEL_PWR	O	1.8V	LCD Panel Power signal.	See LCD interface section for compatiability information.
162	uP_UARTA_CTS	I	2.7V	Clear To Send signal for UART1.	uP_UARTA_CTS	I	1.8V	Clear To Send signal for UART1.	uP_UARTA_CTS	I	1.8V	Clear To Send signal for UART1.	See UART interface section for compatiability information.
163	LCD_BACKLIGHT_PWR	O	1.8V	LCD Backlight Power signal. Active High.	LCD_BACKLIGHT_PWR	O	1.8V	LCD Backlight Power signal. Active High.	LCD_BACKLIGHT_PWR	O	1.8V	LCD Backlight Power signal. Active High.	See LCD interface section for compatiability information.
164	uP_UARTA_RTS	O	2.7V	Ready To Send signal for UART1.	uP_UARTA_RTS	O	1.8V	Ready To Send signal for UART1.	uP_UARTA_RTS	O	1.8V	Ready To Send signal for UART1.	See UART interface section for compatiability information.
165	HSYNC (LCD_HSYNC/HRLP)	O	1.8V	LCD Horizontal Sync signal.	LCD_HSYNC	O	1.8V	LCD Horizontal Sync signal.	LCD_HSYNC	O	1.8V	LCD Horizontal Sync signal.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
166	uP_GPIO_2	I/O	2.7V	Processor GPIO available to user.	uP_GPIO18	O	1.8V	Processor GPIO available to user.	uP_GPIO_2	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_31.	2.7v on i.MX31 and variable voltage on i.MX27
167	VSYNC (LCD_VSYNC/SPS)	O	1.8V	LCD Vertical Sync Signal.	LCD_VSYNC	O	1.8V	LCD Vertical Sync Signal.	LCD_VSYNC	O	1.8V	LCD Vertical Sync Signal.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
168	PWM0	O	2.8V	PWM output 0.	PWM0	O	1.8V	PWM output 0.	PWM0	O	1.8V	PWM output 0.	See PWR/RST/CLK/PWM control signal section
169	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
170	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
171	LCD_DCLK	O	1.8V	LCD Data Clock output.	LCD_DCLK	O	1.8V	LCD Data Clock output.	LCD_DCLK	O	1.8V	LCD Data Clock output.	See LCD interface section for compatiability information.
172	3.3V_uP_BATT	I	3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always on power source.	3.3V_uP_BATT	I	3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always on power source.	BACKUP_BATT	I	1.8V-3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always-on power source.	Same on i.MX31, i.MX27, & OMAP35x.
173	LCD_REV	O	1.8V	LCD Reverse signal.	LCD_REV	O	1.8V	LCD Reverse signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
174	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.	Same on i.MX31, i.MX27, & OMAP35x.
175	MDISP (LCD_PSAVE/MDISP)	O	1.8V	LCD MDISP signal.	MDISP (LCD_PSAVE/MDISP)	O	1.8V	LCD MDISP signal.	LCD_MDISP	O	1.8V	LCD MDISP signal.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
176	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.	Same on i.MX31, i.MX27, & OMAP35x.
177	PSAVE (LCD_PSAVE/MDISP)	O	1.8V	LCD Power Save signal.	PSAVE (LCD_PSAVE/MDISP)	O	1.8V	LCD Power Save signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See LCD interface section for compatiability information.
178	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	5V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used. Note: the default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.	5V	I	4.8V-7V	5V power input. Used by power management controller to charge external MAIN_BATTERY supply or can power the SOM-LV if the MAIN_BATTERY input is not used.	Same on i.MX31, i.MX27 and OMAP35x
179	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 and OMAP35x
180	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	Same on i.MX31, i.MX27 and OMAP35x
181	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 and OMAP35x
182	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	Same on i.MX31, i.MX27 and OMAP35x
183	VREF_LCD (1.8V_NVCC7)	O	1.8V	Voltage reference output for the LCD interface.	VREF_LCD	O	1.8V	Voltage reference output for the LCD interface.	LCD_VREF (VPLL2)	O	1.8V	Voltage reference output for the LCD interface.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
184	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	3.3V	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.	Same on i.MX31, i.MX27 and OMAP35x
185	R1 (LD13)	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.	R1 (LD13)	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.	R1 (LCD_D11)	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
186	TOUCH_LEFT	I	max 2.7V	Touch panel LEFT input signal.	TOUCH_LEFT	I	max 2.7V	Touch panel LEFT input signal.	TOUCH_LEFT	I	max 3.0V	Touch panel LEFT input signal.	See touch interface section for compatiability information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
187	R2 (LD14)	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.	R2 (LD14)	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.	R2 (LCD_D12)	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
188	TOUCH_RIGHT	I	max 2.7V	Touch panel RIGHT input signal.	TOUCH_RIGHT	I	max 2.7V	Touch panel RIGHT input signal.	TOUCH_RIGHT	I	max 3.0V	Touch panel RIGHT input signal.	See touch interface section for compatiability information.
189	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
190	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
191	R3 (LD15)	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.	R3 (LD15)	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.	R3 (LCD_D13)	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
192	TOUCH_BOTTOM	I	max 2.7V	Touch panel BOTTOM input signal.	TOUCH_BOTTOM	I	max 2.7V	Touch panel BOTTOM input signal.	TOUCH_BOTTOM	I	max 3.0V	Touch panel BOTTOM input signal.	See touch interface section for compatiability information.
193	R4 (LD16)	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.	R4 (LD16)	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.	R4 (LCD_D14)	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
194	TOUCH_TOP	I	max 2.7V	Touch panel TOP input signal.	TOUCH_TOP	I	max 2.7V	Touch panel TOP input signal.	TOUCH_TOP	I	max 3.0V	Touch panel TOP input signal.	See touch interface section for compatiability information.
195	R5 (LD17)	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.	R5 (LD17)	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.	R5 (LCD_D15)	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
196	A/D4	I	max 2.7V	Analog to digital converter input 4.	A/D4	I	max 2.7V	Analog to digital converter input 4.	A/D4	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN5.	Same on i.MX31, i.MX27 & OMAP35x
197	G0 (LD6)	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.	G0 (LD6)	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.	G0 (LCD_D5)	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
198	A/D3	I	max 2.7V	Analog to digital converter input 3.	A/D3	I	max 2.7V	Analog to digital converter input 3.	A/D3	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN4.	Same on i.MX31, i.MX27 & OMAP35x
199	G1 (LD7)	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.	G1 (LD7)	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.	G1 (LCD_D6)	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
200	A/D2	I	max 2.7V	Analog to digital converter input 2.	A/D2	I	max 2.7V	Analog to digital converter input 2.	A/D2	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN3.	Same on i.MX31, i.MX27, & OMAP35x.
201	G2 (LD8)	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.	G2 (LD8)	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.	G2 (LCD_D7)	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
202	A/D1	I	max 2.7V	Analog to digital converter input 1.	A/D1	I	max 2.7V	Analog to digital converter input 1.	A/D1	I	max 3.0V	Analog to digital converter input. Connected to Touch chip's AUX input.	Same on i.MX31 and i.MX27

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
203	G3 (LD9)	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.	G3 (LD9)	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.	G3 (LCD_D8)	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
204	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	Same on i.MX31, i.MX27, & OMAP35x.
205	G4 (LD10)	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.	G4 (LD10)	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.	G4 (LCD_D9)	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
206	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	Same on i.MX31, i.MX27, & OMAP35x.
207	G5 (LD11)	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.	G5 (LD11)	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.	G5 (LCD_D10)	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
208	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	Same on i.MX31, i.MX27, & OMAP35x.
209	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
210	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27, & OMAP35x.
211	B1 (LD1)	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.	B1 (LD1)	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.	B1 (LCD_D0)	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
212	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	Same on i.MX31, i.MX27 and OMAP35x
213	B2 (LD2)	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.	B2 (LD2)	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.	B2 (LCD_D1)	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
214	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	MAIN_BATTERY	I	max 4.5V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.	Same on i.MX31, i.MX27 and OMAP35x
215	B3 (LD3)	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.	B3 (LD3)	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.	B3 (LCD_D2)	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
216	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user.	uP_GPIO17	I/O	1.8V	Processor GPIO available to user.	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_11.	Same on i.MX31, i.MX27 & OMAP35x. (See GPIO section.)
217	B4 (LD4)	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.	B4 (LD4)	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.	B4 (LCD_D3)	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
218	uP_GPIO_0	I/O	1.8V	Processor GPIO available to user.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_GPIO_0	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_133.	Same on i.MX31, i.MX27 & OMAP35x. (See GPIO section.)
219	B5 (LD5)	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.	B5 (LD5)	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.	B5 (LCD_D4)	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.	Same on i.MX31, i.MX27 and OMAP35x when operating in 16 bpp 5:6:5 color mode. See LCD interface section for additional compatiability information.
220	uP_SPI_CS1	O	1.8V	SPI interface chip select 1 output.	uP_CSPI1_SS1	O	1.8V	SPI interface chip select 1 output.	uP_SPI_CS1	O	1.8V	McSPI3 interface chip select 1 output.	Same on all SOM-LV modules. See SPI interface section for more information.
221	ONE_WIRE (BATT_LINE)	I/O	2.7V	Bi-directional battery management ONEWIRE interface.	ONE_WIRE (uP_RTCK/1WIRE)	I/O	1.8V	Bi-directional battery management ONEWIRE interface.	ONE_WIRE (BATT_LINE)	I/O	1.8V	Bi-directional battery management ONEWIRE interface. This signal has a 4.7K pull-up to VIO_1V8.	One wire on the i.MX31, i.MX27 and the OMAP35x. Note on i.MX27 this pin is muxed with the JTAG RTCK signal.
222	uP_SPI_CS0	O	1.8V	SPI interface chip select 0 output.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_SPI_CS0	O	1.8V	McSPI3 interface chip select 0 output.	Same on all SOM-LV modules. See SPI interface section for more information.
223	uP_SW_nRESET	I	2.7V	Active low. Input to CPU. Software can setup GPIO as an interrupt. Signal has a 10K pull-up to 2.7V.	uP_SW_nRESET	I	1.8V	Active low. Input to CPU. Software can setup GPIO as an interrupt. Signal has a 10K pull-up to 2.7V.	uP_SW_nRESET (SYS_nRESWARM)	I	1.8V	Active low. Input to CPU and power management controller. This signal has a 4.7K pull-up to VIO_1V8.	See pwr/clk/rst section for more information
224	uP_SPI_RX	I	1.8V	SPI interface receive input.	uP_CSPI1_MISO	I	1.8V	SPI interface receive input.	uP_SPI_SOMI	I	1.8V	McSPI3 interface receive input.	Same on all SOM-LV modules. See SPI interface section for more information.
225	RESET_nOUT (PMIC_nRESET)	O	1.8V	Active low. Reset output from the power management controller that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The RESET_nOUT signal has an onboard 4.7K pull-up to 1.8V_NVCC1 rail.	RESET_nOUT (PMIC_nRESET)	O	1.8V	Active low. Reset output from the power management controller that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The RESET_nOUT signal has an onboard 4.7K pull‑up to 1.8V_NVCC1 rail.	RESET_nOUT (SYS_nRESWARM)	O	1.8V	Active low. Reset output from the CPU that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The SYS_nRESWARM signal has a 4.7K pull‑up to VIO_1V8.	See pwr/clk/rst section for more information
226	uP_SPI_TX	O	1.8V	SPI interface transmit output.	uP_CSPI1_MOSI	O	1.8V	SPI interface transmit output.	uP_SPI_SIMO	O	1.8V	McSPI3 interface transmit output.	Same on all SOM-LV modules. See SPI interface section for more information.
227	MSTR_nRST	I	1.8V	Active low. External reset input to the SOM-LV. This signal should be used to reset all devices on the SOM-LV including the CPU. The MSTR_nRST signal has an onboard 4.7K pull-up to 1.8V_NVCC1 rail.	MSTR_nRST	I	1.8V	Active low. External reset input to the SOM-LV. This signal should be used to reset all devices on the SOM-LV including the CPU. The MSTR_nRST signal has an onboard 4.7K pull-up to 1.8V_NVCC1 rail.	MSTR_nRST	I	1.8V	Active low. External reset input to the SOM-LV. This signal should be used to reset all devices on the SOM-LV including the CPU.	See pwr/clk/rst section for more information
228	uP_SPI_SCLK	I/O	1.8V	SPI Serial clock signal.	uP_CSPI1_SCLK	O	1.8V	SPI Serial clock signal.	uP_SPI_SCLK	O	1.8V	McSPI3 serial clock signal.	Same on all SOM-LV modules. See SPI interface section for more information.
229	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
230	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
231	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	VMMC2	O	VMMC2	VMMC2 LDO output from TPS65950 available to user.	See SD/MMC insterface section for more information.

	i.MX31 J1 Connector				i.MX27 J1 Connector				OMAP35x J1 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
232	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	TOUCH_nIRQ	O	1.8V	If touch chip is populated, this signal is the active low touch interrupt; do not connect. If touch chip is not populated, this signal is a proccesor GPIO available to user; connected to GPIO_153.	RFU on i.MX31 and the i.MX27. GPIO_153 on OMAP35x if touch is not populated.
233	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3424
234	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3425
235	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3426
236	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3427
237	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3428
238	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP3429
239	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
240	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
1	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
2	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
3	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
4	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
5	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
6	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
7	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	WLAN_nIRQ	O	1.8V	If Ethernet chip is populated, this signal is the active low Ethernet interrupt; do not connect. If Ethernet chip is not populated, this signal is a proccesor GPIO available to user; connected to GPIO_152.	Same on i.MX31 and i.MX27 (RFU), The OMAP35x used it as WAN_nIRQ or extra GPIO if the wired Ethernet is not populated.
8	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
9	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	ICT_TEST_MODE	I	1.8V	Used for test only. Do not connect.	Same on i.MX31 and i.MX27 (RFU), Reserved for future use on the OMAP35x.
10	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_CLKOUT2_26MHz	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_186.	Same on i.MX31 and i.MX27 (RFU), Extra GPIO on the OMAP35x.
11	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
12	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
13	PCC_POWER_nEN	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface.	PCC_POWER_nEN	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface.	PCC_POWER_nEN (SIM0_VEN)	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface.	See pcmcia/cf section for compatibility information.
14	PCC_nOE (uP_nLBA)	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal.	PCC_nOE (uP_nLBA)	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal.	PCC_nOE (uP_nOE)	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal.	See static memory and pcmcia/cf section for compatibility information.
15	PCC_PCMCIA_nEN	O	1.8V	Active low. Enables CompactFlash address and control signals.	PCC_PCMCIA_nEN	O	1.8V	Active low. Enables CompactFlash address andcontrol signals.	PCC_PCMCIA_nEN (SIM0_VEN)	O	1.8V	Active low. Enables CompactFlash control signals.	See pcmcia/cf section for compatibility information.
16	uP_PCC_RDYA	I	2.8V	Active high. CompactFlash/PC Card Ready signal.	uP_PCC_RDYA/ATA_CS0	I	1.8V	Active high. CompactFlash/PC Card Ready signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
17	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	HSUSB1_D7	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_17.	Same on i.MX31 and i.MX27. GPIO on OMAP35x.
18	uP_PCC_nWAIT	I	2.8V	Active low. CompactFlash/PC Card Wait signal.	uP_PCC_nWAIT/ATA_CS1	I	1.8V	Active low. CompactFlash/PC Card Wait signal.	uP_PCC_nWAIT	I	1.8V	Active low. CompactFlash/PC Card Wait signal.	See pcmcia/cf section for compatibility information.
19	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	HSUSB1_D6	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_20.	Same on i.MX31 and i.MX27. GPIO on OMAP35x.
20	uP_PCC_BVD2	I	2.8V	CompactFlash/PC Card Battery Voltage Detect 2 input.	uP_PCC_BVD2_DMACK	I	1.8V	CompactFlash/PC Card Battery Voltage Detect 2 input.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
21	ATA_D15 (I2C1_DATA)	I/O	2.8V	ATA interface Data bit 15. This interface is multiplexed with other onboard interfaces.	uP_ATA_D15	I/O	1.8V	ATA interface Data bit 15. This interface is multiplexed with other onboard interfaces.	HSUSB1_D5	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_19.	ATA_D15 on both the i.MX31 and i.MX27. It is also muxed with an I2C bus on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_19 on the OMAP35x.
22	uP_PCC_BVD1	I	2.8V	CompactFlash/PC Card Battery Voltage Detect 1 input.	uP_PCC_BVD1/ATA_DMARQ	I	1.8V	CompactFlash/PC Card Battery Voltage Detect 1 input.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
23	ATA_D14 (I2C1_CLK)	I/O	2.8V	ATA interface Data bit 14. This interface is multiplexed with other onboard interfaces.	uP_ATA_D14	I/O	1.8V	ATA interface Data bit 14. This interface is multiplexed with other onboard interfaces.	HSUSB1_D4	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_18.	ATA_D14 on both the i.MX31 and i.MX27. It is also muxed with an I2C bus on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_18 on the OMAP35x.
24	uP_PCC_CD2	I	2.8V	CompactFlash/ PC Card Detect 2 input.	uP_PCC_CD2	I	1.8V	CompactFlash/ PC Card Detect 2 input.	uP_PCC_CD2 (uP_PCC_CD1)	I	1.8V	CompactFlash/ PC Card Detect 2 input.	See pcmcia/cf section for compatibility information.
25	ATA_D13 (CSI_PCLK)	I/O	2.8V	ATA interface Data bit 13. This interface is multiplexed with other onboard interfaces.	uP_ATA_D13	I/O	1.8V	ATA interface Data bit 13. This interface is multiplexed with other onboard interfaces.	HSUSB1_D3	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_21.	ATA_D13 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_21 on the OMAP35x
26	uP_PCC_CD1	I	2.8V	CompactFlash/ PC Card Detect 1 input.	uP_PCC_CD1	I	1.8V	CompactFlash/ PC Card Detect 1 input.	uP_PCC_CD1	I	1.8V	CompactFlash/ PC Card Detect 1 input.	See pcmcia/cf section for compatibility information.
27	ATA_D12 (CSI_HSYRFU)	I/O	2.8V	ATA interface Data bit 12. This interface is multiplexed with other onboard interfaces.	uP_ATA_D12	I/O	1.8V	ATA interface Data bit 12. This interface is multiplexed with other onboard interfaces.	HSUSB1_D2	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_16.	ATA_D12 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_16 on the OMAP35x.
28	uP_PCC_VS1	I	2.8V	CompactFlash/ PC Card Voltage Sense 1 input.	uP_PCC_VS1/ATA_DA1	I	1.8V	CompactFlash/ PC Card Voltage Sense 1 input.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
29	ATA_D11 (CSI_VSYRFU)	I/O	2.8V	ATA interface Data bit 11. This interface is multiplexed with other onboard interfaces.	uP_ATA_D11	I/O	1.8V	ATA interface Data bit 11. This interface is multiplexed with other onboard interfaces.	HSUSB1_D1	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_15.	ATA_D11 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_15 on the OMAP35x.
30	uP_PCC_VS2	I	2.8V	CompactFlash/PC Card Voltage Sense 2 input.	uP_PCC_VS2/ATA_DA0	I	1.8V	CompactFlash/PC Card Voltage Sense 2 input.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
31	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
32	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
33	ATA_D10 (CSI_MCLK)	I/O	2.8V	ATA interface Data bit 10. This interface is multiplexed with other onboard interfaces.	uP_ATA_D10	I/O	1.8V	ATA interface Data bit 10. This interface is multiplexed with other onboard interfaces.	HSUSB1_CLK	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_13.	ATA_D10 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_13 on the OMAP35x.
34	uP_PCC_RESET	O	2.8V	CompactFlash/PC Card Reset output.	PCC_RESET (uP_PCC_RESET/ATA_nRESET)	I	1.8V	CompactFlash/PC Card Reset output.	uP_PCC_RESET	O	1.8V	CompactFlash/PC Card Reset output.	See pcmcia/cf section for compatibility information.
35	ATA_D9 (CSI_D15)	I/O	2.8V	ATA interface Data bit 9. This interface is multiplexed with other onboard interfaces.	uP_ATA_D9	I/O	1.8V	ATA interface Data bit 9. This interface is multiplexed with other onboard interfaces.	HSUSB1_NXT	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_23.	ATA_D9 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_23 on the OMAP35x.
36	PCC_nDRV (uP_PC_POE)	O	2.8V	CompactFlash/PC Card buffer Drive output.	PCC_nDRV (uP_PC_POE/ATA_BUFFER_EN)	O	1.8V	CompactFlash/PC Card buffer Drive output.	PCC_nDRV (uP_nCS3)	O	1.8V	CompactFlash/PC Card buffer Drive output.	See pcmcia/cf section for compatibility information.
37	ATA_D8 (CSI_D14)	I/O	2.8V	ATA interface Data bit 8. This interface is multiplexed with other onboard interfaces.	uP_ATA_D8	I/O	1.8V	ATA interface Data bit 8. This interface is multiplexed with other onboard interfaces.	HSUSB1_STP	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_12.	ATA_D8 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_12 on the OMAP35x.
38	PCC_nIOWR (uP_nOE)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.	PCC_nIOWR (uP_nOE)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.	PCC_nIOWR (VIO_1V8)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.	See pcmcia/cf section for compatibility information.
39	ATA_D7 (CSI_D13)	I/O	2.8V	ATA interface Data bit 7. This interface is multiplexed with other onboard interfaces.	uP_ATA_D7	I/O	1.8V	ATA interface Data bit 7. This interface is multiplexed with other onboard interfaces.	HSUSB1_DIR	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_22.	ATA_D7 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_22 on the OMAP35x.
40	PCC_nWE (uP_RnW)	O	1.8V	Active low. CompactFlash/PC Card Write Enable output.	PCC_nWE (uP_RnW)	O	1.8V	Active low. CompactFlash/PC Card Write Enable output.	PCC_nWE (uP_nWE)	O	1.8V	Active low. CompactFlash/PC Card Write Enable output.	See pcmcia/cf section for compatibility information.
41	ATA_D6 (CSI_D12)	I/O	2.8V	ATA interface Data bit 6. This interface is multiplexed with other onboard interfaces.	uP_ATA_D6	I/O	1.8V	ATA interface Data bit 6. This interface is multiplexed with other onboard interfaces.	HSUSB1_D0	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_14.	ATA_D6 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_14 on the OMAP35x.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
42	PCC_nIORD (uP_nEB1)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.	PCC_nIORD (uP_nEB1)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.	PCC_nIORD (VIO_1V8)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.	See pcmcia/cf section for compatibility information.
43	ATA_D5 (CSI_D11)	I/O	2.8V	ATA interface Data bit 5. This interface is multiplexed with other onboard interfaces.	uP_ATA_D5	I/O	1.8V	ATA interface Data bit 5. This interface is multiplexed with other onboard interfaces.	HSUSB2_STP	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_25. If R71 not populated, reserved for future use; do not connect.	ATA_D5 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_25 if R71 is populated on OMAP35x.
44	PCC_REG (uP_nEB0)	O	1.8V	CompactFlash/PC Card Reg access output.	PCC_REG (uP_nEB0)	O	1.8V	CompactFlash/PC Card Reg access output.	PCC_REG (VIO_1V8)	O	1.8V	CompactFlash/PC Card Reg access output.	See pcmcia/cf section for compatibility information.
45	ATA_D4 (CSI_D10)	I/O	2.8V	ATA interface Data bit 4. This interface is multiplexed with other onboard interfaces.	uP_ATA_D4	I/O	1.8V	ATA interface Data bit 4. This interface is multiplexed with other onboard interfaces.	HSUSB2_D1	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_29. If R71 not populated, reserved for future use; do not connect.	ATA_D4 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_29 if R71 is populated on the OMAP35x.
46	uP_PCC_nIOIS16	I	2.8V	CompactFlash/PC Card nIOIS16 input.	uP_PCC_nIOIS16/ATA_INTRQ	I	1.8V	CompactFlash/PC Card nIOIS16 input.	RFU	I/O	NA	Reserved for future use. Do not connect.	See pcmcia/cf section for compatibility information.
47	ATA_D3 (CSI_D9)	I/O	2.8V	ATA interface Data bit 3. This interface is multiplexed with other onboard interfaces.	uP_ATA_D3	I/O	1.8V	ATA interface Data bit 3. This interface is multiplexed with other onboard interfaces.	HSUSB2_D0	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_28. If R71 not populated, reserved for future use; do not connect.	ATA_D3 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO28 if R71 is populated on the OMAP35x.
48	PCC_nCE1A (uP_MSDBA1)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.	PCC_nCE1A (uP_MSDBA1)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.	PCC_nCE1A (uP_nCS3)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.	See pcmcia/cf section for compatibility information.
49	ATA_D2 (CSI_D8)	I/O	2.8V	ATA interface Data bit 2. This interface is multiplexed with other onboard interfaces.	uP_ATA_D2	I/O	1.8V	ATA interface Data bit 2. This interface is multiplexed with other onboard interfaces.	MCSPI_CS1 (HSUSB2_D3)	I/O	1.8V	If R71 populated, processor GPIO available to user; connected to GPIO_182. If R71 not populated, reserved for future use; do not connect.	ATA_D2 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_182 if R71 is populated on the OMAP35x.
50	PCC_nCE2A (uP_MSDBA0)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A.	PCC_nCE2A (uP_MSDBA0)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A.	PCC_nCE2A (uP_nCS3)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A.	See pcmcia/cf section for compatibility information.
51	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
52	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
53	ATA_D1 (CSI_D7)	I/O	2.8V	ATA interface Data bit 1. This interface is multiplexed with other onboard interfaces.	uP_ATA_D1	I/O	1.8V	ATA interface Data bit 1. This interface is multiplexed with other onboard interfaces.	MCSPI2_CS0 (HSUSB2_D6)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_181. If R70 not populated, reserved for future use; do not connect.	ATA_D1 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_181 if R70 if R70 is populated on the OMAP35x.
54	VREF_PCMCIA (NVCC3)	O	2.8V	CompactFlash/PC Card Voltage reference output.	VREF_PCMCIA	O	1.8V	CompactFlash/PC Card Voltage reference output.	VREF_PCMCIA (VIO_1V8)	O	1.8V	CompactFlash/PC Card Voltage reference output.	See pcmcia/cf section for compatibility information.
55	ATA_D0 (CSI_D6)	I/O	2.8V	ATA interface Data bit 0. This interface is multiplexed with other onboard interfaces.	uP_ATA_D0	I/O	1.8V	ATA interface Data bit 0. This interface is multiplexed with other onboard interfaces.	MCSPI2_SOMI (HSUSB2_D5)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_180. If R70 not populated, reserved for future use; do not connect.	ATA_D0 on both the i.MX31 and i.MX27. It is also muxed with the CSI interface on i.MX31. Voltage is dependant on VCAM on the i.MX31 and is also variable on the i.MX27. See ATA section for more information. Connected to GPIO_180 if R70 is populated on the OMAP35x.
56	MFP (uP_A25)	O	1.8V	Processor WEIM bus Address bit 25 output.	uP_A25	O	1.8V	Processor WEIM bus Address bit 25 output.	A26 (uP_A10)	O	1.8V	Processor GPMC bus address bit 26. (see note 1)	See static memory for compatibility information.
57	IORDY (PWMO)	O	2.8V	ATA interface IORDY output. This interface is multiplexed with other onboard interfaces.	IORDY (uP_PC_RnW/ATA_IORDY)	O	1.8V	ATA interface IORDY output. This interface is multiplexed with other onboard interfaces.	MCSPI2_SIMO (HSUSB2_D4)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_179. If R70 not populated, reserved for future use; do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. GPIO_179 if R70 is populated on the OMAP35x.
58	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
59	ATA_RESET	O	2.8V	ATA interface Reset output. This interface is multiplexed with other onboard interfaces.	ATA_RESET (uP_PCC_RESET/ATA_nRESET)	I	1.8V	ATA interface Reset output. This interface is multiplexed with other onboard interfaces.	MCSPI2_CLK (HSUSB2_D7)	I/O	1.8V	If R70 populated, processor GPIO available to user; connected to GPIO_178. If R70 not populated, reserved for future use; do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. GPIO_178 if R70 is populated on the OMAP35x.
60	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
61	ATA_DMACK	O	2.8V	ATA interface DMA Acknowledge output. This interface is multiplexed with other onboard interfaces.	ATA_DMACK (uP_PCC_BVD2_DMACK)	I	1.8V	ATA interface DMA Acknowledge output. Thisinterface is multiplexed with other onboard interfaces.	RFU	I/O	NA	Reserved for future use. Do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. RFU on the OMAP35x.
62	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
63	ATA_DIOW (CSI_D3)	O	2.8V	ATA interface Data I/O Write output. This interface is multiplexed with other onboard interfaces.	ATA_DIOW (uP_PCC_CD2/ATA_DIOW)	I	1.8V	ATA interface Data I/O Write output. This interface is multiplexed with other onboard interfaces.	RFU	I/O	NA	Reserved for future use. Do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. RFU on the OMAP35x.
64	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
65	ATA_DIOR (CSI_D2)	O	2.8V	ATA interface Data I/O Read output. This interface is multiplexed with other onboard interfaces.	ATA_DIOR (uP_PCC_CD1/ATA_DIOR)	I	1.8V	ATA interface Data I/O Read output. This interface is multiplexed with other onboard interfaces.	RFU	I/O	NA	Reserved for future use. Do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. RFU on the OMAP35x.
66	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
67	ATA_CS1 (CSI_D1)	O	2.8V	ATA interface Chip Select 1 output. This interface is multiplexed with other onboard interfaces.	ATA_CS1 (uP_PCC_nWAIT/ATA_CS1)	I	1.8V	ATA interface Chip Select 1 output. This interface is multiplexed with other onboard interfaces.	RFU	I/O	NA	Reserved for future use. Do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. RFU on the OMAP35x.
68	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
69	ATA_CS0 (CSI_D0)	O	2.8V	ATA interface Chip Select 0 output. This interface is multiplexed with other onboard interfaces.	ATA_CS0 (uP_PCC_RDYA/ATA_CS0)	I	1.8V	ATA interface Chip Select 0 output. This interface is multiplexed with other onboard interfaces.	RFU	I/O	NA	Reserved for future use. Do not connect.	Muxed with CSI and ATA on the i.MX31. Required for ATA support on the i.MX27. RFU on the OMAP35x.
70	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
71	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
72	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
73	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
74	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
75	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	VIBRA_M	O	MAIN_BATTERY	Vibrator M signal for H-Bridge operation.	See pwr/clk/rst section for more information
76	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
77	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	VIBRA_P	O	MAIN_BATTERY	Vibrator P signal for H-Bridge operation.	See pwr/clk/rst section for more information
78	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
79	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	RFU	NA	Reserved for future use. Do not connect.	START_ADC	I	1.8V	This signal is the TPS65950 ADC conversion request.	Same on i.MX31 and i.MX27, see ADC section for OMAP35x
80	VREF_MMC/SD1 (NVCC3)	O	2.8V	MMC/SD1 interface voltage reference output.	VREF_MMC/SD2 (NVDD15)	O	2.8V	MMC/SD2 interface voltage reference output.	VREF_MMC/SD1 (VMMC1)	O	1.8V (VMMC1)	MMC/SD1 interface voltage reference output.	See MMC/SD Card interface section for compatiability information.
81	CDCOUT	O	2.7V	MC13783 CDCOUT signal.	CDCOUT	O	2.7V	MC13783 CDCOUT signal.	RF_LED0	O	3.0V	Wireless LAN LED0 signal.	Same on i.MX31 and i.MX27, connected to the Atlas chip on both SOMs, Wireless LAN LED0 on the OMAP35x
82	SD1_DATA3	I/O	2.8V	MMC/SD1 Data 3 signal.	SD2_DATA3	I/O	2.8V	MMC/SD2 Data 3 signal.	SD1_DATA3	I/O	1.8V (VMMC1)	MMC/SD2 Data 3 signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.
83	uP_CSPI1_RDY	I	1.8V_NVCC10	CSPI1 Ready signal.	uP_CSPI1_RDY	I	1.8V	CSPI1 Ready signal.	RF_LED1	O	3.0V	Wireless LAN LED1 signal.	Same on i.MX31 and i.MX27 SOM-LV modules. See SPI interface section for more information. Wireless LAN LED1 on OMAP35x.
84	SD1_DATA2	I/O	2.8V	MMC/SD1 Data 2 signal.	SD2_DATA2	I/O	2.8V	MMC/SD2 Data 2 signal.	SD1_DATA2	I/O	1.8V (VMMC1)	MMC/SD2 Data 2 signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.
85	uP_CSPI2_RDY	I	2.7V_NVCC5,8	CSPI2 Ready signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_nWP	O	1.8V	Processor GPMC write protect signal.	SPI2_RDY not useful on i.MX31, RFU on i.MX27, uP_nWP on OMAP35x
86	SD1_DATA1	I/O	2.8V	MMC/SD1 Data 1 signal.	SD2_DATA1	I/O	2.8V	MMC/SD2 Data 1 signal.	SD1_DATA1	I/O	1.8V (VMMC1)	MMC/SD2 Data 1 signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
87	uP_CSPI2_SS2	O	2.7V_NVCC5,8	CSPI2 Slave Select 2 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_nADV_ALE	O	1.8V	Processor GPMC address valid or address latch enable signal.	Alternate function I2C3_SDA, CSI_FLASH_STROBE alternate function on i.MX31, RFU on i.MX27, and uP_nADV_ALE on OMAP35x
88	SD1_DATA0	I/O	2.8V	MMC/SD1 Data 0 signal.	SD2_DATA0	I/O	2.8V	MMC/SD2 Data 0 signal.	SD1_DATA0	I/O	1.8V (VMMC1)	MMC/SD2 Data 0 signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.
89	uP_CSPI2_SS1	O	2.7V_NVCC5,8	CSPI2 Slave Select 1 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFID_EN	O	VMMC2	RFID device enable.	Alternate function CSPI3_SS1 and CSPI_SS3 on the i.MX31, RFU on i.MX27, and RFID_EN on OMAP35x
90	SD1_CMD	I/O	2.8V	MMC/SD1 Command signal.	SD2_CMD	I/O	2.8V	MMC/SD2 Command signal.	SD1_CMD	I/O	1.8V (VMMC1)	MMC/SD2 Command signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.
91	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
92	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
93	uP_SPI_SCLK	I/O	??	(ATA_DA2)	PC_PWRON/ATA_DA2	I	1.8V	ATA_DA2	KEY_COL7	I/O	1.8V	Keypad Column 7 signal.	ATA_DA2 on both i.MX31 and i.MX27. Also a keypad column on i.MX31 and the OMAP35x. See ATA and the keypad section for more information.
94	SD1_CLK	I/O	2.8V	MMC/SD1 Clock signal.	SD2_CLK	I/O	2.8V	MMC/SD2 Clock signal.	SD1_CLK	O	1.8V (VMMC1)	MMC/SD2 Clock signal. This signal has a 10K pull-up to VMMC1.	See MMC/SD Card interface section for compatiability information.
95	KEY_COL6	I/O	2.7V_NVCC6,9	Keypad Column 6 signal. (ATA_DA1)	uP_PCC_VS1/ATA_DA1	I	1.8V	ATA_DA1	KEY_COL6	I/O	1.8V	Keypad Column 6 signal.	ATA_DA1 on both i.MX31 and i.MX27. Also a keypad column on i.MX31 and the OMAP35x. See ATA and the keypad section for more information.
96	VREF_I2C2 (2.7V_NVCC5/NVCC8)	O	2.7V_NVCC5,8	I2C channel 2 voltage reference output.	VREF_I2C2	O	1.8V	I2C channel 2 voltage reference output.	VREF_I2C3 (VIO_1V8)	O	1.8V	I2C channel 3 voltage reference output.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.
97	KEY_COL5	I/O	2.7V_NVCC6,9	Keypad Column 5 signal. (ATA_DA0)	uP_PCC_VS2/ATA_DA0	I	1.8V	ATA_DA0	KEY_COL5	I/O	1.8V	Keypad Column 5 signal.	ATA_DA0 on both i.MX31 and i.MX27. Also a keypad column on i.MX31 and on the OMAP35x. See ATA and keypad section for more information.
98	I2C2_CLK	I/O	2.7V_NVCC5,8	I2C channel 2 Clock signal.	I2C2_CLK	I/O	1.8V	I2C channel 2 Clock signal.	uP_I2C3_SCL	I/O	1.8V	I2C channel 3 Clock signal.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.
99	KEY_COL4	I/O	2.7V_NVCC6,9	Keypad Column 4 signal. (ATA_DMARQ)	uP_PCC_BVD1/ATA_DMARQ	I	1.8V	ATA_DMARQ	KEY_COL4	I/O	1.8V	Keypad Column 4 signal.	ATA_DMARQ on both i.MX31 and i.MX27. Also a keypad column on i.MX31 and the OMAP35x. See ATA and keypad section for more information.
100	I2C2_DATA	I/O	2.7V_NVCC5,8	I2C channel 2 Data signal.	I2C2_DATA	I/O	1.8V	I2C channel 2 Data signal.	uP_I2C3_SDA	I/O	1.8V	I2C channel 3 Data signal.	Variable voltage on the SOM-LVs. See I2C interface section for additional compatiability information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
101	KEY_COL3	I/O	2.7V_NVC C6,9	Keypad Column 3 signal.	KEY_COL3	I/O	1.8V	Keypad Column 3 signal.	KEY_COL3	I/O	1.8V	Keypad Column 3 signal.	See keyapd section for more information.
102	uP_TEST1	I	2.7V_NVC C6,9	Test 1 signal tied to CPU SJC_MOD signal to enable / disable JTAG access. This signal has a 4.7k ohm pull down.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	JTAG enable on i.MX31, RFU on i.MX27 & OMAP35x
103	KEY_COL2	I/O	2.7V_NVC C6,9	Keypad Column 2 signal.	KEY_COL2	I/O	1.8V	Keypad Column 2 signal.	KEY_COL2	I/O	1.8V	Keypad Column 2 signal.	See keyapd section for more information.
104	uP_TEST2	I	2.7V_NVC C5,8	Test 2 signal tied to CPU CE_CONTROL signal. Refer to i.MX31 documentation for more information on this signal. This signal has a 1k ohm pull down.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	CE_CONTROL signal on i.MX31, RFU on i.MX27 & OMAP35x
105	KEY_COL1	I/O	2.7V_NVC C6,9	Keypad Column 1 signal.	KEY_COL1	I/O	1.8V	Keypad Column 1 signal.	KEY_COL1	I/O	1.8V	Keypad Column 1 signal.	See keyapd section for more information.
106	uP_DE	I	2.7V_NVC C6,9	CPU JTAG Debug Request signal. This signal has a 4.7k ohm pull up.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Jtag debug request signal on i.MX31, RFU on i.MX27 & OMAP35x
107	KEY_COL0	I/O	2.7V_NVC C6,9	Keypad Column 0 signal.	KEY_COL0	I/O	1.8V	Keypad Column 0 signal.	KEY_COL0	I/O	1.8V	Keypad Column 0 signal.	See keyapd section for more information.
108	uP_TMS	I	2.7V_NVC C6,9	CPU JTAG Test Mode Signal. This signal has a 4.7k ohm pull up.	uP_TMS	I	1.8V	CPU JTAG Test Mode Signal. This signal has a 4.7k ohm pull up.	uP_TMS	I	1.8V	CPU JTAG Test Mode Signal.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
109	KEY_ROW7	I/O	2.7V_NVC C6,9	Keypad Row 7 signal.	uP_PC_POE/ATA_ BUFFER_EN	O	1.8V	ATA_BUFFER_EN	KEY_ROW7	I/O	1.8V	Keypad Row 7 signal.	ATA_BUFFER_EN on both i.MX31 and i.MX27. Also a keypad column on i.MX31 and keypad row on the OMAP35x. See ATA and keypad section for more information.
110	uP_TCK	I	2.7V_NVC C6,9	CPU JTAG Test Clock input signal.	uP_TCK	I	1.8V	CPU JTAG Test Clock input signal.	uP_TCK	I	1.8V	CPU JTAG Test Clock input signal.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
111	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
112	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
113	KEY_ROW6	I/O	2.7V_NVC C6,9	Keypad Row 6 signal.	uP_PCC_nIOIS16/A TA_INTRQ	I	1.8V	ATA_INTRQ	KEY_ROW6	I/O	1.8V	Keypad Row 6 signal.	ATA_INTRQ on both i.MX31 and i.MX27. Keypad column on i.MX31. Keypad row on the OMAP35x. See ATA and keypad section for more information.
114	uP_TDO	O	2.7V_NVC C6,9	CPU JTAG Test Data Output from the CPU to the JTAG device.	uP_TDO	O	1.8V	CPU JTAG Test Data Output from the CPU to the JTAG device.	uP_TDO	O	1.8V	CPU JTAG Test Data Output from the CPU to the JTAG device.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
115	uP_GPIO_7	I/O	2.7V_NVC C6,9	Keypad Row 5 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	KEY_ROW5	I/O	1.8V	Keypad Row 5 signal.	See keyapd section for more information.
116	uP_nTRST	I	2.7V_NVC C6,9	CPU JTAG Test Reset input. This signal has a 4.7k ohm pull up.	uP_nTRST	I	1.8V	CPU JTAG Test Reset input. This signal has a 4.7k ohm pull up.	uP_nTRST	I	1.8V	CPU JTAG Test Reset input.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
117	uP_GPIO_6	I/O	2.7V_NVC C6,9	Keypad Row 4 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	KEY_ROW4	I/O	1.8V	Keypad Row 4 signal.	See keyapd section for more information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
118	uP_TDI	I	2.7V_NVCC6,9	CPU JTAG Test Data Input to the CPU from the JTAG device. This signal has a 4.7k ohm pull-up.	uP_TDI	I	1.8V	CPU JTAG Test Data Input to the CPU from theJTAG device. This signal has a 4.7k ohm pull-up.	uP_TDI	I	1.8V	CPU JTAG Test Data Input to the CPU from the JTAG device.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
119	KEY_ROW3	I/O	2.7V_NVCC6,9	Keypad Row 3 signal.	KEY_ROW3	I/O	1.8V	Keypad Row 3 signal.	KEY_ROW3	I/O	1.8V	Keypad Row 3 signal.	See keyapd section for more information.
120	uP_RTCK	O	2.7V_NVCC6,9	CPU JTAG Return Test Clock signal.	uP_RTCK/1WIRE	O	1.8V	CPU JTAG Return Test Clock signal.	uP_RTCK	O	1.8V	CPU JTAG Return Test Clock signal.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
121	KEY_ROW2	I/O	2.7V_NVCC6,9	Keypad Row 2 signal.	KEY_ROW2	I/O	1.8V	Keypad Row 2 signal.	KEY_ROW2	I/O	1.8V	Keypad Row 2 signal.	See keyapd section for more information.
122	VREF_JTAG (2.7V_NVCC6/NVCC9)	O	2.7V_NVCC6,9	CPU JTAG reference voltage output.	VREF_JTAG	O	1.8V	CPU JTAG reference voltage output.	VREF_JTAG (VIO_1V8)	O	1.8V	CPU JTAG reference voltage output.	Same on i.MX31, i.MX27 & OMAP35x. See the BDM/JTAG Interface section for recommended connector interface.
123	KEY_ROW1	I/O	2.7V_NVCC6,9	Keypad Row 1 signal.	KEY_ROW1	I/O	1.8V	Keypad Row 1 signal.	KEY_ROW1	I/O	1.8V	Keypad Row 1 signal.	See keyapd section for more information.
124	SIM0_VEN	O	2.7V_NVCC6,9	SIM Card 0 Voltage Enable signal.	SD1_DATA3	I/O	2.8V	MMC/SD1 Data 3 signal.	SIM0_VEN	O	1.8V (VSIM)	Smart card voltage enable.	See the SIM and MMC sections for compatiablitiy information.
125	KEY_ROW0	I/O	2.7V_NVCC6,9	Keypad Row 0 signal.	KEY_ROW0	I/O	1.8V	Keypad Row 0 signal.	KEY_ROW0	I/O	1.8V	Keypad Row 0 signal.	Variable voltage on i.MX31 and on i.MX27
126	SIM0_nDETECT	O	2.7V_NVCC6,9	SIM Card 0 Voltage Dectect signal.	SD1_DATA2	I/O	2.8V	MMC/SD1 Data 2 signal.	SIM0_nDETECT	I	1.8V (VSIM)	Smart card detect.	See the SIM and MMC sections for compatiablitiy information.
127	CSI_HSYRFU	I/O	2.8V, NVCC4	Camera Sensor Interface Horizontal Sync signal.	CSI_HSYRFU	I/O	1.8V	Camera Sensor Interface Horizontal Sync signal.	CSI_HSYRFU	I/O	1.8V	Camera Sensor Interface Horizontal Sync signal.	See camera interface section for compatiability information.
128	SIM0_CLK	I/O	2.7V_NVCC6,9	SIM Card 0 Clock signal.	SD1_DATA1	I/O	2.8V	MMC/SD1 Data 1 signal.	SIM0_CLK	O	1.8V (VSIM)	Smart card clock output.	See the SIM and MMC sections for compatiablitiy information.
129	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
130	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
131	CSI_VSYRFU	I/O	2.8V	Camera Sensor Interface Vertical Sync signal.	CSI_VSYRFU	I/O	1.8V	Camera Sensor Interface Vertical Sync signal.	CSI_VSYRFU	I/O	1.8V	Camera Sensor Interface Vertical Sync signal.	See camera interface section for compatiability information.
132	SIM0_IO/TX	I/O	2.7V_NVCC6,9	SIM Card 0 I/O Transmit signal.	SD1_DATA0	I/O	2.8V	MMC/SD1 Data 0 signal.	SIM0_IO/TX	I/O	1.8V (VSIM)	Smart card data inout signal.	See the SIM and MMC sections for compatiablitiy information.
133	CSI_D0	I/O	2.8V	Camera Sensor Interface Data bit 0.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D0	I	1.8V	Camera Sensor Interface Data bit 0.	See camera interface section for compatiability information.
134	SIM0_RX	I/O	2.7V_NVCC6,9	SIM Card 0 Receive signal.	SD1_CMD	I/O	2.8V	MMC/SD1 Data CMD signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	See the SIM and MMC sections for compatiablitiy information.
135	CSI_D1	I/O	2.8V	Camera Sensor Interface Data bit 1.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D1	I	1.8V	Camera Sensor Interface Data bit 1.	See camera interface section for compatiability information.
136	SIM0_nRESET	I/O	2.7V_NVCC6,9	SIM Card 0 Reset signal. Active low.	SD1_CLK	I/O	2.8V	MMC/SD1 Data CLK signal.	SIM0_nRESET	O	1.8V (VSIM)	Smart card reset.	See the SIM and MMC sections for compatiablitiy information.
137	CSI_D2	I/O	2.8V	Camera Sensor Interface Data bit 2.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D2	I	1.8V	Camera Sensor Interface Data bit 2.	See camera interface section for compatiability information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
138	SIM0_VCC	O	SIM0_VCC	SIM Card 0 Voltage Output signal.	VREF_MMC/SD1 (VMMC1)	I/O	?	?	VREF_SIM (VSIM)	O	1.8V (VSIM)	Smart card reference voltage.	See the SIM and MMC sections for compatiablitiy information.
139	CSI_D3	I/O	2.8V	Camera Sensor Interface Data bit 3.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D3	I	1.8V	Camera Sensor Interface Data bit 3.	See camera interface section for compatiability information.
140	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
141	CSI_D4	I/O	2.8V	Camera Sensor Interface Data bit 4.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D4	I	1.8V	Camera Sensor Interface Data bit 4.	See camera interface section for compatiability information.
142	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	ICT_JTAG_TDO	O	1.8V	Used for test only. Do not connect.	RFU on i.MX31 and i.MX27, ICT on the OMAP35x
143	CSI_D5	I/O	2.8V	Camera Sensor Interface Data bit 5.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D5	I	1.8V	Camera Sensor Interface Data bit 5.	See camera interface section for compatiability information.
144	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	ICT_JTAG_TMS	I	1.8V	Used for test only. Do not connect.	RFU on i.MX31 and i.MX27, ICT on the OMAP35x
145	CSI_D6	I/O	2.8V	Camera Sensor Interface Data bit 6.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D6	I	1.8V	Camera Sensor Interface Data bit 6.	See camera interface section for compatiability information.
146	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	ICT_JTAG_TDI	I	1.8V	Used for test only. Do not connect.	RFU on i.MX31 and i.MX27, ICT on the OMAP35x
147	CSI_D7	I/O	2.8V	Camera Sensor Interface Data bit 7.	RFU	I/O	NA	Reserved for future use. Do not connect.	CSI_D7	I	1.8V	Camera Sensor Interface Data bit 7.	See camera interface section for compatiability information.
148	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	ICT_JTAG_CLK	I	1.8V	Used for test only. Do not connect.	RFU on i.MX31 and i.MX27, ICT on the OMAP35x
149	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
150	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
151	CSI_D8	I/O	2.8V	Camera Sensor Interface Data bit 8.	CSI_D0	I/O	1.8V	Camera Sensor Interface Data bit 0.	CSI_D8	I	1.8V	Camera Sensor Interface Data bit 8.	See camera interface section for compatiability information.
152	PCC_POWER_nEN	O	1.8V_NVC7	When asserted low this signal should turn power on to CompactFlash/ CF Card slot.	PCC_POWER_nEN	O	1.8V	When asserted low this signal should turn power on to CompactFlash/ CF Card slot.	uP_GPIO_2	I/O	1.8V	Processor GPIO available to user. Connected to JTAG_EMU1/GPIO_31.	PCC_POWER_EN on i.MX31 and i.MX27, uP_GPIO_2 on the OMAP35x
153	CSI_D9	I/O	2.8V	Camera Sensor Interface Data bit 9.	CSI_D1	I/O	1.8V	Camera Sensor Interface Data bit 1.	CSI_D9	I	1.8V	Camera Sensor Interface Data bit 9.	See camera interface section for compatiability information.
154	LCD_LCS0	O	1.8V_NVC7	LCD Chip Select 0 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user. Connected to JTAG_EMU0/GPIO_11.	LCD CS0 on i.MX31, RFU on i.MX27. i.MX27 does not support LCD CS signal, uP_GPIO_1/JTAG_EMU0 on OMAP35x
155	CSI_D10	I/O	2.8V	Camera Sensor Interface Data bit 10.	CSI_D2	I/O	1.8V	Camera Sensor Interface Data bit 2.	CSI_D10	I	1.8V	Camera Sensor Interface Data bit 10.	See camera interface section for compatiability information.
156	LCD_CONTRAST	O	1.8V_NVC7	LCD Contrast signal.	MFP (LCD_CONTRAST)	O	1.8V	LCD Contrast signal.	BT_PCM_DX	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.17.	LCD_CONTRAST on i.MX31 and i.MX27, GPIO signal on OMAP35x
157	CSI_D11	I/O	2.8V	Camera Sensor Interface Data bit 11.	CSI_D3	I/O	1.8V	Camera Sensor Interface Data bit 3.	CSI_D11	I	1.8V	Camera Sensor Interface Data bit 11.	See camera interface section for compatiability information.
158	LCD_WRITE	O	1.8V_NVC7	LCD Write Enable signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	BT_PCM_DR	I/O	1.8V	TPS65950 GPIO available to user. Connected to TPS65950 GPIO.16.	LCD WR on i.MX31, RFU on i.MX27. i.MX27 does not support WR signal, GPIO signal on OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Migration Notes
159	CSI_D12	I/O	2.8V	Camera Sensor Interface Data bit 12.	CSI_D4	I/O	1.8V	Camera Sensor Interface Data bit 4.	RFU	I/O	NA	Reserved for future use. Do not connect.	See camera interface section for compatiability information.
160	LCD_READ	O	1.8V_NVCC7	LCD Read Enable signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	BT_PCM_VFS	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_143.	LCD RD on i.MX31, RFU on i.MX27. i.MX27 does not support RD signal, PCM connection on OMAP35x
161	CSI_D13	I/O	2.8V	Camera Sensor Interface Data bit 13.	CSI_D5	I/O	1.8V	Camera Sensor Interface Data bit 5.	RFU	I/O	NA	Reserved for future use. Do not connect.	See camera interface section for compatiability information.
162	LCD_VSYRFU0	O	1.8V_NVCC7	LCD Vertical Sync 0 signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	PCM_DX	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_141.	LCD VSYRFU0 on i.MX31, RFU on i.MX27. i.MX27 does not support VSYRFU0 signal, PCM connection on OMAP35x
163	CSI_D14	I/O	2.8V	Camera Sensor Interface Data bit 14.	CSI_D6	I/O	1.8V	Camera Sensor Interface Data bit 6.	RFU	I/O	NA	Reserved for future use. Do not connect.	See camera interface section for compatiability information.
164	LCD_PAR_RS	O	1.8V_NVCC7	LCD Parallel RS signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	PCM_DR	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_140.	LCD Parallel RS on i.MX31, RFU on i.MX27. i.MX27 does not support Parallel RS signal, PCM connection on OMAP35x
165	CSI_D15	I/O	2.8V	Camera Sensor Interface Data bit 15.	CSI_D7	I/O	1.8V	Camera Sensor Interface Data bit 7.	RFU	I/O	NA	Reserved for future use. Do not connect.	See camera interface section for compatiability information.
166	LCD_SER_RS	O	1.8V_NVCC7	LCD Serial RS signal.	RFU	I/O	NA	Reserved for future use. Do not connect.	BT_PCM_CLK	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_142.	LCD Serial RS on i.MX31, RFU on i.MX27. i.MX27 does not support Serial RS signal, PCM connection on OMAP35x
167	CSI_MCLK	I/O	2.8V	Camera Sensor Interface Master Clock signal.	CSI_MCLK	I/O	1.8V	Camera Sensor Interface Master Clock signal.	CSI_MCLK	O	1.8V	Camera Sensor Interface Master Clock signal.	See camera interface section for compatiability information.
168	EXT_BOOT_nSELECT	I	1.8V	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then FLASH_nCS = uP_nCS0; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS0. This defaults to the onboard flash if left unconnected (pulled to 1.8V through a 10K resistor).	EXT_BOOT_nSELECT	I	1.8V	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then FLASH_nCS = uP_nCS0; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS0. This defaults to the onboard flash if left unconnected (pulled to 1.8Vthrough a 10K resistor).	EXT_BOOT_nSELECT	I	1.8V	Boot select signal (0 = external boot device, 1 = onboard NOR flash, if populated). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then NOR_nCS = uP_nCS2; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS2. This defaults to the onboard flash if left unconnected (pulled to 1.8V through a 10K resistor). Note: R57 must be populated to boot from NOR or an external device.	Same on i.MX31, i.MX27 & OMAP35x
169	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
170	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
171	CSI_PCLK	I/O	2.8V	Camera Sensor Interface Pixel Clock signal.	CSI_PCLK	I/O	1.8V	Camera Sensor Interface Pixel Clock signal.	CSI_PCLK	I	1.8V	Camera Sensor Interface Pixel Clock signal.	See camera interface section for compatiability information.
172	BOOT_nCS	O	1.8V	Active Low. This signal is the chip select for boot ROM in area 0 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. See memory map for addressing details.	BOOT_nCS	O	1.8V	Active Low. This signal is the chip select for boot ROM in area 0 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. See memory map for addressing details.	BOOT_nCS	O	1.8V	Active Low. This signal is connected to uP_nCS2 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. This signal has a 4.7K pull-up to VIO_1V8.	Same on i.MX31, i.MX27 & OMAP35x
173	VREF_CSI (NVCC4)	O	2.8V	Camera Sensor Interface reference voltage output.	VREF_CSI (VCAM)	O	1.8V	Camera Sensor Interface reference voltage output.	VREF_CSI (VPLL2)	O	1.8V (VPLL2)	Camera Sensor Interface reference voltage output.	See camera interface section for compatiability information.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
174	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D23	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	Same on i.MX31 and i.MX27, LCD signal on the OMAP35x
175	LEDB3	O	max 5.5V	LED Drive Blue bit 3.	LEDB3	O	max 5.5V	LED Drive Blue bit 3.	VAUX3	O	VAUX3	Auxilary power supply available to user.	LED Drive on i.MX31 and i.MX27, VAUX3 on OMAP35x
176	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D22	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	Same on i.MX31 and i.MX27, LCD signal on the OMAP35x
177	LEDG3	O	max 5.5V	LED Drive Green bit 3.	LEDG3	O	max 5.5V	LED Drive Green bit 3.	TWL_CLK256FS	I/O	1.8V	Processor GPIO available to user. Connected to GPIO_160.	LED Drive on i.MX31 and i.MX27, TWL_CLK256FS/GPIO on OMAP35x
178	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D21	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
179	LEDR3	O	max 5.5V	LED Drive Red bit 3.	LEDR3	O	max 5.5V	LED Drive Red bit 3.	RFU	I/O	NA	Reserved for future use. Do not connect.	LED Drive on i.MX31 and i.MX27, RFU on OMAP35x
180	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D20	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
181	LEDB2	O	max 5.5V	LED Drive Blue bit 2.	LEDB2	O	max 5.5V	LED Drive Blue bit 2.	CSI1_DY1	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX1.	LED Drive on i.MX31 and i.MX27, Camera Serial on OMAP34x, RFU on the OMAP35x
182	B0 (LD0)	O	1.8V_NVCC7	LCD B0 data bit.	LD0	O	1.8V	LCD B0 data bit.	LCD_D19	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
183	LEDG2	O	max 5.5V	LED Drive Green bit 2.	LEDG2	O	max 5.5V	LED Drive Green bit 2.	CSI1_DX1	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY1.	LED Drive on i.MX31 and i.MX27, Camera Serial on OMAP34x, RFU on the OMAP35x
184	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D18	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
185	LEDR2	O	max 5.5V	LED Drive Red bit 2.	LEDR2	O	max 5.5V	LED Drive Red bit 2.	CSI1_DY0	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DX0.	LED Drive on i.MX31 and i.MX27, Camera Serial on OMAP34x, RFU on the OMAP35x
186	RFU	RFU	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	LCD_D17	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
187	LEDB1	O	max 5.5V	LED Drive Blue bit 1.	LEDB1	O	max 5.5V	LED Drive Blue bit 1.	CSI1_DX0	I	VAUX4	Camera Serial Interface 2 data/clock input. Route as differential pair with CSI1_DY0.	LED Drive on i.MX31 and i.MX27, Camera Serial on OMAP34x, RFU on the OMAP35x
188	R0 (LD12)	O	1.8V_NVCC7	RLCD R0 data bit.	LD12	O	1.8V	RLCD R0 data bit.	LCD_D16	O	1.8V	LCD data bit when operating in 24 bpp color mode. Please reference the OMAP35xx TRM for LCD bus mapping.	See LCD interface section for compatiability information.
189	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 and OMAP35x
190	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 and OMAP35x
191	LEDG1	O	max 5.5V	LED Drive Green bit 1.	LEDG1	O	max 5.5V	LED Drive Green bit 1.	MCSPI1_SOMI	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_173.	LED Drive on i.MX31 and i.MX27, GPIO on OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
192	HSPGF	O	2.7V	See MC13783 data sheet for more information.	HSPGF	O	2.7V	See MC13783 data sheet for more information.	TV_OUT2	O	VDAC	Analog TV_OUT2.	Same on i.MX31 and i.MX27. Signal used with Headset Connection with Phantom Ground. TV_ouput signal for the OMAP35x. See TV Display Interface section for more information.
193	LEDR1	O	max 5.5V	LED Drive Red bit 1.	LEDR1	O	max 5.5V	LED Drive Red bit 1.	T2_REGEN	O	MAIN_BATTERY	Active high. External LDO enable signal generated by the TPS65950.	LED Drive on i.MX31 and i.MX27, External LDO enable on OMAP35x
194	HSPGS	O	2.7V	See MC13783 data sheet for more information.	HSPGS	O	2.7V	See MC13783 data sheet for more information.	TV_OUT1	O	VDAC	Analog TV_OUT1.	Same on i.MX31 and i.MX27. Signal used with Headset Connection with Phantom Ground. TV_ouput signal for the OMAP35x. See TV Display Interface section for more information.
195	LEDKP	O	max 5.5V	LED Key Press signal.	LEDKP	O	max 5.5V	LED Key Press signal.	ADCIN6	I	max 2.7V	Analog to digital converter input. Connected to TPS65950 ADCIN6.	LED Drive on i.MX31 and i.MX27, ADC on OMAP35x
196	LSPL	O	2.7V	See MC13783 data sheet for more information.	LSPL	O	2.7V	See MC13783 data sheet for more information.	ADCIN2	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN2.	Same on i.MX31 and i.MX27, ADC on OMAP35x
197	LEDAD2	O	max 5.5V	LED AD2 signal.	LEDAD2	O	max 5.5V	LED AD2 signal.	WLAN_MMC3_DATA3	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_139.	LED Drive on i.MX31 and i.MX27, 802.11 or GPIO on OMAP35x
198	SPM	O	2.7V	See MC13783 data sheet for more information.	SPM	O	2.7V	See MC13783 data sheet for more information.	ADCIN1	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN1.	Same on i.MX31 and i.MX27, ADC on OMAP35x
199	LEDAD1	O	max 5.5V	LED AD1 signal.	LEDAD1	O	max 5.5V	LED AD1 signal.	WLAN_MMC3_DATA2	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_138.	LED Drive on i.MX31 and i.MX27. GPIO on OMAP35x.
200	SPP	O	2.7V	See MC13783 data sheet for more information.	SPP	O	2.7V	See MC13783 data sheet for more information.	ADCIN0	I	1.5V	Analog to digital converter input. Connected to TPS65950 ADCIN0.	Same on i.MX31 and i.MX27, ADC on OMAP35x
201	LEDMD4	O	max 5.5V	LED MD4 signal.	LEDMD4	O	max 5.5V	LED MD4 signal.	WLAN_MMC3_DATA1	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_137.	LED Drive on i.MX31 and i.MX27. GPIO on OMAP35x.
202	LSPM	O	2.7V	See MC13783 data sheet for more information.	LSPM	O	2.7V	See MC13783 data sheet for more information.	IHF_RIGHT_M	O	MAIN_BATTERY	Hands-free speaker output right (M).	Same on i.MX31 and i.MX27, Audio signal on the OMAP35x
203	LEDMD3	O	max 5.5V	LED MD3 signal.	LEDMD3	O	max 5.5V	LED MD3 signal.	WLAN_MMC3_DATA0	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_136.	LED Drive on i.MX31 and i.MX27. GPIO on OMAP35x.
204	LSPP	O	2.7V	See MC13783 data sheet for more information.	LSPP	O	2.7V	See MC13783 data sheet for more information.	IHF_RIGHT_P	O	MAIN_BATTERY	Hands-free speaker output right (P).	Same on i.MX31 and i.MX27, Audio signal on the OMAP35x
205	LEDMD2	O	max 5.5V	LED MD2 signal.	LEDMD2	O	max 5.5V	LED MD2 signal.	WLAN_MMC3_CMD	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_175.	LED Drive on i.MX31 and i.MX27. GPIO on OMAP35x.
206	A/D6	I	max 2.7V	Analog to Digital Converter 6 input.	A/D6	I	max 2.7V	Analog to Digital Converter 6 input.	IHF_LEFT_M	O	MAIN_BATTERY	Hands-free speaker output left (M).	Same on i.MX31 and i.MX27, Audio signal on the OMAP35x
207	LEDMD1	O	max 5.5V	LED MD1 signal.	LEDMD1	O	max 5.5V	LED MD1 signal.	WLAN_MMC3_CLK	I/O	1.8V	If 802.11 populated, do not connect. If 802.11 not populated, Processor GPIO available to user; connected to GPIO_176.	LED Drive on i.MX31 and i.MX27, Wireless 802.11 or GPIO on OMAP35x
208	A/D5	I	max 2.7V	Analog to Digital Converter 5 input.	A/D5	I	max 2.7V	Analog to Digital Converter 5 input.	IHF_LEFT_P	O	MAIN_BATTERY	Hands-free speaker output right (P).	Same on i.MX31 and i.MX27, Audio signal on the OMAP35x
209	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
210	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
211	HSLDET	I	2.7V	Head Set Left detect signal.	HSLDET	I	2.7V	Head Set Left detect signal.	MCSPI1_CLK	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_171.	Same on i.MX31 and i.MX27, BT or GPIO signal on the OMAP35x
212	MIC_IN	I	2.7V	Microphone input.	MIC_IN	I	2.7V	Microphone input.	MIC_IN	I	max 2.7V	Microphone input.	Same on i.MX31, i.MX27 & OMAP35x
213	PC_PWRON	O	2.8V	PC Card power applied input.	PC_PWRON/ATA_DA2	O	1.8V	PC Card power applied input.	MCSPI1_SIMO	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_172.	Same on i.MX31 and i.MX27, BT or GPIO signal on the OMAP35x
214	MIC_INR	I	2.7V	Right side microphone input.	MIC_INR	I	2.7V	Right side microphone input.	MIC_SUB_M	I	MICBIAS2	Main microphone right input (M).	Same on i.MX31, i.MX27. MIC_SUB_M on the OMAP35x
215	ATLAS_GPO3	O	2.7V	MC13783 general purpose output.	ATLAS_GPO3	O	2.7V	MC13783 general purpose output.	MCSPI1_CS0	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_174.	Same on i.MX31 and i.MX27, BT or GPIO signal on the OMAP35x
216	MIC_INL	I	2.7V	Left side microphone input.	MIC_INL	I	2.7V	Left side microphone input.	MIC_SUB_P	I	MICBIAS2	Main microphone right input (P).	Same on i.MX31, i.MX27. MIC_SUB_P on the OMAP35x
217	ATLAS_GPO2	O	2.7V	MC13783 general purpose output.	ATLAS_GPO2	O	2.7V	MC13783 general purpose output.	MICBIAS2	O	MICBIAS2	Analog microphone bias 2.	Same on i.MX31, i.MX27. MICBIAS2 on the OMAP35x
218	HP_OUTL	O	2.7V	Head Phone Out Left channel.	HP_OUTL	O	2.7V	Head Phone Out Left channel.	MIC_MAIN_M	I	MICBIAS1	Main microphone left input (M).	Same on i.MX31, i.MX27. MIC_MAIN_M on the OMAP35x
219	ATLAS_GPO1	O	2.7V	MC13783 general purpose output.	ATLAS_GPO1	O	2.7V	MC13783 general purpose output.	MICBIAS1	O	MICBIAS1	Analog microphone bias 1.	Same on i.MX31, i.MX27. MICBIAS1 on the OMAP35x
220	HP_OUTR	O	2.7V	Head Phone Out Right channel.	HP_OUTR	O	2.7V	Head Phone Out Right channel.	MIC_MAIN_P	I	MICBIAS1	Main microphone left input (P).	Same on i.MX31, i.MX27. MIC_MAIN_P on the OMAP35x
221	I2S/AC97_CLK (uP_SCK4)	I/O	2.7V_NVC C5,8	I2S Serial Clock signal.	I2S/AC97_CLK (uP_SCK1)	O	1.8V	I2S Serial Clock signal.	MCBSP2_CLKX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_117.	See I2S/AC97/PCM interface section for compatiability information.
222	CODEC_INL	I	2.7V	CODEC Left channel Line In.	CODEC_INL	I	2.7V	CODEC Left channel Line In.	CODEC_INL	I	max 2.7V	Auxiliary left channel line in.	Same on i.MX31, i.MX27 & OMAP35x
223	I2S/AC97_FRAME (uP_SFS4)	O	2.7V_NVC C5,8	I2S Framing signal.	I2S/AC97_FRAME (uP_SFS1)	O	1.8V	I2S Framing signal.	MCBSP2_FSX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_116.	See I2S/AC97/PCM interface section for compatiability information.
224	CODEC_INR	I	2.7V	CODEC Right channel Line In.	CODEC_INR	I	2.7V	CODEC Right channel Line In.	CODEC_INR	I	max 2.7V	Auxiliary right channel line in.	Same on i.MX31, i.MX27 & OMAP35x
225	I2S/AC97_RX (uP_SRXD4)	I	2.7V_NVC C5,8	I2S data Receive signal.	I2S/AC97_RX (uP_SRXD1)	I	1.8V	I2S data Receive signal.	MCBSP2_DR	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_118.	See I2S/AC97/PCM interface section for compatiability information.
226	CODEC_OUTL	O	2.7V	CODEC Left channel Line Out.	CODEC_OUTL	O	2.7V	CODEC Left channel Line Out.	CODEC_OUTL	O	max 2.7V	Left channel line out.	Same on i.MX31, i.MX27 & OMAP35x
227	I2S/AC97_TX (uP_STXD4)	O	2.7V_NVC C5,8	I2S data Transmit signal.	I2S/AC97_TX (uP_STXD1)	O	1.8V	I2S data Transmit signal.	MCBSP2_DX	I/O	1.8V	If using audio, do not connect. If not using audio, Processor GPIO available to user; connected to GPIO_119.	See I2S/AC97/PCM interface section for compatiability information.
228	CODEC_OUTR	O	2.7V	CODEC Right Channel Line Out.	CODEC_OUTR	O	2.7V	CODEC Right Channel Line Out.	CODEC_OUTR	O	max 2.7V	Right channel line out.	Same on i.MX31, i.MX27 & OMAP35x
229	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
230	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	DGND	I	GND	Ground. Connect to digital ground.	Same on i.MX31, i.MX27 & OMAP35x
231	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	T2_CLKREQ	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31 and i.MX27, Clock request signal on OMAP35x
232	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	BT_IRQ	I/O	1.8V	If Bluetooth populated, do not connect. If Bluetooth not populated, Processor GPIO available to user; connected to GPIO_157.	Same on i.MX31 and i.MX27, BT or GPIO signal on the OMAP35x
233	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	uP_CLKOUT1_26MHz	O	1.8V	Processor SYS_CLKOUT1.	Same on i.MX31 and i.MX27. Processor clock output signal on OMAP35x.

	i.MX31 J2 Connector				i.MX27 J2 Connector				OMAP35x J2 Connector				Migration Notes
Pin	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	Signal Name	I/O	Voltage	Description	
234	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	TWL_32K_CLK_OUT	O	1.8V	TPS65950 32kHz clock output.	Same on i.MX31 and i.MX27. TPS65950 clock output signal on OMAP35x.
235	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
236	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
237	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
238	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
239	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x
240	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	RFU	I/O	NA	Reserved for future use. Do not connect.	Same on i.MX31, i.MX27 & OMAP35x