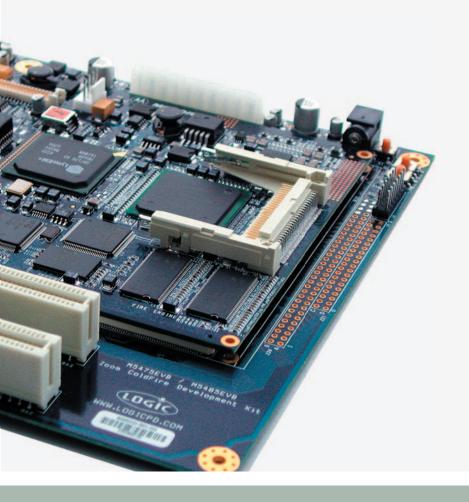
Zoom™

ColdFire Development Kit

MCF547x/8x Fire Engine LogicLoader™ User's Manual Addendum







REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
Α	Bruce Rovner	Release	BDR	08/20/2004
В	Aaron Stewart, Sam Siciliano, Bruce Rovner	Updated to accommodate LoLo 2.0.4; Updated diagrams; Updated Supported Hardware Peripherals table	HAR	10/21/2005

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1 MCF547x/8x Memory Map Diagrams

1.1 MCF547x/8x Hardware Memory Map

The MCF547x/8x Fire Engine is designed to accommodate SDRAM and flash memory of different sizes. LogicLoader™ (LoLo) will always detect the correct amount of installed SDRAM and configure it into a flat memory space. The MMU is not used by LoLo to map or control access to memory. LoLo will detect the correct amount of installed boot flash and user flash, and will always place the base of the respective flash areas as shown in the diagram below. The region where the flash is located will be configured by LoLo to accommodate the largest possible size that can be installed. Use the 'info cpu' command to view how LogicLoader has setup the different resources in memory.

1.2 Physical Hardware Memory Map

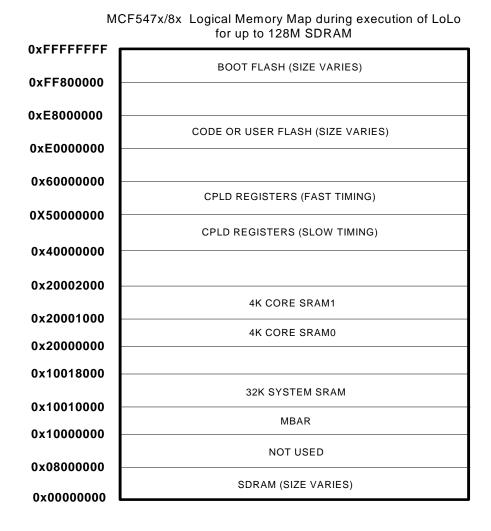


Figure 1.1: MCF547x/8x Hardware Memory Map

1.3 Location of dBUG and LogicLoader in Flash Memory

The Zoom™ ColdFire Development Kits come with both dBUG and LoLo programmed into the Fire Engine's resident boot flash array (see figures 1.2 and 1.3 below).

Please note that Fire Engines included with Zoom ColdFire Development Kits ship with dBUG starting at block zero of boot flash, while production Fire Engines will ship with LoLo at block zero of boot flash.

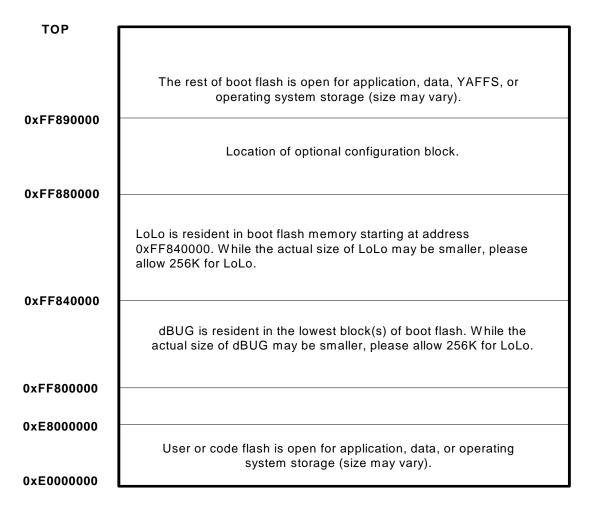


Figure 1.2: Flash Memory Layout With dBUG (as shipped with ColdFire Development Kits)

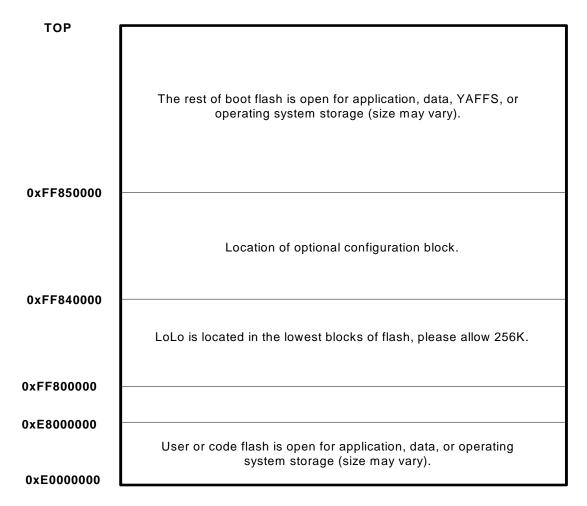


Figure 1.3: Flash Memory Layout Without dBUG (as shipped with Production Fire Engines)

1.4 LogicLoader and dBug Location in RAM

Both Freescale's dBUG bootloader and Logic's LoLo bootloader execute out of SDRAM. The diagrams below depict run time location of LogicLoader. You can use the dBUG command 'mmap' to find out information about its execution environment. Refer to the *CDK QuickStart Guide* for the steps required to start LoLo from the dBUG prompt.

Run-time location of LogicLoader:

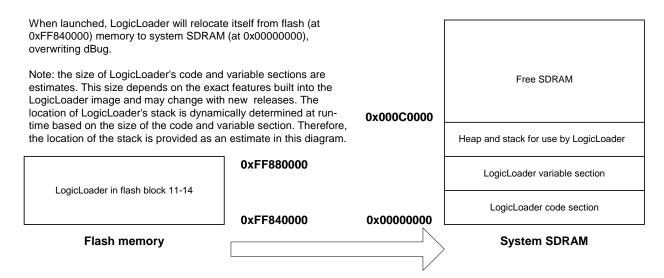


Figure 1.4: LogicLoader RAM Execution Environment (with dBUG in Flash)

Run-time location of LogicLoader:

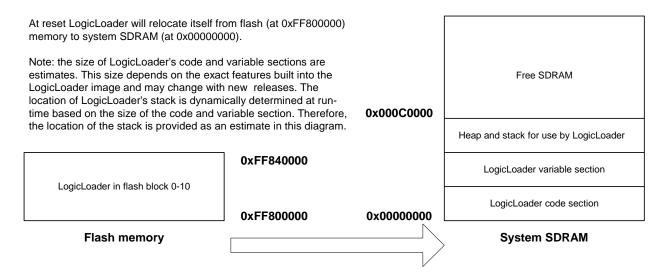


Figure 1.5: LogicLoader RAM Execution Environment (without dBUG in Flash)

2 MCF547x/8x LogicLoader Functionality

2.1 Supported Hardware Peripherals

The table below lists MCF547x/8x-specific peripherals supported by LogicLoader. Additional functionality is possible by implementing custom code or commands on the system.

Hardware Peripheral	Support (Y/N)	Details	
Audio	N		
Display:	Υ	LogicLoader supports 8 and 16 bits per pixel; custom displays can be supported by using the config block	
LCD-3.5-QVGA-10	N		
LCD-3.5-QVGA-20	Υ	Display kit with LCD part number LQ035Q7DB02	
LCD-3.6-QVGA-10	Υ	Display kit with LCD part number LQ036Q1DA01	
LCD-5.7-QVGA-10	Υ	Display kit with LCD part number LQ057Q3DC02	
LCD-6.4-VGA-10	Υ	Display kit with LCD part number LQ64D343	
LCD-10.4-VGA-10	Y	Display kit with LCD part number LQ10D368	
LCD-12.1-SVGA-10	Y	Display kit with LCD part number LQ121S1DG31	
CAN	N		
Ethernet	Υ	10/100MBit support	
Flash Memory	Υ	4 MB Boot NOR for MCF54x4 Kits, 2MB Boot + 16MB Code for MCF54x5	
IrDA	N		
Memory Card Expansion:	Υ	CompactFlash memory cards are supported only. 16 -> 256MB memory densities have been verified.	
IO Mode PCMCIA/ CF	N		
Memory Mode CF	Υ	Recommended: SanDisk, Toshiba, PNY. Programmed CPLD required for this feature.	
SD/MMC	N		
Smart Card	N		
PCI	Υ	Partial on-board peripheral support only.	
Processor:			
Cache	Υ	Copy-back mode	
Clock	Υ	266MHz (MCF547x), 200MHz (MCF548x)	
Power Management	N		
MMU	N		
RTC (on baseboard)	N		
SDRAM	Υ	CS-0 (64MB, 128MB); CS-1 (128MB)	
Serial Port:			
UART0	Υ	115200 baud standard, 2400 to 460800 baud can be supported by using the config block	
UART1	N		
UART2	N		
UART3	N		
USB Host	N		
USB Function	N		
Misc:			
GPIO	Y	Use 'w' and 'x' commands to access data direction and data registers to control GPIO lines per register description in processor and IO Controller specification documents.	
Status	Υ	Toggles to show system "heartbeat"	
Mode Line 2	N		
Serial EEPROM	Y	128 bytes	
Jenai LLF NOW	1	120 Dytes	

3 Disclaimer

Logic strives to provide the most up to date information. However, the list of supported features in this document is partial and subject to change.

The "Supported Hardware Peripherals" table was created to describe the supported features for fully populated standard card engine builds. If the card engine in use is a custom build or has some hardware feature omitted, the commands related to those hardware features may not function.

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