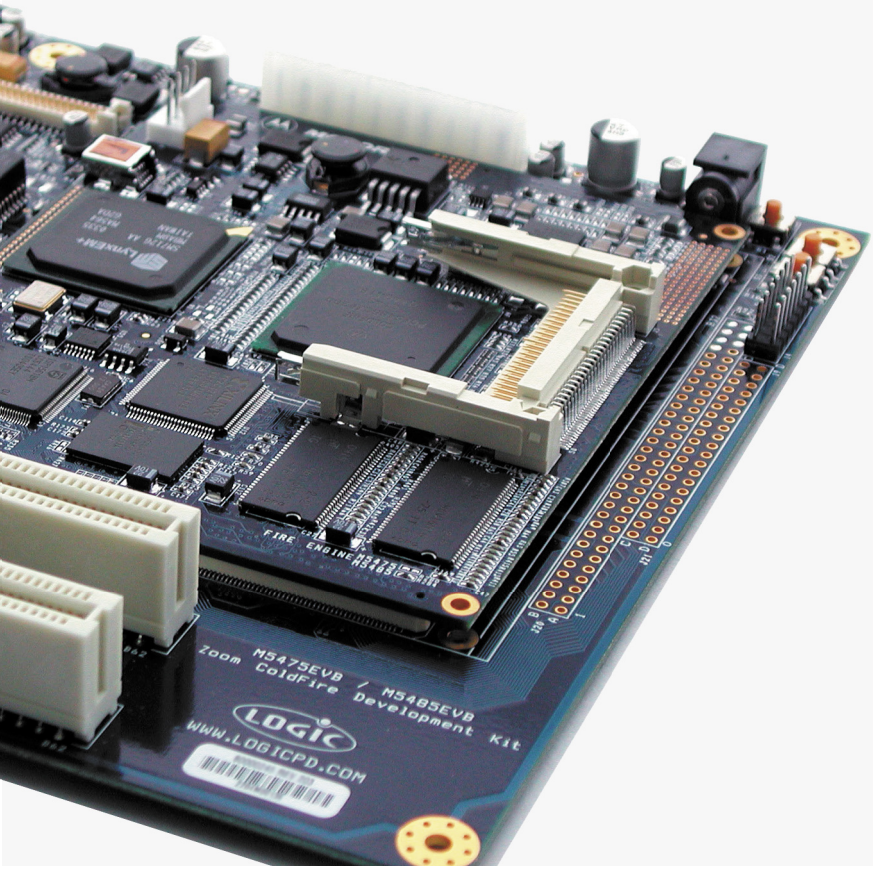
Zoom™

ColdFire Development Kit

M547x/8x Fire Engine Hardware Specification



developed by LOGIC

Launched by Motorola
freescale semiconductor

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A	Kurt Larson	Pilot update	KTL	8/02/04
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C	Nathan Kro	Internal Release: Added note to Mechanical Drawing	KTL	11/12/04
D	Nathan Kro	Updated Section 9	KTL	12/17/04
E	Kurt Larson	Corrected CAN0/CAN1 locations	KTL	04/15/05

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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Table of Contents

1 Introduction ... 1
1.1 Product Brief ... 1
1.2 Acronyms ... 2
1.3 Technical Specifications ... 3
1.4 Fire Engine Advantages ... 4
1.5 Fire Engine Interface ... 5
1.6 Fire Engine ETX Block Diagram ... 6
1.7 Electrical, Mechanical, and Environmental Specifications ... 7
1.7.1 Absolute Maximum Ratings ... 7
2 Electrical Specification ... 8
2.1 Microcontroller ... 8
2.1.1 Freescale MCF547x/8x Block Diagram ... 8
2.2 Clocks ... 9
2.3 DDR RAM Memory ... 9
2.4 NOR Flash (Boot) ... 9
2.5 NOR Flash (Code)(Optional) ... 9
2.6 CompactFlash Interface ... 9
2.7 Diagnostic/Debug Interface ... 9
2.8 Serial Interface ... 10
2.9 PCI Interface ... 10
2.9.1 PCI- USB Host ... 11
2.9.2 PCI- Video ... 11
2.9.3 External PCI Ports ... 12
2.10 On Board USB Device Interface ... 12
2.11 Ethernet Interface ... 13
2.12 CAN Interface ... 13
2.13 FlexBus Interface ... 13
2.14 CPLD ... 14
2.15 I2C (Inter-Integrated Circuit) ... 14
3 System Integration ... 15
3.1 Module Configurations ... 15
3.2 Resets ... 16
3.3 Microcontroller Configuration on Reset ... 16
3.4 Debugger Interface/BDM Connector ... 17
3.5 Power Management ... 17
3.6 ESD Considerations ... 17
4 Memory & I/O Mapping ... 18
5 ETX Pin Definitions Listed by Connector Number ... 19
5.1 J1 (X1) ... 19
5.2 J2 (X2) ... 20
5.3 J3 (X3) ... 21
5.4 J4 (X4) ... 22
6 ETX Connector Signal Description ... 24
6.1 Reset Input Signal ... 24
6.2 SPI Interface Signals ... 24
6.3 I2C Interfaces Signals ... 25
6.4 Programmable Timer In/ Out Signals ... 25
6.5 FlexBus Signals (PC104 Interface) ... 26
6.6 DMA Control Signals ... 28
6.7 CPLD Signals ... 28
6.8 Video Display Signals ... 28
6.9 Flat Panel Display Signals ... 29
6.10 PCI Bus Signals ... 30

 All Rights Reserved

6.11 Ethernet Signals 32
6.12 Serial Port Signals 33
6.13 USB Signals 35
6.14 Reserved Pins: 35
6.15 VCC 5V 35
6.16 3.3V: 36
6.17 Ground 36
6.18 Not Connected 36
7 Differences: ETX Standard vs. ETX Fire Engine 37
7.1 X1 Connector: 37
7.2 X2 connector: 38
7.3 X3 Connector: 40
7.4 X4 Connector: 41
8 General Purpose I/O 44
9 Mechanical Specifications 46
9.1 ETX Footprint 46
9.2 Mating ETX Footprint 47

 All Rights Reserved

Table of Figures

Figure 1.1: Logic's Fire Engine 5
Figure 1.2: Logic's Fire Engine Advantage: ETX Board Installed On Mini-ITX Host Platform 5
Figure 1.3: ETX Block Diagram 6
Figure 2.1: MCF548x Block Diagram 8
Figure 2.2: PCI Interface Diagram 11
Figure 2.3: PCI Video Diagram 12
Figure 8.1: GPIO Table 45
Figure 9.1: Fire Engine ETX Footprint Mechanical Drawing 46
Figure 9.2: Fire Engine Mating ETX Footprint Mechanical Drawing 47

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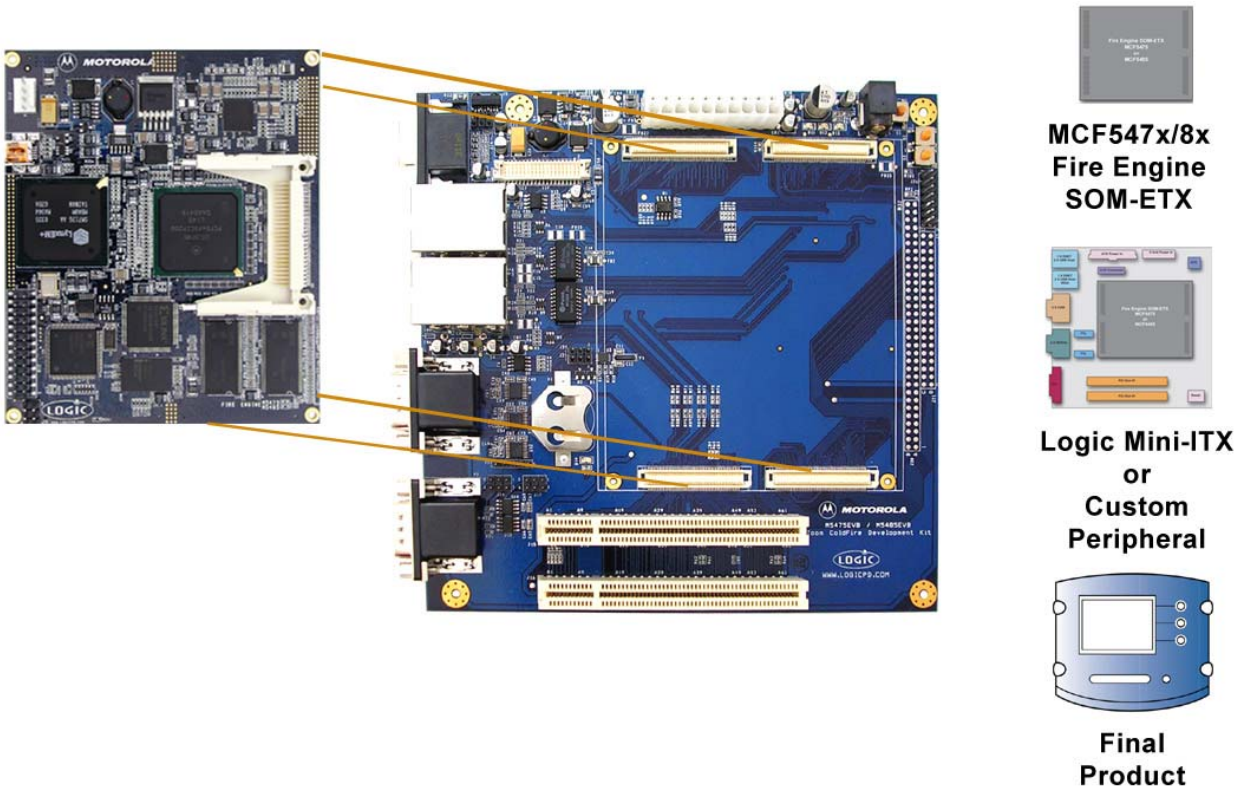
1 Introduction

1.1 Product Brief

The MCF547x/8x Fire Engine is a compact, product ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The MCF547x/8x Fire Engine is a complete single board computer offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. Customers can use the product ready Mini-ITX development kit, ETX standard carrier boards, custom baseboards, or a standalone Fire Engine to accelerate product development and time to market. The standard ETX form factor and signal pin out provides scalability to next generation microcontroller Fire Engines when new functionality for performance is required.



Actual Size: 3.7" x 4.5"

Processor: Freescale MCF547x or MCF548x Processor

DDR RAM Memory: Selectable 64MB or 128MB

Flash Memory: 2MB Boot flash, Selectable User Flash from 0MB to 32MB

Display: Optional Silicon Motion SM712 Graphics Controller

- DSTN and TFT LCD support up to 1024x768 resolution
- CRT or TV output also available

Network Support:

- Processor supported dual 10/100 Ethernet MAC
- Onboard Broadcom dual 10/100 Ethernet PHY

PC Card Expansion:

- Supports two offboard PCI 2.2 slots
- Supports one Compact Flash Type 1 Memory Mode Only Slot

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USB:

- Processor supported Single USB Highspeed Device port with mini jack onboard
- Optional Four USB 2.0 High speed host ports supported by the Philips ISP1561

GPIO: Programmable I/O depending on peripheral requirements

Serial Ports:

- Up to four 115.2Kbps RS-232 serial ports

CAN 2.0b: Two ports (supported by MCF548x only)

SPI: Processor supported SPI interface

Software:

- LogicLoader™ (bootloader/monitor)
- ARC MQX RTOS[1]
- Freescale dBUG ROM Monitor
- Green Hills Integrity[1]

Mechanical SOM-ETX:

- 3.7" (93.4 mm) long x 4.5" (114.3 mm) wide x .5" (14 mm) high

[1]*Third party ports available from Freescale*

1.2 Acronyms

ADC	Analog to Digital Converter
BDM	Background Debug Mode
BoLo	Boot Loader
BSP	Board Support Package
CMOS	Complimentary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSPI	DMA Serial Peripheral Interface
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
ETX	Embedded Technology Extended
FEC	Fast-Ethernet Controller
FET	Field Effect Transistor
FIFO	First In First Out
FIR	Fast Infrared
GPIO	General Purpose Input Output
IC	Integrated Circuit
I²C	Inter-Integrated Circuit
I/O	Input/Output
IRED	Infrared Device
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MBAR	Module Base Address Register
MIR	Mid Infrared
MMC	Multimedia Card
NC	No Connect
PC	Personal Computer
PCI	Peripheral Component Interconnect
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
POTS	Plain Old Telephone System

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PSC	Programmable Serial Controller
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System-on-Chip
SoM	System-on-Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Freescale ColdFire Microcontroller MCF547x/8x
- USB Host Controller ISP1561BM
- CPLD Xilinx XC2C128
- Broadcom Ethernet PHY BCM5222KPF
- DDR SDRAM MT46V16M16TG
- Boot Flash TE28F160C3BD70
- User/Code Flash RC28F256K3C120
- Video Controller Silicon Motion SM712
- Logic Document: Mini-ITX Hardware Specification
- Logic Document: Application Note 228: Fire Engine Design Guideline

Note: *All users implementing the Fire Engine module should reference Logic's* Application Note 228: Fire Engine Design Guideline *document.*

For further Freescale documentation please visit: http://www.freescale.com/.

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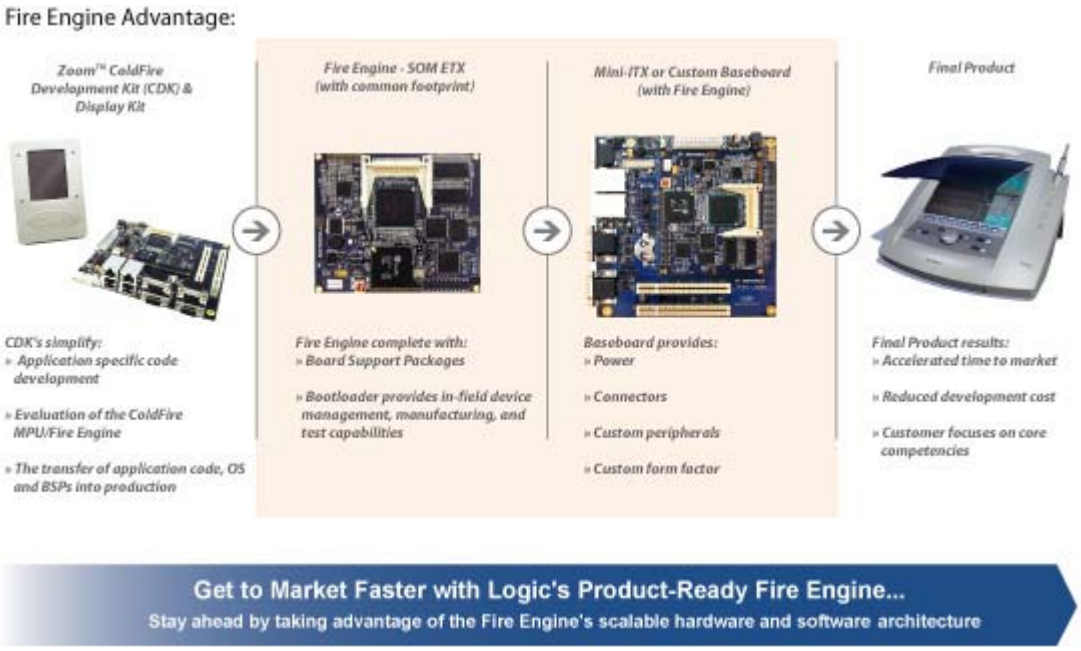
1.4 Fire Engine Advantages



- Logic's Fire Engines accelerate your product's time-to-market, and provide the following advantages:
  - Product Ready Hardware and Software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – Allows you to focus on other aspects of your design
- Common SOM-ETX form factor
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations are available to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

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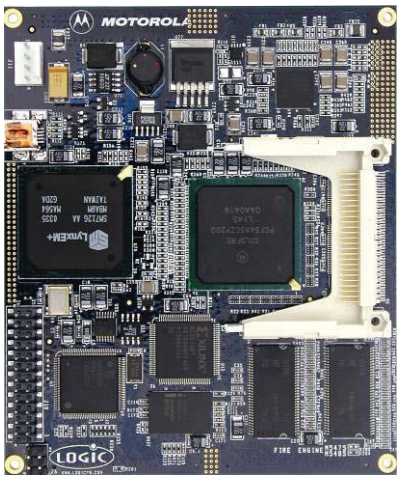
1.5 Fire Engine Interface

The ETX interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common ETX footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of your design onto the Fire Engine reduces any long-term risk of obsolescence. If a component on the Fire Engine design becomes obsolete, Logic will simply design for alternative part that is transparent to your product. Furthermore, Logic tests all Fire Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.



Fire Engine Top View

Fire Engine Bottom View

Figure 1.1: Logic's Fire Engine

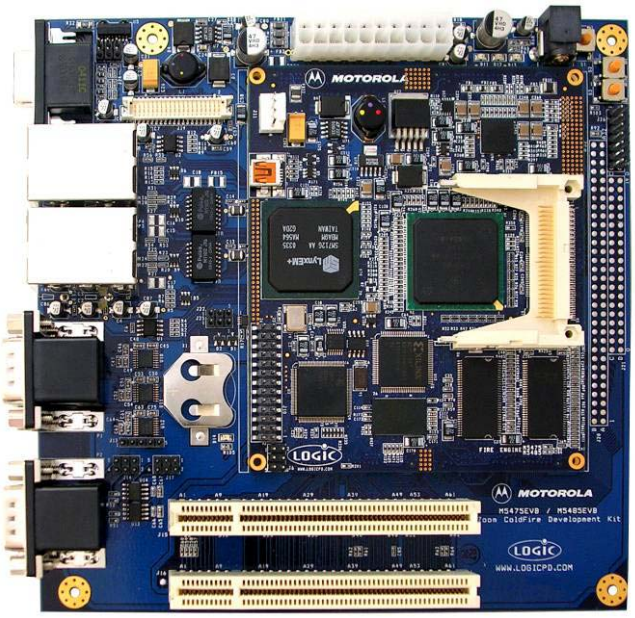


Figure 1.2: Logic's Fire Engine Advantage: ETX Board Installed On Mini-ITX Host Platform

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1.6 Fire Engine ETX Block Diagram

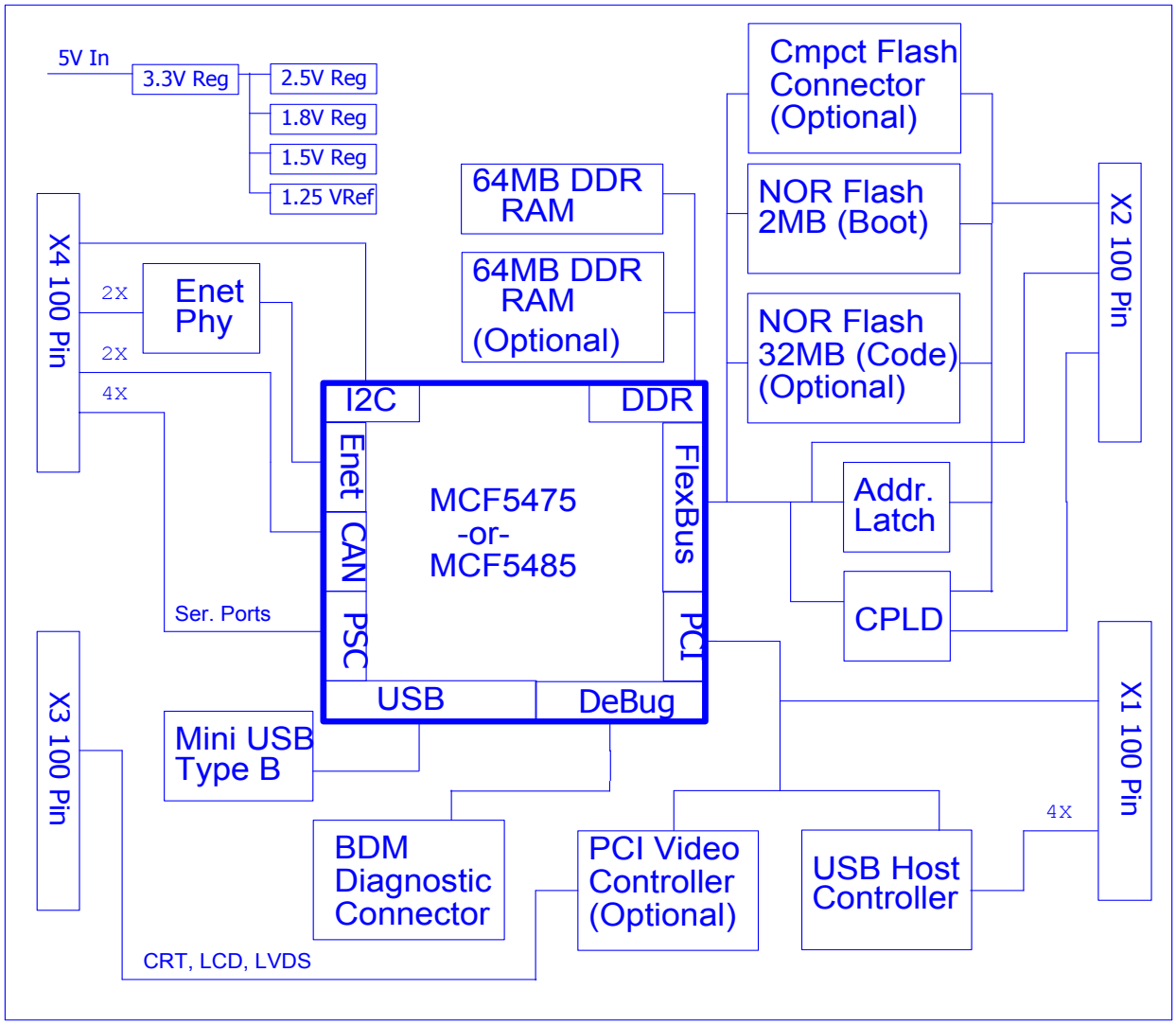

Figure 1.3: ETX Block Diagram

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1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	unit
Power Supply Input Voltage	6V	V
Any signal input on External connectors	4V	V

NOTE: Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Fire Engine and its components.

1.7.1.1 Recommended Operating Conditions

Parameter	MCF547x: Min	MCF547x: Typical	MCF547x: Max	MCF548x: Min	MCF548x: Typical	MCF548x: Max	Unit	Notes
DC Supply Voltage	4.75	5.00	5.25	4.75	5.00	5.25	V	
DC Supply Active Current		1.1			1.1		A	
Operating Temperature	0		70	-40		+85	°C	
Storage Temperature	-55		+150	-55		+150	°C	
ETX Connector Insertion/removal		50			50		Cycles	
Input signal High Voltage	2.0	3.0	3.6	2.0	3.0	3.6	V	
Input Signal Low Voltage	-.5	0	.8	-.5	0	.8	V	
Output Signal High Voltage	2.4			2.4			V	
Output Signal Low Voltage	0		.5	0		.5	V	

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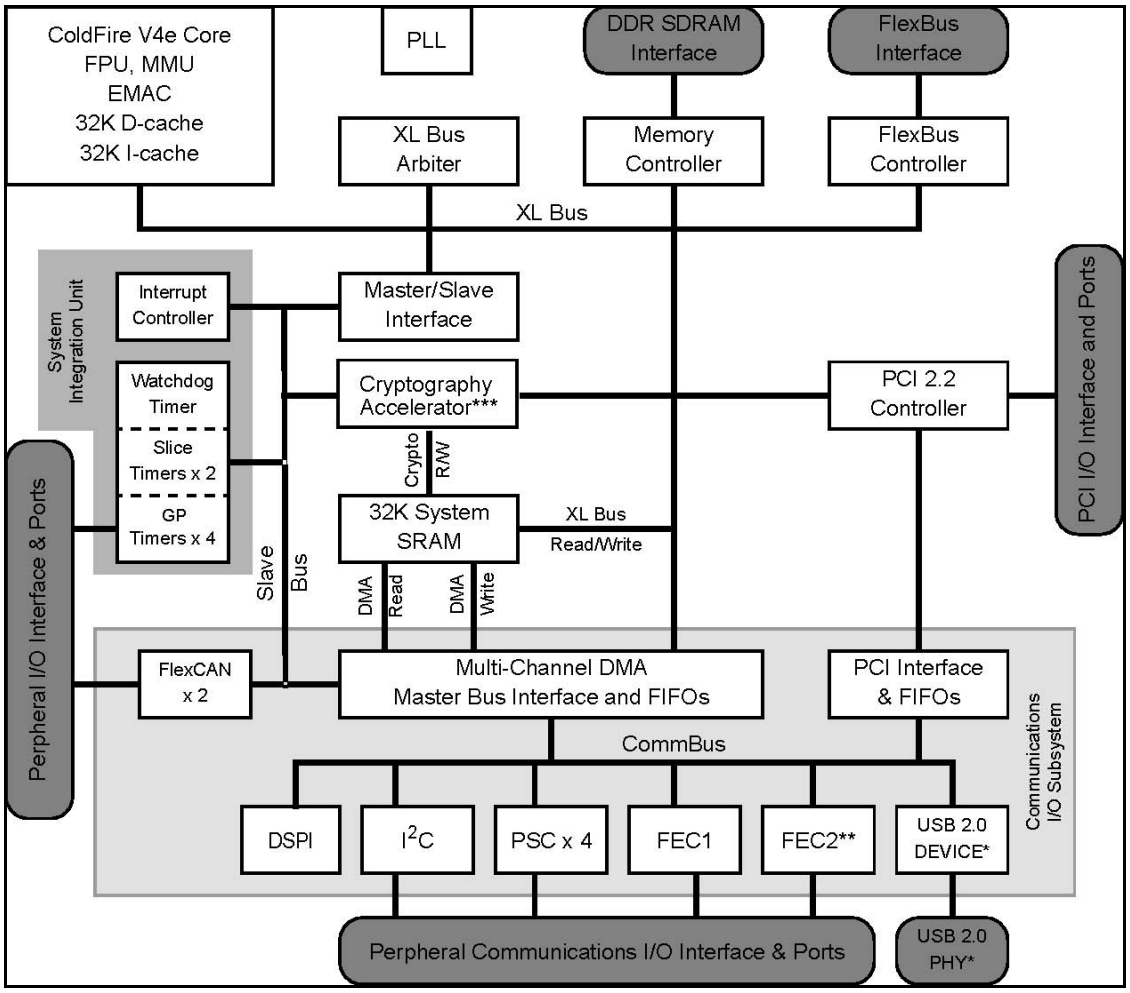
2 Electrical Specification

2.1 Microcontroller

The featured microcontroller is the MCF547x/8x superset processor from the Freescale ColdFire family. However, since all the derivatives of the family are pin-compatible, any member of the MCF547x/8x family can be populated on this platform.

Logic offers this ETX product with either an MCF547x or MCF548x processor installed.

2.1.1 Freescale MCF547x/8x Block Diagram



*Available in MCF5485, MCF5484, MCF5483, and MCF5482 devices. **Available in MCF5485, MCF5484, MCF5481, and MCF5480 devices. ***Available in MCF5485, MCF5483, and MCF5481 devices.

Figure 2.1: MCF548x Block Diagram

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2.2 Clocks

MCF548x: The system clock provided is a 50 MHz Oscillator that provides a PCI operating speed of 50MHZ, a DDR RAM operating frequency of 100MHZ, and a core operating frequency of 200MHZ.

MCF547x: The system clock provided is a 66MHz Oscillator that provides a PCI operating speed of 66MHz, a DDR RAM operating frequency of up to 133MHZ, and a core operating frequency of up to 266MHz.

The input clock to the MCF547x/8x is applied to the PCI bus and FlexBus. The input clock X2 is applied to DDR RAM, and the input clock X4 is applied to the internal processor.

Half the oscillator frequency is used as the system clock when the USB Host controller chip is populated. If R288 on the back of the ETX board is populated and R285 is not, the system clock operates at the Oscillator Rate. If R285 is populated and R288 is not, the system clock operates at ½ the OSC rate.

2.3 DDR RAM Memory

DDR RAM is provided on board in two densities: 64MB and 128MB It is organized as 16 M Words (or 32 M words) X 32 Bits wide. The speed grade of these chips allow clocks at 100 MHz with the CAS latency set at 2 and 133 MHz with the CAS latency set at 2.5. (Please refer to the Micron Technology data sheet for more information). This provides a maximum memory bandwidth of 8.5 Gbits/sec.

2.4 NOR Flash (Boot)

The Fire Engine ETX module ships with 2MB or 4MB onboard NOR flash which contains the Logic Loader operating system. The processor boots from this memory area by default on reset. This memory is organized as 1M x 16 Bits wide. It is attached to the MCF547x/8x FlexBus interface and appears in the FlexBus Memory Map on Chip Select #0.

2.5 NOR Flash (Code)(Optional)

An optional 0, 16, or 32 Mbytes of NOR Flash is available. This flash area is intended for user code including operating systems or other custom functionality. This memory is organized as 16M x 16 Bits wide. It is attached to the MCF547x/8x FlexBus interface and appears in the FlexBus Memory Map on Chip Select #1.

2.6 CompactFlash Interface

The Compact Flash connector on the ETX board provides removable media capability. It has a 16 bit wide data bus and is attached to the Microcontroller FlexBus interface. Its address space in the memory map is dependant on the CPLD. Please contact Logic Product Development for detailed CPLD information and usage.

2.7 Diagnostic/Debug Interface

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The MCF547x/8x debug module provides support in three different areas:

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- Real-time trace support: The ability to determine the dynamic execution path through an application is fundamental for debugging. The ColdFire solution implements an 8-bit parallel output bus that reports processor execution status and data to an external BDM emulator system.
- Background debug mode (BDM): Provides low-level debugging in the ColdFire processor complex. In BDM, the processor complex is halted and a variety of commands can be sent to the processor to access memory and registers. The external BDM emulator uses a three-pin, serial, full-duplex channel.
- Real-time debug support: BDM requires the processor to be halted, which many real-time embedded applications cannot permit. Debug interrupts let real-time systems execute a unique service routine that can quickly save key register and variable contents and return the system to normal operation without halting. External development systems can access saved data because the hardware supports concurrent operation of the processor and BDM-initiated commands. In addition, the option is provided to allow interrupts to occur, a 26 pin diagnostic connector is provided to interface to Freescale's standard BDM Module for the purpose of program emulation, monitoring and debugging. Debugging and development software from companies such as P&E Microcomputer Systems Inc. or Green Hills Software Inc. and many other vendors can be used with this interface.

2.8 Serial Interface

4 Programmable Serial Controllers (PSC) are available and are wired directly from the Freescale processor to the ETX external connectors.

The 4 PSC's can be independently configured to operate in the following modes:

- Universal asynchronous receiver transmitter (UART) mode
  - 5,6,7,8 bits of data plus parity
  - Odd, even, none, or force parity
  - Stop bit width programmable in 1/16 bit increments
  - Parity, framing, and overrun error detection
  - Automatic PSCCTS and PSCRTS modem control signals
- IrDA 1.0 SIR mode (SIR)
  - Baud rate range of 2400–115200 bps
  - Selectable pulse width: either 3/16 of the bit duration or 1.6 µs
- IrDA 1.1 MIR mode (MIR)
  - Baud rate of 0.576 or 1.152 Mbps
- IrDA 1.1 FIR mode (FIR)
  - Baud rate of 4.0 Mbps
- 8-bit soft modem mode (modem8)
- 16-bit soft modem mode (modem16)
- AC97 soft modem mode (AC97)

Each PSC supports synchronous (USART) and asynchronous (UART) protocols. The PSC's can be used to interface to external full-function modems or external CODEC's for soft modem support, as well as IrDA 1.1 or 1.0 interfaces. Both 8- and 16-bit data widths are supported. PSC's can be configured to support 1200 baud plain old telephone system (POTS) modem, V.34 or V.90 protocols. The standard UART interface supports connection to an external terminal/computer for debug support.

2.9 PCI Interface

The Freescale processor has a built-in PCI interface Host/arbiter and provides for 4 ports external to the chip. 2 of these ports are used on the ETX board (USB Host and PCI Video) and 2 PCI ports are available for external use offboard. Although 2 ports are available, it is not mandatory to use them.

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The PCI controller is a PCI V2.2-compliant bus controller and arbiter. The PCI bus is capable of 66-MHz operation with a 32-bit address/data bus and support for five external masters.

Important Note: A Fire Engine Module with USB Host controller limits the PCI bus to a Maximum clock rate of 33MHZ.

Processor	USB Host onboard	PCI CLK
MCF547x	Y	33MHz
MCF547x	N	66MHz
MCF548x	Y	25MHz
MCF548x	N	50MHz

Figure 2.2: PCI Interface Diagram

The USB Host controller (U3) shares processor IRQ5 with the Graphics Controller (U70), and offboard PCI IRQC# and IRQD#.

The USB Host controller (U3) utilizes AD17 for IDSEL making it PCI Device ID 1.
The Graphics Controller (U70) utilizes AD18 for IDSEL making it PCI Device ID 2.

The PCI module includes an inbound FIFO to increase performance when using an external bus master. The bus can address all 4 Gbytes of PCI-addressable space.

When implemented, the PCI controller acts as the central resource, bus arbiter, and configuring master on the PCI bus.

2.9.1 PCI- USB Host

A USB Controller Manufactured by Philips provides 4 standard USB ports to the Host Board.
The ISP1561 is a PCI-based, single-chip Universal Serial Bus (USB) Host Controller. It integrates two Original USB Open Host Controller Interface (OHCI) cores, one Hi-Speed USB Enhanced Host Controller Interface (EHCI) core and four transceivers that are compliant with Hi-Speed USB and Original USB. The functional parts of the ISP1561 are fully compliant with Universal Serial Bus Specification Rev.2.0, Open Host Controller Interface Specifications Rev.1.0a, Enhanced Host Controller Interface Specification for Universal Serial BusRev.0.95, PCI Local Bus Specification Rev. 2.2and PCI Bus Power Management Interface Specification Rev.1.1.

The integrated high performance USB transceivers enable the ISP1561 to handle all Hi-Speed USB transfer speed modes: high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s). The ISP1561 provides four downstream ports that enable simultaneous connections of USB devices at different speeds.

The USB Host controller (U3) shares processor IRQ5 with the Graphics Controller (U70), and offboard PCI IRQC# and IRQD#. It utilizes AD17 for IDSEL making it PCI Device ID 1.

Contact Logic Product Development for assistance in implementing USB Host hardware or software solutions.

2.9.2 PCI- Video

Through the use of an on-board LynxEM+ Video chip manufactured by Silicon Motion, Support can be provided for CRT, LCD, and flat-panel type displays.

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The Graphics controller (U70) shares processor IRQ5 with the USB Host Controller (U3), and offboard PCI IRQC# and IRQD#. It also utilizes AD18 for IDSEL making it PCI Device ID 2.

The Fire Engine provides the CRT and LCD interfaces off board through ETX connector X3. Logic Product Development sells three Zoom Display Kits that interface directly with Logic Product Development SOM-ETX Fire Engines, Mini-ITX baseboards, and Logic software ports. The displays kits are available in 3.5” QVGA, 6.4” VGA, and 12.1” SVGA sizes.

Part Number	Size	Type
MQVGADK	3.5"	Color TFT
MVGADK	6.4"	Color TFT
MSVGADK	12.1"	Color TFT

Figure 2.3: PCI Video Diagram

Contact Logic Product Development for assistance in implementing various display types involving hardware or software solutions. Example circuitry for interfacing to CRT and LCD interfaces is available on Logic Product Development’s Mini ITX application board.

2.9.3 External PCI Ports

Signals are provided to allow the host board to contain 1 or 2 standard 32-bit 33 MHz **3.3V only** PCI slots. The PCI signals to the MCF547x/8x are not 5V tolerant.

External ETX IRQA# and IRQB# signals are connected to processor IRQ7#. IRQC# and IRQD# are shared with the onboard graphics controller (U70) and USB Host controller (U3) and tied to the processor IRQ5#.

The PCI reference clock is dependant on the board configuration. The following table outlines standard configurations. Contact Logic Product Development for alternate configurations. See Figure 2.2, above.

Example circuitry for interfacing to external PCI slots is available on Logic Product Development’s Mini ITX application board.

2.10 On Board USB Device Interface

The Freescale Processor has provisions for a USB Device on chip. This interface is available via an on-board mini USB type B connector.

The USB module implementation on the MCF547x/8x product family provides all the logic necessary to process the USB protocol as defined by version 2.0 specification for peripheral devices.

- High-speed operation up to 480 Mbps, full-speed operation at 12 Mbps, and low-speed operation at 1.5 Mbps
- Physical interface on chip
- Bulk, interrupt, and isochronous transport modes.
- Six programmable in/out endpoints and one control endpoint
- 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM

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2.11 Ethernet Interface

The processor supports a dual 10/100 MAC interface and a Broadcom Ethernet PHY is provided to give connectivity to two 10/100 Ethernet ports on the host board.

The controller is full duplex, supports a programmable maximum frame length and retransmission from the transmit FIFO following a collision.

- IEEE 802.3 full-duplex flow control.
- Support for full-duplex operation (200 Mbps throughput) with a minimum system clock frequency of 50 MHz.
- Support for half duplex operation (100 Mbps throughput) with a minimum system clock frequency of 25 MHz.
- Retransmit from transmit FIFO following collision.
- Internal loopback for diagnostic purposes.

Example circuitry for interfacing to the Ethernet interface is available on Logic Product Development's Mini ITX application board.

Note: baseboards require these signals to be routed as differential pairs due to impedance characteristics of the board and other layout considerations.

2.12 CAN Interface

2 Controller Area Network (CAN) interfaces are provided through the ETX connectors from the on-chip ports of the Freescale processor. Freescale refers to these as FlexCAN modules implementing the CAN protocol. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of real-time processing and reliable operation in a harsh EMI environment, while maintaining cost-effectiveness. Each of the two CAN controllers on the MCF548x family products contains sixteen message buffers. The CAN controllers can be configured to either function as an interface with two separate CAN networks, or as a single 32 message buffer CAN network.

Note: ONLY supported on the MCF548x series of processors. Transceiver example circuitry is available on the Mini ITX application board design.

2.13 FlexBus Interface

The FlexBus module is intended to provide the user with basic functionality required to interface to peripheral devices. The FlexBus interface is a multiplexed or non-multiplexed bus, with an operating frequency from 25MHz–66 MHz. The FlexBus is targeted to support external Flash memories, boot ROMs, gate-array logic, or other simple target interfaces. Up to six chip selects are supported by the FlexBus.

The Flex bus is multiplexed out of the processor and the address is latched before it is brought offboard and to the other host based chips onboard.

The FlexBus frequency is based on the processor type and onboard PCI peripheral set. See the clocking section for details. The FlexBus will either be 25MHz, 33MHz, 50MHz, or 66MHz based on PCI requirements and processor type.

Logic uses a 32bit multiplexed address bus and latches the address to boot from an onboard 16bit 2MB flash device.

Address latching is provided along with a CPLD for custom I/O applications.

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2.14 CPLD

The onboard CPLD provides power management, CompactFlash, ISA, and onboard EEPROM support. The CPLD has the ability to be reprogrammed in circuit so in the field updates are possible. Please contact Logic Product Development for more information regarding the onboard CPLD interface and its features.

2.15 I2C (Inter-Integrated Circuit)

The MCF547x/8x provides an I2C two-wire, bi-directional serial bus for on-board communication.

- Multimaster operation with arbitration and collision detection
- Calling address recognition and interrupt generation
- Automatic switching from master to slave on arbitration loss
- Software-selectable acknowledge bit
- Start and stop signal generation and detection
- Bus busy status detection

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3 System Integration

3.1 Module Configurations

The Fire Engine was designed to meet multiple applications for specific users and budget requirements. As a result, the Fire Engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Optional RAM: 64MB or 128MB DDR SDRAM
- Optional NOR FLASH ROM, 0, 16, or 32MB
- Optional Graphics Controller
- Optional USB Controller

Below is the complete table of standard available models. Please contact Logic Product Development for additional hardware configurations to meet your application needs.

Freescale PN	DDR Mem	Nor Flash	Boot Flash	Graphics Ctrlr	USB*
MCF5475AFE	64MB	0	2MB	-	-
MCF5475BFE	64MB	16	2MB	-	-
MCF5475CFE**	64MB	16	2MB	Y	Y
MCF5475DFE	64MB	0	2MB	-	Y
MCF5475EFE	64MB	0	2MB	Y	Y
MCF5475FFE	128MB	32	2MB	Y	Y
MCF5474GFE***	64MB	0	4MB	-	-

*When ordering Fire Engines with USB Host PCI slot is locked at 33 MHz
**Denotes the Fire Engine module on the M5475EVB Zoom ColdFire Development Kit
***Denotes the Fire Engine module on the M5474EVB Zoom ColdFire Lite Development Kit

Freescale PN	DDR Mem	Nor Flash	Boot Flash	Graphics Ctrlr	USB*
MCF5485AFE	64MB	0	2MB	-	-
MCF5485BFE	64MB	16	2MB	-	-
MCF5485CFE**	64MB	16	2MB	Y	Y
MCF5485DFE	64MB	0	2MB	-	Y
MCF5485EFE	64MB	0	2MB	Y	Y
MCF5485FFE	128MB	32	2MB	Y	Y
MCF5484GFE***	64MB	0	4MB	-	-

* When ordering Fire Engines with USB Host PCI slot is locked at 25 MHz
** Denotes the Fire Engine Configuration on M5485EVB Zoom ColdFire Development Kit
***Denotes the Fire Engine module on the M5484EVB Zoom ColdFire Lite Development Kit

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3.2 Resets

All hardware peripherals should connect their hardware-reset pin to the RESET# signal on the external connector (X2-98). Internally all Fire Engine peripheral hardware reset pins are connected to the RESET#. Typically, the ETX Carrier board will contain a push-button switch that will provide a Master Reset to the hardware. This switch is connected to the Fire Engine via external connector pin X4-98. "De-bouncing" circuitry is incorporated on the Fire Engine which holds the RESET# active for approximately 130ms after the push button is released.

3.3 Microcontroller Configuration on Reset

At reset, FB_AD[12:0] and MTMOD0 are used to determine various configurations. The following table shows the reset configuration options.

Pin(s)	Chip Configuration Function	Operation	
FB_AD[1:0]	Boot Chip-Select Data Port Size Configuration	00 01 1x*	32-bits 8-bits 16-bits
FB_AD[2]	Boot Chip-Select Auto Acknowledge Configuration	0 1*	External termination Only (auto acknowledge disabled) Internal or external termination (auto acknowledge with 63 wait states)
FB_AD[3]	Byte Strobe Configuration	0* 1	/FB_BS[3:0] will assert on read and write cycles /FB_BS[3:0] will only assert for write cycles
FB_AD[4]	FlexBus/PCI Operating Mode	0 1*	FB_AD[31:0] used for FlexBus Data and PCI_AD[31:0] used for FlexBus Address; PCI module disabled. FB_AD[31:0] used for multiplexed FlexBus Address and Data
FB_AD[5]	Byte Strobe/Size/FlexBus Address Configuration	0* 1	Bytes Strobes output on /FB_BS[3:0] (operation determined by FB_AD[3] reset configuration bit) /SIZ[1:0] output on /FB_BS[3:2] and FB_ADDR[1:0] output on /FB_BS[1:0]
FB_AD[12:8]	PLL Clock Configuration	00011* 00101 01111	1:2 SD_CLK to CLKIN ratio 1:2 SD_CLK to CLKIN ratio 1:4 SD_CLK to CLKIN ratio
MTMOD0	BDM/JTAG Select	0* 1	BDM Mode JTAG Mode

Note: "*" Denotes default setting for the Fire Engine.

To accommodate this configuration on the Fire Engine board, a set of resistor pads has been placed on the bottom side of the board near U92.

0 Ohm resistors are soldered between the center pad and the "+" pad to set a specific bit to a "1" and are soldered between the center pad and the "-" pad to set a specific bit to a "0"

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3.4 Debugger Interface/BDM Connector

The debug signals will be brought out to one 2x13 header. This 26-pin header will be labeled as 'BDM'. The revision D BDM pin-out is shown in Figure 3.2. For timing purposes, the PSTDDATA[7:0] signals should be impedance matched. The signal traces to the BDM header should be less than three inches from the MCF547x/8x part.

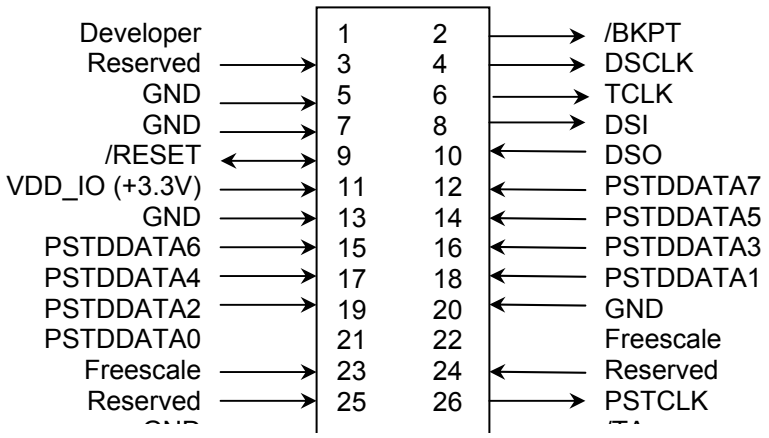

Figure 3.2: BDM Connector (Revision D)

3.5 Power Management

The power input requirement to the Fire engine is 5VDC +/- 5% @ at least 2A. This can be supplied in either of 2 ways;

1. Through the external connectors, X1,X2,X3,X4 when the Fire Engine is plugged on to a host board.
2. Via J11. This is a 4-pin connector that is adaptable to many requirements. Pins 1 and 2 are dedicated to 5V and pins 3 and 4 are dedicated to GND.

All of the other required voltages are acquired via regulators off the 5V input onboard.
These voltages are: 3.3V, 2.5V, 1.8V, 1.5V and 1.25V.

3.6 ESD Considerations

The Fire Engine was designed to interface to a customer's peripheral board, be low cost and adaptable to many different applications. It does not provide any on-board ESD protection circuitry – this must be provided by the product in which it is used. Logic has extensive experience in designing products with ESD requirements. Please contact Logic Product Development if you need any assistance in ESD design considerations.

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4 Memory & I/O Mapping

On the Freescale ColdFire MCF547x/MCF548x Microcontroller, all address mapping is accomplished through the use of a Module Base Address Register (MBAR) and several Address pointer registers. Please consult the Microcontroller Reference Manual for details.

FlexBus:

Mapped “Chip Select” signals for the FlexBus are available as outputs from the Microcontroller and are assigned as follows:

FB_CS0# = NOR Flash (Boot)
FB_CS1# = NOR Flash (Code)
FB_CS2# = Optional use by CPLD
FB_CS3# = Optional use by CPLD or external (Host Board)
FB_CS4# = Used by CPLD or external (Host Board)
FB_CS5# = Used by CPLD or external (Host Board)

PCI IDSEL Lines:
To form an Address Select on the PCI Bus certain address lines are dedicated to the IDSEL pins on the target chips:

PCI_AD17 = On Board USB Host Controller
PCI_AD18 = On Board Graphics Controller

PCI_AD20 = Recommended for Off Board PCI slot #1
PCI_AD21 = Recommended for Off Board PCI slot #2

DDR RAM Chip Select lines:
SD_CS0 = 1st 64MB bank of DDR RAM
SD_CS1 = 2nd 64MB bank of DDR RAM (Optional)
SD_CS2 = Not Used
SD_CS3 = Not Used

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5 ETX Pin Definitions Listed by Connector Number

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

5.1 J1 (X1)

		J1				J1
Pin	Dir	Signal		Pin	Dir	Signal
1	PWR	GND		2	PWR	GND
3	OUT	PCI_CLK3		4	OUT	PCI_CLK4
5	PWR	GND		6	PWR	GND
7	None	N.C.		8	None	N.C.
9	BIDIR	PCIREQ3#		10	BIDIR	PCI_BG3#
11	BIDIR	PCI_BG2#		12	OUT	3.3V
13	BIDIR	PCIREQ2#		14	None	N.C.
15	None	N.C.		16	OUT	3.3V
17	None	N.C.		18	None	N.C.
19	PWR	VCC		20	PWR	VCC
21	None	N.C.		22	None	N.C.
23	BIDIR	PCI_AD0		24	OUT	3.3V
25	BIDIR	PCI_AD1		26	BIDIR	PCI_AD2
27	BIDIR	PCI_AD4		28	BIDIR	PCI_AD3
29	BIDIR	PCI_AD6		30	BIDIR	PCI_AD5
31	BIDIR	PCI_C/BE0#		32	BIDIR	PCI_AD7
33	BIDIR	PCI_AD8		34	BIDIR	PCI_AD9
35	PWR	GND		36	PWR	GND
37	BIDIR	PCI_AD10		38	None	N.C.
39	BIDIR	PCI_AD11		40	BIDIR	M66EN
41	BIDIR	PCI_AD12		42	None	N.C.
43	BIDIR	PCI_AD13		44	None	N.C.
45	BIDIR	PCI_AD14		46	None	N.C.
47	BIDIR	PCI_AD15		48	None	N.C.
49	BIDIR	PCI_C/BE1#		50	None	N.C.
51	PWR	VCC		52	PWR	VCC
53	BIDIR	PCI_PAR		54	BIDIR	PCI_SERR#
55	BIDIR	PCI_PERR#		56	None	N.C.
57	None	N.C.		58	BIDIR	USB_DM3
59	BIDIR	PCI_LOCK#		60	BIDIR	PCI_DEVSEL#
61	BIDIR	PCI_TRDY#		62	BIDIR	USB_DM4
63	BIDIR	PCI_IRDY#		64	BIDIR	PCI_STOP#
65	BIDIR	PCI_FRAME#		66	BIDIR	USB_DP3
67	PWR	GND		68	PWR	GND
69	BIDIR	PCI_AD16		70	BIDIR	PCI_C/BE2#
71	BIDIR	PCI_AD17		72	BIDIR	USB_DP4

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73	BIDIR	PCI_AD19		74	BIDIR	PCI_AD18
75	BIDIR	PCI_AD20		76	BIDIR	USB_DM1
77	BIDIR	PCI_AD22		78	BIDIR	PCI_AD21
79	BIDIR	PCI_AD23		80	BIDIR	USB_DM2
81	BIDIR	PCI_AD24		82	BIDIR	PCI_C/BE3#
83	PWR	VCC		84	PWR	VCC
85	BIDIR	PCI_AD25		86	BIDIR	PCI_AD26
87	BIDIR	PCI_AD28		88	BIDIR	USB_DP1
89	BIDIR	PCI_AD27		90	BIDIR	PCI_AD29
91	BIDIR	PCI_AD30		92	BIDIR	USB_DP2
93	OUT	PCI_RESET#		94	BIDIR	PCI_AD31
95	INP	INTC#		96	INP	INTD#
97	INP	INTA#		98	INP	INTB#
99	PWR	GND		100	PWR	GND

5.2 J2 (X2)

		J2				J2
Pin	Dir	Signal		Pin	Dir	Signal
1	PWR	GND		2	PWR	GND
3	BIDIR	FB_AD30		4	BIDIR	FB_AD31
5	BIDIR	FB_AD29		6	None	N.C.
7	BIDIR	FB_AD28		8	None	N.C.
9	BIDIR	FB_AD27		10	None	N.C.
11	BIDIR	FB_AD26		12	None	N.C.
13	BIDIR	FB_AD25		14	None	N.C.
15	BIDIR	FB_AD24		16	None	N.C.
17	OUT	MCF_RW#		18	None	N.C.
19	OUT	MCF_OE#		20	INP	548X_DREQ0#
21	OUT	FB_CS3#		22	OUT	548X_DACK0#
23	OUT	FB_CS4#		24	None	N.C.
25	OUT	FB_CS5#		26	None	N.C.
27	None	N.C.		28	None	N.C.
29	OUT	MCF_TA#		30	None	N.C.
31	None	N.C.		32	None	N.C.
33	None	N.C.		34	None	N.C.
35	PWR	GND		36	PWR	GND
37	None	N.C.		38	None	N.C.
39	BIDIR	LA_FB_AD0		40	None	N.C.
41	BIDIR	LA_FB_AD1		42	OUT	BALE
43	BIDIR	LA_FB_AD2		44	None	N.C.
45	BIDIR	LA_FB_AD3		46	None	N.C.
47	BIDIR	LA_FB_AD4		48	INP	ISA_IRQ0
49	BIDIR	LA_FB_AD5		50	INP	ISA_IRQ1
51	PWR	VCC		52	PWR	VCC
53	BIDIR	LA_FB_AD6		54	INP	ISA_IRQ2
55	BIDIR	LA_FB_AD7		56	INP	ISA_IRQ3
57	BIDIR	LA_FB_AD8		58	None	N.C.
59	BIDIR	LA_FB_AD9		60	OUT	SYSCLK

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61	BIDIR	LA_FB_AD10		62	None	N.C.
63	BIDIR	LA_FB_AD11		64	INP	548X_DREQ1#
65	BIDIR	LA_FB_AD12		66	OUT	548X_DACK1#
67	PWR	GND		68	PWR	GND
69	BIDIR	LA_FB_AD13		70	None	N.C.
71	BIDIR	LA_FB_AD14		72	None	N.C.
73	BIDIR	LA_FB_AD15		74	OUT	IORD#
75	BIDIR	LA_FB_AD16		76	OUT	IOWR#
77	BIDIR	LA_FB_AD18		78	BIDIR	LA_FB_AD17
79	BIDIR	LA_FB_AD19		80	None	N.C.
81	INP	CHRDY#		82	OUT	AEN#
83	PWR	VCC		84	PWR	VCC
85	BIDIR	FB_AD16		86	None	N.C.
87	BIDIR	FB_AD18		88	BIDIR	FB_AD17
89	BIDIR	FB_AD19		90	None	N.C.
91	None	N.C.		92	BIDIR	FB_AD20
93	BIDIR	FB_AD21		94	None	N.C.
95	BIDIR	FB_AD22		96	BIDIR	FB_AD23
97	None	N.C.		98	OUT	RESET#
99	PWR	GND		100	PWR	GND

5.3 J3 (X3)

		J3				J3
Pin	Dir	Signal		Pin	Dir	Signal
1	PWR	GND		2	PWR	GND
3	OUT	CRT_RED		4	OUT	CRT_BLUE
5	OUT	CRT_HSYNC		6	OUT	CRT_GREEN
7	OUT	CRT_VSYNC		8	BIDIR	DDC_SCL
9	INP	VID_GND		10	BIDIR	DDC_SDA
11	OUT	FP_DATA4		12	OUT	FP_SHIFTCLK
13	OUT	FP_DATA5		14	OUT	FP_DISPLAY_EN
15	PWR	GND		16	PWR	GND
17	OUT	FP_DATA1		18	OUT	FP_DATA3
19	OUT	FP_DATA0		20	OUT	FP_DATA2
21	PWR	GND		22	PWR	GND
23	OUT	FP_DATA10		24	OUT	FP_DATA13
25	OUT	FP_DATA11		26	OUT	FP_DATA12
27	PWR	GND		28	PWR	GND
29	OUT	FP_DATA20		30	OUT	FP_DATA9
31	OUT	FP_DATA21		32	OUT	FP_DATA8
33	PWR	GND		34	PWR	GND
35	OUT	FP_DATA17		36	OUT	FP_DATA19
37	OUT	FP_DATA16		38	OUT	FP_DATA18
39	PWR	VCC		40	PWR	VCC
41	None	N.C.		42	OUT	FP_VSYNC
43	OUT	TMDS_IDCK		44	OUT	FP_EN
45	OUT	FP_HSYNC		46	OUT	FP_VDDEN
47	OUT	FP_VBIASEN		48	None	N.C.

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49	None	N.C.		50	None	N.C.
51	None	N.C.		52	None	N.C.
53	PWR	VCC		54	PWR	GND
55	None	N.C.		56	OUT	PCI_VID_POWERDOWN#
57	None	N.C.		58	None	N.C.
59	INP	PSC2_RXD		60	None	N.C.
61	OUT	PSC2_TXD		62	None	N.C.
63	INP	PSC1_RXD		64	None	N.C.
65	PWR	GND		66	PWR	GND
67	BIDIR	PSC1_RTS#		68	None	N.C.
69	None	N.C.		70	None	N.C.
71	None	N.C.		72	GND	GND
73	None	N.C.		74	INP	PSC3_CTS#
75	INP	PSC1_CTS#		76	None	N.C.
77	OUT	PSC1_TXD		78	INP	PSC3_RXD
79	None	N.C.		80	None	N.C.
81	PWR	VCC		82	PWR	VCC
83	INP	PSC0_RXD		84	None	N.C.
85	BIDIR	PSC0_RTS#		86	OUT	PSC3_TXD
87	None	N.C.		88	None	N.C.
89	None	N.C.		90	BIDIR	PSC3_RTS#
91	None	N.C.		92	None	N.C.
93	INP	PSC0_CTS#		94	None	N.C.
95	OUT	PSC0_TXD		96	None	N.C.
97	None	N.C.		98	None	N.C.
99	PWR	GND		100	PWR	GND

5.4 J4 (X4)

		J4				J4
Pin	Dir	Signal		Pin	Dir	Signal
1	PWR	GND		2	PWR	GND
3	PWR	5V_SB		4	BIDIR	DSPISCK
5	OUT	PS_ON#		6	INP	DSPI_DIN
7	INP	PWRBTN#		8	OUT	DSPI_DOUT
9	OUT	JTAG_nOE		10	OUT	LNKLED2
11	OUT	DSPI_CS0		12	OUT	ACTLED2
13	OUT	DSPI_CS2		14	None	N.C.
15	None	N.C.		16	BIDIR	I2C_SCL
17	PWR	VCC		18	PWR	VCC
19	INP	USB_nOVRC		20	None	N.C.
21	OUT	TOUT1		22	BIDIR	I2C_SDA
23	OUT	TOUT3		24	None	N.C.
25	OUT	TOUT0		26	None	N.C.
27	PWR	GND		28	None	N.C.
29	None	N.C.		30	None	N.C.
31	None	N.C.		32	None	N.C.
33	PWR	GND		34	PWR	GND

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35	None	N.C.		36	INP	J_FB_AD1
37	OUT	PSC2_RTS# (CANTX0)*		38	INP	J_FB_AD1
39	INP	PSC2_CTS# (CANRX0)*		40	OUT	FB_CS0#
41	None	N.C.		42	INP	TIN3
43	INP	TIN2 (CANRX1)*		44	None	N.C.
45	OUT	TOUT2 (CANTX1)*		46	None	N.C.
47	OUT	LNKLED1		48	None	N.C.
49	PWR	VCC		50	PWR	VCC
51	OUT	ACTLED1		52	None	N.C.
53	None	N.C.		54	None	N.C.
55	PWR	GND		56	OUT	USB1_nEN
57	INP	RX-_1		58	None	N.C.
59	INP	RX+_1		60	None	N.C.
61	OUT	TX-_1		62	OUT	USB2_nEN
63	OUT	TX+_1		64	None	N.C.
65	PWR	GND		66	PWR	GND
67	None	N.C.		68	OUT	USB3_nEN
69	None	N.C.		70	None	N.C.
71	PWR	GND		72	None	N.C.
73	None	N.C.		74	OUT	USB4_nEN
75	None	N.C.		76	None	N.C.
77	PWR	GND		78	None	N.C.
79	None	N.C.		80	None	N.C.
81	PWR	VCC		82	PWR	VCC
83	None	N.C.		84	None	N.C.
85	OUT	LAN_GND		86	None	N.C.
87	None	N.C.		88	None	N.C.
89	None	N.C.		90	None	N.C.
91	INP	RX-_0		92	None	N.C.
93	INP	RX+_0		94	None	N.C.
95	OUT	TX-_0		96	None	N.C.
97	OUT	TX+_0		98	INP	BUTTON_MRESET#
99	PWR	LAN_GND		100	PWR	GND

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6 ETX Connector Signal Description

6.1 Reset Input Signal

Connector	Signal Name	Type	Load	Description
J4-98	BUTTON_MRESET#	Input	10K p.u.	When pulled low, causes a Master Reset to the ETX board. Normally connected to a Push Button to a Push Button tied to ground on an ETX carrier board.

6.2 SPI Interface Signals

These signals are intended to connect to a standard “ZIGBEE SPI” interfaces.

Connector	Signal Name	Type	Load	Description
J4-11	DSPI_CS0	Output		In master mode, the DSPI_CS0 signal is peripheral chip select output that selects which slave device the current transmission is intended for. In slave mode, the SS signal is a slaveselect input signal that allows an SPI master to select the DSPI as the target for transmission.
J4-13	DSPI_CS2	Output		This signal provides a DSPI peripheral chip select that can be programmed to be active high or low
J4-9	DSPI_CS5	Output		This is a peripheral chip select output signal. When the DSPI is in master mode and the DMCR[PCSSE] bit is cleared, this signal is used to select which slave device the current transfer is intended for.
J4-6	DSPI_DIN	Input		The DSPI_DIN input provides the serial data to the DSPI and can be programmed to be sampled on the rising or falling edge of DSPISCK.
J4-8	DSPI_DOUT	Output		The DSPI_DOUT output provides the serial data from the DSPI and can be programmed to be driven

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				on the rising or falling edge of DSPISCK.
J4-4	DSPISCK	Bidir		DSPISCK is a serial communication clock signal. In master mode, the DSPI generates the DSPISCK. In slave mode, DSPISCK is an input from an external bus master.

6.3 I2C Interfaces Signals

Connector	Signal Name	Type	Load	Description
J4-22	I2C_SDA	Bidir	4.7K p.u.	This bi-directional open-drain signal is the clock signal for the I2C interface. It is either driven by the I2C module when the bus is in master mode or it becomes the clock input when the I2C is in slave mode.
J4-16	I2C_SCL	Bidir	4.7K p.u.	This bidirectional open-drain signal is the data input/output for the I2C interface.

6.4 Programmable Timer In/ Out Signals

Connector	Signal Name	Type	Load	Description
None None J4-43 J4-42	Tin0 Tin1 TIN2 TIN3	Input Input Input Input	4.7K p.u. 4.7K p.u. 4.7K p.u. 4.7K p.u.	TIN*n* can be programmed as clocks that cause events in the counter and prescalers. They can also cause captures on the rising edge, falling edge, or both edges.
J4-25 J4-21 J4-45 J4-23	TOUT0 TOUT1 TOUT2 TOUT3	Output Output Output Output		The programmable timer outputs, TOUT*n*, pulse or toggle on various timer events.

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6.5 FlexBus Signals (PC104 Interface)

Connector	Signal Name	Type	Load	Description
J2-85 J2-88 J2-87 J2-89 J2-92 J2-93 J2-95 J2-96 J2-15 J2-13 J2-11 J2-9 J2-7 J2-5 J2-3 J2-4	FB_AD16 FB_AD17 FB_AD18 FB_AD19 FB_AD20 FB_AD21 FB_AD22 FB_AD23 FB_AD24 FB_AD25 FB_AD26 FB_AD27 FB_AD28 FB_AD29 FB_AD30 FB_AD31	Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir		The AD[31:0] bus carries address and data. The full 32-bit address is always driven on the first clock of a bus cycle (address phase). The number of bytes used for data during the data phase is determined by the port size associated with the matching chip select. Only the Upper half word (Bits 16-31) is available off board.

Connector	Signal Name	Type	Load	Description
J2-39 J2-41 J2-43 J2-45 J2-47 J2-49 J2-53 J2-55 J2-57 J2-59 J2-61 J2-63 J2-65 J2-69 J2-71 J2-73 J2-75 J2-78 J2-77 J2-79	LA_FB_AD0 LA_FB_AD1 LA_FB_AD2 LA_FB_AD3 LA_FB_AD4 LA_FB_AD5 LA_FB_AD6 LA_FB_AD7 LA_FB_AD8 LA_FB_AD9 LA_FB_AD10 LA_FB_AD11 LA_FB_AD12 LA_FB_AD13 LA_FB_AD14 LA_FB_AD15 LA_FB_AD16 LA_FB_AD17 LA_FB_AD18 LA_FB_AD19	Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir		The Latched Address bits allow for direct addressing of memory mapped registers.

Connector	Signal Name	Type	Load	Description
J2-21* J2-23* J2-25* J4-40*	FB_CS3# FB_CS4# FB_CS5# FB_CS0#	Output Output Output Output	4.7K p.u. 4.7K p.u. 4.7K p.u. 4.7K p.u.	FB_CS[5:0]# are asserted to indicate which device is being selected. A particular chip select asserts when the transfer address is within the device's address space as defined in the base and mask address registers. Each chip select can be programmed for a base address location, masking

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				addresses, port size, burst-capability indication, wait-state generation, and internal/external termination.

*Reset clears all chip select programming; FBCS0 is the only chip select initialized out of reset. FBCS0 is also unique because it can function at reset as a global chip select that allows boot ROM to be selected at any defined address space. Port size and termination (internal vs. external) for boot FBCS0 are configured by the levels on AD[2:0] on the rising edge of RSTI.

Connector	Signal Name	Type	Load	Description
J2-19	MCF_OE#	Output	4.7K p.u.	The output enable signal is sent to the interfacing memory and/or peripheral to enable a read transfer. OE is asserted only when a chip select matches the current address decode. Active Low.
J2-17	MCF_RW#	Output	4.7K p.u.	The MCF547x/8x drives the R/W signal to indicate the direction of the current bus operation. It is driven high during read bus cycles and driven low during write bus cycles.
J2-29	MCF_TA#	Input	10K p.u.	The external system drives this input to terminate the bus transfer. For write cycles, the processor continues to drive data at least one clock after FBCS*x* is negated. During read cycles, the peripheral must continue to drive data until TA is recognized. The number of wait states is determined either by an internally programmed auto acknowledgement or the external TA input. If the external TA is used, the peripheral has total control over the number of wait states.
J2-60	SYSCLK	Output		System Clock active only when in a Reset condition.
J2-98	RESET#	Output (Open drain)	4.7K p.u.	Power on Reset, Push Button Reset, BDM reset. User should implement this as a system wide hardware reset pin.

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6.6 DMA Control Signals

Connector	Signal Name	Type	Load	Description
J2-20 J2-64	548X_DREQ0# 548X_DREQ1#	Input Input	4.7K p.u. 4.7K p.u.	These inputs are asserted by a peripheral device to request an operand transfer between that peripheral and memory by either channel 0 or 1 of the on-chip DMA module.
J2-22 J2-66	548X_DACK0# 548X_DACK1#	Output Output	4.7Kp.u. 4.7Kp.u.	These outputs are asserted to acknowledge that a DMA request has been recognized.

6.7 CPLD Signals

Connector	Signal Name	Type	Load	Description
J2-74	IORD#	Output	10K p.u.	Active low ISA READ cycle.
J2-76	IOWR#	Output	10K p.u.	Active low ISA WRITE cycle.
J2-48 J2-50 J2-54 J2-56	ISA_IRQ0 ISA_IRQ1 ISA_IRQ2 ISA_IRQ3	Input Input Input Input	10K p.u. 10K p.u. 10K p.u. 10K p.u.	offboard IRQx comes to the CPLD and generates IRQ6back at the processor
J2-82	AEN#	Output		Address enable
J2-42	BALE	Output		Address latch enable
J2-81	CHRDY#	Input	10K p.u.	Channel ready
J4-9	JTAG_nOE	Output		Active low output during onboard CPLD code field updates.

6.8 Video Display Signals

Connector	Signal Name	Type	Load	Description
J3-3	CRT_RED	Output		Analog Red Current Output. Requires external 75 Ohm pull downs if CRT is implemented.
J3-6	CRT_GREEN	Output		Analog Green Current Output. Requires external 75 Ohm pull downs if CRT is implemented.
J3-4	CRT_BLUE	Output		Analog Blue Current output. Requires external 75 Ohm pull downs if CRT is implemented.
J3-7	CRT_VSYNC	Output		CRT Vertical Sync
J3-5	CRT_HSYNC	Output		CRT Horizontal Sync or Composite Sync depending on CCR65[0]: 0 =CRT Horizontal Sync

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				1= Composite sync
J3-8	DDC_SCL	Bidir	4.7K p.u.	General Purpose Register USR1/DDC2/I2C Clock. . Can be used to select different test modes.
J3-10	DDC_SDA	Bidir	4.7K p.u.	General Purpose Register USR1/DDC2/I2C Data. Can be used to select different test modes.
J3-56	PCI_VID_ POWERDOWN#	Input	4.7K p.u.	Power Down Mode Enable. Active Low.
J3-9	VID_GND	Output		Video Ground is a signal that is connected to Digital Ground through a ferrite bead for noise reduction.

6.9 Flat Panel Display Signals

Connector	Signal Name	Type	Load	Description
J3-43	TMDS_IDCK	Output		Memory Clock In (~EXCKEN=0) or LVDSCLK Out (~EXCKEN=1) LVDSCLK is a free running clock, which can be used to drive an LVDS transmitter for DSTN panels.
J3-19 J3-17 J3-20 J3-18 J3-11 J3-13 J3-32 J3-30 J3-23 J3-25 J3-26 J3-24 J3-37 J3-35 J3-38 J3-36 J3-29 J3-31	FP_DATA0 FP_DATA1 FP_DATA2 FP_DATA3 FP_DATA4 FP_DATA5 FP_DATA8 FP_DATA9 FP_DATA10 FP_DATA11 FP_DATA12 FP_DATA13 FP_DATA16 FP_DATA17 FP_DATA18 FP_DATA19 FP_DATA20 FP_DATA21	Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output		These 18 data outputs represent the color bits to a flat panel display from the SM712 Video Controller.
J3-14	FP_DISPLAY_EN	Output		M-signal of Display Enable. This signal is used to indicate the active horizontal display time. FPR3E[7] is used to select 1=M-Signal 0=Display Enable
J3-44	FP_EN	Output		Flat Panel Enable. This signal needs to become

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				active after all panel voltages, Clocks, and data are supplied. This signal also needs to become inactive before any panel voltages or control signals are removed. FP_EN is part of the VESA FPDI-1B specification.
J3-47	FP_VBIASEN	Output		Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power.
J3-46	FP_VDDEN	Output		Flat Panel VDD Enable. This signal is used to control LCD logic power.
J3-45	FP_HSYNC	Output		DSTN LCD:Line Pulse TFT LCD: LCD Horizontal sync.
J3-42	FP_VSYNC	Output		DSTN LCD:Frame Pulse TFT LCD: LCD Vertical sync.

6.10 PCI Bus Signals

Connector	Signal Name	Type	Load	Description
J1-23	PCI_AD0	Bidir		The PCI_AD[31:0] lines are a time-multiplexed address data bus. The address is presented on the bus during the address phase while the data is presented on the bus during one or more data phases.
J1-25	PCI_AD1	Bidir		
J1-26	PCI_AD2	Bidir		
J1-28	PCI_AD3	Bidir		
J1-27	PCI_AD4	Bidir		
J1-30	PCI_AD5	Bidir		
J1-29	PCI_AD6	Bidir		
J1-32	PCI_AD7	Bidir		
J1-33	PCI_AD8	Bidir		
J1-34	PCI_AD9	Bidir		
J1-37	PCI_AD10	Bidir		
J1-39	PCI_AD11	Bidir		
J1-41	PCI_AD12	Bidir		
J1-43	PCI_AD13	Bidir		
J1-45	PCI_AD14	Bidir		
J1-47	PCI_AD15	Bidir		
J1-69	PCI_AD16	Bidir		
J1-71	PCI_AD17	Bidir		
J1-74	PCI_AD18	Bidir		
J1-73	PCI_AD19	Bidir		
J1-75	PCI_AD20	Bidir		
J1-78	PCI_AD21	Bidir		
J1-77	PCI_AD22	Bidir		
J1-79	PCI_AD23	Bidir		
J1-81	PCI_AD24	Bidir		
J1-85	PCI_AD25	Bidir		
J1-86	PCI_AD26	Bidir		
J1-89	PCI_AD27	Bidir		
J1-87	PCI_AD28	Bidir		
J1-90	PCI_AD29	Bidir		

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J1-91 J1-94	PCI_AD30 PCI_AD31	Bidir Bidir		
J1-31 J1-49 J1-70 J1-82	PCI_C/BE0# PCI_C/BE1# PCI_C/BE2# PCI_C/BE3#	Bidir Bidir Bidir Bidir	15K p.u. 15K p.u. 15K p.u. 15K p.u	The PCI_C/BE[3:0]# lines are time multiplexed. The PCI command is presented during the address phase and the byte enables are presented during the data phase. Active Low.
J1-53	PCI_PAR	Bidir	15K p.u.	The PCIPAR signal indicates the parity of data on the PCI_AD[31:0] and PCI_C/BE[3:0] lines.
J1-55	PCI_PERR#	Bidir	15K p.u.	The PCIPERR signal is asserted when a data phase parity error is detected if enabled. Active Low.
J1-60	PCI_DEVSEL#	Output	15K p.u.	The DEVSEL# signal is asserted active low when the MCF547x/8x decodes that it is the target of a PCI transaction from the address presented on the PCI bus during the address phase. Active Low.
J1-65	PCI_FRAME#	Bidir	15K p.u.	The FRAME# signal is asserted by a PCI initiator to indicate the beginning of a transaction. It is negated when the initiator is ready to complete the final data phase. Active Low.
J1-63	PCI_IRDY#	Bidir	15K p.u.	The IRDY# signal is asserted to indicate that the PCI initiator is ready to transfer data. During a write operation, assertion indicates that the master is driving valid data on the bus. During a read operation, assertion indicates that the master is ready to accept data. Active Low.
J1-61	PCI_TRDY#	Bidir	15K p.u.	The PCI_TRDY# signal is asserted by the currently addressed target to indicate that it is ready to complete the current data phase. Active Low.
J1-59	PCI_LOCK#	Bidir	15K p.u.	This signal is used to manage resource locks

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				on the PCI bus. Active Low.
J1-54	PCI_SERR#	Bidir	15K p.u.	The PCISERR signal, if enabled, is asserted when an address phase parity error is detected. Active Low.
J1-64	PCI_STOP#	Bidir	15K p.u.	This signal is asserted by the currently addressed target to indicate that it wishes to stop the current transaction. Active Low.
J1-93	PCI_RESET#	Output	15K p.u.	The PCIRESET signal is asserted active low by MCF548*x* to reset the PCI bus. This signal is asserted after the MCF547x/8x` is reset and must be negated to enable usage of the PCI bus. Active Low.
J1-40	M66EN	Input		Sense line for CPLD to detect 66MHZ PCI Cards.
J1-95 J1-96	INTC# INTD#	Input	4.7K p.u.	These two interrupts are tied together and connected to IRQ5# on the MCF547x/8x. Active Low.
J1-97 J1-98	INTA# INTB#	Input	4.7K p.u.	These two interrupts are tied together and connected to IRQ7# on the MCF547x/8x. Active Low.

6.11 Ethernet Signals

Connector	Signal Name	Type	Load	Description
J4-93 J4-91	RX+_0 RX-_0	Input Input	50 p.u. 50 p.u.	Port 1 Receive pair. Differential data from the media is received on this pair.
J4-97 J4-95	TX+_0 TX-_0	Output	50 p.u. 50 p.u.	Port 1 Transmit pair. Differential data is transmitted to the media on this pair.
J4-47	LNKLED1	Output		Port 1 Link Integrity LED. This signal indicates the link status of the PHY. It is driven low when the link to the PHY is good.
J4-51	ACTLED1	Output		Port 1 Activity LED. This signal is driven low for approximately 80 ms. Each time there is receive or transmit activity while in the link pass state.

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J4-85 J4-99	LAN_GND LAN_GND	Power Power		These signals are connected to Digital Ground through a ferrite bead for noise reduction.
J4-59 J4-57	RX+_1 RX-_1	Input Input	50 p.u. 50 p.u.	Port 2 Receive pair. Differential data from the media is received on this pair.
J4-63 J4-61	TX+_1 TX-_1	Output Output	50 p.u. 50 p.u.	Port 2 Transmit pair. Differential data is transmitted to the media on this pair.
J4-10	LNKLED2	Output		Port 2 Link Integrity LED. This signal indicates the link status of the PHY. It is driven low when the link to the PHY is good.
J4-12	ACTLED2	Output		Port 2 Activity LED. This signal is driven low for approximately 80 ms. Each time there is receive or transmit activity while in the link pass state.

6.12 Serial Port Signals

There are 4 Programmable Serial Controller ports and they all function in the same way.

Connector	Signal Name	Type	Load	Description
J3-95 J3-77 J3-61 J3-86	PSC0_TXD PSC1_TXD PSC2_TXD PSC3_TXD	Output Output Output Output		PSCx_TXD are the transmitter serial data outputs for the PSC modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. The PSCx_TXD pins can be programmed to be driven low (break status) by a command.
J3-83 J3-63 J3-59 J3-78	PSC0_RXD PSC1_RXD PSC2_RXD PSC3_RXD	Input Input Input Input		PSCx_RXD are the receiver serial data inputs for the PSC modules. When the PSC clock is stopped for power-down mode, any transition on the pins restarts them.
J3-93 J3-75 J4-39 J3-74	PSC0_CTS# PSC1_CTS# PSC2_CTS# PSC3_CTS#	Input Input Input Input	4.7Kp.u.	These signals either operate as the clear to send input signals in UART mode or the bit clock input signals in modem modes and IrDA modes. In MIR and FIR mode, the frequency is a

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				multiple of the input bit clock frequency, and the bit clock frequency should be within +/- 0.1% and +/- 0.01% of the ideal one, respectively.
J3-85 J3-67 J4-37 J3-90	PSC0_RTS# PSC1_RTS# PCS2_RTS# PSC3_RTS#	Bidir Bidir Bidir Bidir	4.7Kp.u.	The PSCx_RTS signals act as transmitter request to send (RTS) outputs in UART mode, the frame sync input in modem8 and modem16 modes or the RTS output (which acts as frame sync) in AC97 modem mode.

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6.13 USB Signals

There are 4 Universal Serial Bus Controller ports and they all function in the same way.

Connector	Signal Name	Type	Load	Description
J1-88 J1-76 J1-92 J1-80 J1-66 J1-58 J1-72 J1-62	USB_DP1 USB_DM1 USB_DP2 USB_DM2 USB_DP3 USB_DM3 USB_DP4 USB_DM4	Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir	15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d.	D+ and D- Analog data connection for USB downstream ports. NOTE: Differential routing is required for these traces offboard.
J4-19	USB1_nOVRC	Input	15K p.u.	Overcurrent sense input for the USB downstream ports. (Digital). Push-pull; TTL with hysteresis; 5V Tolerant.
J4-56 J4-62 J4-68 J4-74	USB1_nEN USB2_nEN USB3_nEN USB4_nEN	Bidir O.D. Bidir O.D. Bidir O.D. Bidir O.D.	15K p.u. 15K p.u. 15K p.u. 15K p.u.	

6.14 Reserved Pins:

Connector	Signal Name	Type	Load	Description
J4-36 J4-38	J_FB_AD1 J_FB_AD1	Input Input		Reserved for future use.
J4-67 J4-69 J4-73 J4-75 J4-79 J4-83 J4-29 J4-31	USB_DP1 USB_DM1 USB_DP2 USB_DM2 USB_DP3 USB_DM3 USB_DP4 USB_DM4	Bidir Bidir Bidir Bidir Bidir Bidir Bidir Bidir	15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d. 15K p.d.	These pins provide Backwards compatibility to older versions of the Mini-ITX baseboard. These signals are Not connected on board revisions 301 and higher.
J4-58 J4-64 J4-70 J4-76	USB1_nOVRC USB2_nOVRC USB3_nOVRC USB4_nOVRC	Input Input Input Input	15K p.u. 15K p.u. 15K p.u. 15K p.u.	These pins provide Backwards compatibility to older versions of the Mini-ITX baseboard. These signals are Not connected on board revisions 301 and higher.

6.15 VCC 5V

J1-19,J1-51,J1-83,J1-20,J1-52,J1-84,J2-51,J2-83 J2-52,J2-84,J3-39,J3-53,J3-81,J3-40,J3-82,J4-17 J4-49,J4-81,J4-18,J4-50,J4-82	Input PWR	5V power input.

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6.16 3.3V:

J1-12,J1-16,J1-24	Output PWR	3.3V power output. Maximum load 500mA per ETX specification.

6.17 Ground

J1-1,J1-5,J1-35,J1-67,J1-99,J1-2,J1-6,J1-36,J1-68 J1-100,J2-1,J2-35,J2-67,J2-99,J2-2,J2-36,J2-68 J2-100,J3-1,J3-15,J3-21,J3-27,J3-33,J3-65,J3-99 J3-2,J3-16,J3-22,J3-28,J3-34,J3-54,J3-66,J3-72 J3-100,J4-1,J4-27,J4-33,J4-55,J4-65,J4-71,J4-77 J4-2,J4-34,J4-66,J4-100	PWR	VCC

6.18 Not Connected

J1-7,J1-15,J1-17,J1-21,J1-57,J1-8,J1-14,J1-18 J1-22,J1-38,J1-42,J1-44,J1-46,J1-48,J1-50,J1-56 J2-27,J2-31,J2-33,J2-37,J2-91,J2-97,J2-6,J2-8 J2-10,J2-12,J2-14,J2-16,J2-18,J2-24,J2-26,J2-28 J2-30,J2-32,J2-34,J2-38,J2-40,J2-44,J2-46,J2-58 J2-62,J2-70,J2-72,J2-80,J2-86,J2-90,J2-94,J3-41 J3-49,J3-51,J3-55,J3-57,J3-69,J3-71,J3-73,J3-79 J3-87,J3-89,J3-91,J3-97,J3-48,J3-50,J3-52,J3-58 J3-60,J3-62,J3-64,J3-68,J3-70,J3-76,J3-80,J3-84 J3-88,J3-92,J3-94,J3-96,J3-98,J4-15,J4-35,J4-41 J4-53,J4-87,J4-89,J4-14,J4-20,J4-24,J4-26,J4-28 J4-30,J4-32,J4-44,J4-46,J4-48,J4-52,J4-54,J4-60 J4-72,J4-78,J4-80,J4-84,J4-86,J4-88,J4-90,J4-92 J4-94,J4-96	None	N.C.

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7 Differences: ETX Standard vs. ETX Fire Engine.

In order to accommodate the rich feature set of the Freescale Coldfire processor, compromises were required with regard to the ETX standard Pinout. Generally, when a signal defined by the ETX standard was not used by the MCF7x/8x, it was left unconnected. However, when a signal defined by the MCF7x/8x did not appear in the ETX standard, it was necessary to re-define certain signal names to accommodate the MCF7x/8x. The following tables show these differences. The shaded signal names define the specific differences.

7.1 X1 Connector:

	ETX STD.	LOGIC		ETX STD.	LOGIC
	X1	J1		X1	J1
Pin	Signal	Signal	Pin	Signal	Signal
1	GND	GND	2	GND	GND
3	PCICLK3	PCICLK3	4	PCICLK4	PCICLK4
5	GND	GND	6	GND	GND
7	PCICLK1	N.C.	8	PCICLK2	N.C.
9	REQ3#	REQ3#	10	GNT3#	GNT3#
11	GNT2#	GNT2#	12	3V	3V
13	REQ2#	REQ2#	14	GNT1#	N.C.
15	REQ1#	N.C.	16	3V	3V
17	GNT0#	N.C.	18	RESERVED	N.C.
19	VCC	VCC	20	VCC	VCC
21	SERIRQ	N.C.	22	REQ0#	N.C.
23	AD0	AD0	24	3V	3V
25	AD1	AD1	26	AD2	AD2
27	AD4	AD4	28	AD3	AD3
29	AD6	AD6	30	AD5	AD5
31	CBE0#	CBE0#	32	AD7	AD7
33	AD8	AD8	34	AD9	AD9
35	GND	GND	36	GND	GND
37	AD10	AD10	38	AUXAL	N.C.
39	AD11	AD11	40	MIC	M66EN
41	AD12	AD12	42	AUXAR	N.C.
43	AD13	AD13	44	ASVCC	N.C.
45	AD14	AD14	46	SNDL	N.C.
47	AD15	AD15	48	ASGND	N.C.
49	CBE1#	CBE1#	50	SNDR	N.C.
51	VCC	VCC	52	VCC	VCC
53	PAR	PAR	54	SERR#	SERR#
55	PERR#	PERR#	56	RESERVED	N.C.
57	PME#	N.C.	58	USB2#	USB_DM3
59	LOCK#	LOCK#	60	DEVSEL#	DEVSEL#
61	TRDY#	TRDY#	62	USB3#	USB_DM4
63	IRDY#	IRDY#	64	STOP#	STOP#

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65	FRAME#	FRAME#	66	USB2	USB_DP3
67	GND	GND	68	GND	GND
69	AD16	AD16	70	CBE2#	CBE2#
71	AD17	AD17	72	USB3	USB_DP4
73	AD19	AD19	74	AD18	AD18
75	AD20	AD20	76	USB0#	USB_DM1
77	AD22	AD22	78	AD21	AD21
79	AD23	AD23	80	USB1#	USB_DM2
81	AD24	AD24	82	CBE3#	CBE3#
83	VCC	VCC	84	VCC	VCC
85	AD25	AD25	86	AD26	AD26
87	AD28	AD28	88	USB0	USB_DP1
89	AD27	AD27	90	AD29	AD29
91	AD30	AD30	92	USB1	USB_DP2
93	PCIRST#	PCIRST#	94	AD31	AD31
95	INTC#	INTC#	96	INTD#	INTD#
97	INTA#	INTA#	98	INTB#	INTB#
99	GND	GND	100	GND	GND

X1 – 40 is defined as an audio “Microphone input”. Logic Product Development has re-assigned this pin to provide a “66MHZ PCI board detect” which is not available on the ETX Standard.

7.2 X2 connector:

	ETX STD X2	LOGIC J2		ETX STD X2	LOGIC J2
Pin	Signal	Signal	Pin	Signal	Signal
1	GND	GND	2	GND	GND
3	SD14	FB_AD30	4	SD15	FB_AD31
5	SD13	FB_AD29	6	MASTER#	N.C.
7	SD12	FB_AD28	8	DREQ7	N.C.
9	SD11	FB_AD27	10	DACK7#	N.C.
11	SD10	FB_AD26	12	DREQ6	N.C.
13	SD9	FB_AD25	14	DACK6#	N.C.
15	SD8	FB_AD24	16	DREQ5	N.C.
17	MEMW#	MCF_RW#	18	DACK5#	N.C.
19	MEMR#	MCF_OE#	20	DREQ0	548X_DREQ0#
21	LA17	FB_CS3#	22	DACK0#	548X_DACK0#
23	LA18	FB_CS4#	24	IRQ14	N.C.
25	LA19	FB_CS5#	26	IRQ15	N.C.
27	LA20	N.C.	28	IRQ12	N.C.
29	LA21	MCF_TA#	30	IRQ11	N.C.
31	LA22	N.C.	32	IRQ10	N.C.
33	LA23	N.C.	34	IO16#	N.C.
35	GND	GND	36	GND	GND

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37	SBHE#	N.C.	38	M16#	N.C.
39	SA0	LA_FB_AD0	40	OSC	N.C.
41	SA1	LA_FB_AD1	42	BALE	BALE
43	SA2	LA_FB_AD2	44	TC	N.C.
45	SA3	LA_FB_AD3	46	DACK2#	N.C.
47	SA4	LA_FB_AD4	48	IRQ3	ISA_IRQ0
49	SA5	LA_FB_AD5	50	IRQ4	ISA_IRQ1
51	VCC	VCC	52	VCC	VCC
53	SA6	LA_FB_AD6	54	IRQ5	ISA_IRQ2
55	SA7	LA_FB_AD7	56	IRQ6	ISA_IRQ3
57	SA8	LA_FB_AD8	58	IRQ7	N.C.
59	SA9	LA_FB_AD9	60	SYSCLK	SYSCLK
61	SA10	LA_FB_AD10	62	REFSH#	N.C.
63	SA11	LA_FB_AD11	64	DREQ1	548X_DREQ1
65	SA12	LA_FB_AD12	66	DACK1#	548X_DACK1#
67	GND	GND	68	GND	GND
69	SA13	LA_FB_AD13	70	DREQ3	N.C.
71	SA14	LA_FB_AD14	72	DACK3#	N.C.
73	SA15	LA_FB_AD15	74	IOR#	IORD#
75	SA16	LA_FB_AD16	76	IOW#	IOWR#
77	SA18	LA_FB_AD18	78	SA17	LA_FB_AD17
79	SA19	LA_FB_AD19	80	SMEMR	N.C.
81	IOCHRDY	CHRDY#	82	AEN	AEN
83	VCC	VCC	84	VCC	VCC
85	SD0	FB_AD16	86	SMEMW#	N.C.
87	SD2	FB_AD18	88	SD1	FB_AD17
89	SD3	FB_AD19	90	NOWS#	N.C.
91	DREQ2	N.C.	92	SD4	FB_AD20
93	SD5	FB_AD21	94	IRQ9	N.C.
95	SD6	FB_AD22	96	SD7	FB_AD23
97	IOCHK#	N.C.	98	RSTDRV	RESET#
99	GND	GND	100	GND	GND

ETX standard:	ETX Fire Engine:
X2 - 21 = LA17	FBCS3#
X2 – 23 = LA18	FBCS4#
X2 – 25 = LA19	FBCS5#
X2 – 29 = LA21	MCF_TA

The ETX Fire Engine has re-assigned these pins in order to better utilize the features of the MCF7x/8x FlexBus. FBCS3#, FBCS4# and FBCS5# are “Chip selects” for accessing external devices.

MCF_TA is a “Transfer Acknowledge”
The external device drives this input to terminate the bus transfer. For write cycles, the processor continues to drive data at least one clock after FBCSx is negated. During read cycles, the peripheral must continue to drive data until TA is recognized. The number of wait states is determined either by an internally programmed auto acknowledgement or the external TA input. If the external TA is used, the peripheral has total control over the number of wait states

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7.3 X3 Connector:

	ETX STD1 X3	ETX STD2 X3	LOGIC J3		ETX ST1 X3	ETX ST2 X3	LOGIC J3
Pin	Signal	Signal	Signal	Pin	Signal	Signal	Signal
1	GND	GND	GND	2	GND	GND	GND
3	R	R	R	4	B	B	B
5	HSY	HSY	HSY	6	G	G	G
7	VSY	VSY	VSY	8	DDCK	DDCK	DDC_SCL
9	DETECT#	DETECT#	VID_GND	10	DDDA	DDDA	DDC_SDA
11	LCDDO16	B4	FP_DATA4	12	LCDDO18	SHFCLK	N.C.
13	LCDDO17	B5	FP_DATA5	14	LCDDO19	EN	N.C.
15	GND	GND	GND	16	GND	GND	GND
17	LCDDO13	B1	FP_DATA1	18	LCDDO15	B3	FP_DATA3
19	LCDDO12	B0	FP_DATA0	20	LCDDO14	B2	FP_DATA2
21	GND	GND	GND	22	GND	GND	GND
23	LCDDO8	G2	FP_DATA10	24	LCDDO11	G5	FP_DATA13
25	LCDDO9	G3	FP_DATA11	26	LCDDO10	G4	FP_DATA12
27	GND	GND	GND	28	GND	GND	GND
29	LCDDO4	R4	FP_DATA20	30	LCDDO7	G1	FP_DATA9
31	LCDDO5	R5	FP_DATA21	32	LCDDO6	G0	FP_DATA8
33	GND	GND	GND	34	GND	GND	GND
35	LCDDO1	R1	FP_DATA17	36	LCDDO3	R3	FP_DATA19
37	LCDDO0	R0	FP_DATA16	38	LCDDO2	R2	FP_DATA18
39	VCC	VCC	VCC	40	VCC	VCC	VCC
41	JILI_DAT	JILI_DAT	N.C.	42	LTGIO0	VSYNC	FP_VSYNC
43	JILI_CLK	JILI_CLK	TMDS_IDCK	44	BLON#	BLON#	FP_EN
45	BIASON	HSYNC	FP_HSYNC	46	DIGON	DIGON	FP_VDDEN
47	COMP	COMP	FP_BIASEN	48	Y	Y	N.C.
49	SYNC	SYNC	N.C.	50	C	C	N.C.
51	LPT/FLPY#	LPT/FLPY#	N.C.	52	RESERVED	RESERVED	N.C.
53	VCC	VCC	VCC	54	GND	GND	GND
55	STB#	RESERVED	N.C.	56	AFD#	DENSEL	PCI_VID_PWRDN#
57	RESERVED	RESERVED	N.C.	58	PD7	RESERVED	N.C.
59	IRRX	IRRX	PSC2_RXD	60	ERR#	HDSEL	N.C.
61	IRTX	IRTX	PSC2_TXD	62	PD6	RESERVED	N.C.
63	RXD2	RXD2	PSC1_RXD	64	INIT#	DIR#	N.C.
65	GND	GND	GND	66	GND	GND	GND
67	RTS2#	RTS2#	PSC1_RTS#	68	PD5	RESERVED	N.C.
69	DTR2#	DTR2#	N.C.	70	SLIN#	STEP#	N.C.
71	DCD2#	DCD2#	N.C.	72	PD4	DSKCHG	GND
73	DSR2#	DSR2#	N.C.	74	PD3	RDATA#	PSC3_CTS#
75	CTS2#	CTS2#	PSC1_CTS#	76	PD2	WP#	N.C.
77	TXD2#	TXD2#	PSC1_TXD	78	PD1	TRK0#	PSC3_RXD
79	RI2#	RI2#	N.C.	80	PD0	INDEX#	N.C.
81	VCC	VCC	VCC	82	VCC	VCC	VCC
83	RXD1	RXD1		84	ACK#	DRV	N.C.

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85	RTS1#	RTS1#	PSC0_RTS#	86	BUSY#	MOT	PSC3_TXD
87	DTR1#	DTR1#	N.C.	88	PE	WDATA#	N.C.
89	DCD1#	DCD1#	N.C.	90		WGATE#	PSC3_RTS#
91	DSR1#	DSR1#	N.C.	92	MSCLK	MSCLK	N.C.
93	CTS1#	CTS1#	PSC0_CTS#	94	MSDAT	MSDAT	N.C.
95	TXD1	TXD1	PSC0_TXD	96	KBCLK	KBCLK	N.C.
97	RI1#	RI1#	N.C.	98	KBDAT	KBDAT	N.C.
99	GND	GND	GND	100	GND	GND	GND

ETX standard:	ETX Fire Engine:
X3 - 43 = JILI_CLK	TMDS_IDCK
X3 – 47 = COMP	FP_BIASEN
X3 – 44 = BLON#	FP_EN
X3 – 46 = DIGON	FP_VDDEN
X3 – 56 = DENSEL	PCI_VID_PWRDN#

These pins were re-assigned to provide necessary signaling for Flat Panel Interfaces that was not available in the ETX standard.

ETX standard:	ETX Fire Engine:
X3 - 72 = DSKCHG	GND
X3 – 74 = RDATA#	PSC3_CTS#
X3 – 78 = TRK0#	PSC3_RXD
X3 – 86 = MOT	PSC3_TXD
X3 – 90 = WGATE#	PSC3_RTS#

These pins were re-assigned to provide and additional Programmable Serial Controller which was not available in the ETX standard.

7.4 X4 Connector:

	ETX STD X4	LOGIC J4		ETX STD X4	LOGIC J4
Pin	Signal	Signal	Pin	Signal	Signal
1	GND	GND	2	GND	GND
3	5V_SB	5V_SB	4	PWGIN	DSPISCK
5	PS_ON	PS_ON	6	SPEAKER	DSPI_DIN
7	PWRBTN#	PWRBTN#	8	BATT	DSPI_DOUT
9	KBINH	JTAG_nOE	10	LILED	LNKLED2
11	RSMRST#	DSPI_CS0	12	ACTLED	ACTLED2
13	ROMKBCS	DSPI_CS2	14	SPEEDLED	N.C.
15	EXT_PRG	N.C.	16	12CLK	I2C_SCL
17	VCC	VCC	18	VCC	VCC
19	OVCR#	USB_nOVRC	20	GPCS#	N.C.
21	EXTSMI#	TOUT1	22	I2DAT	12CSDA
23	SMBCLK	TOUT3	24	SMBDATA	SMBDATA
25	SIDE_CS3#	TOUT0	26	SMBALRT#	N.C.

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27	SIDE_CS1#	GND	28	DASP_S	N.C.
29	SIDE_A2	N.C.	30	PIDE_CS3#	N.C.
31	SIDE_A0	N.C.	32	PIDE_CS1#	N.C.
33	GND	GND	34	GND	GND
35	PDIAG_S	N.C.	36	PIDE_A2	J_FB_AD1
37	SIDE_A1	CANTX0	38	PIDE_A0	J_FB_AD1
39	SIDE_INTRQ	CANRX0	40	PIDE_A1	FB_CS0#
41	BATLOW#	N.C.	42	GPE1#	TIN3
43	SIDE_AK#	CANRX1	44	PIDE_INTRQ	N.C.
45	SIDE_RDY	CANTX1	46	PIDE_AK#	N.C.
47	SIDE_IOR#	LNKLED1	48	PIDE_RDY	N.C.
49	VCC	VCC	50	VCC	VCC
51	SIDE_IOW#	ACTLED1	52	PIDE_IOR#	N.C.
53	SIDE_DRQ	N.C.	54	PIDE_IOW#	N.C.
55	SIDE_D15	GND	56	PIDE_DRQ	USB1_nEN
57	SIDE_D0	RX-_1	58	PIDE_D15	N.C.
59	SIDE_D14	RX+_1	60	PIDE_D0	N.C.
61	SIDE_D1	TX-_1	62	PIDE_D14	USB2_nEN
63	SIDE_D13	TX+_1	64	PIDE_D1	N.C.
65	GND	GND	66	GND	GND
67	SIDE_D2	N.C.	68	PIDE_D13	USB3_nEN
69	SIDE_D12	N.C.	70	PIDE_D2	N.C.
71	SIDE_D3	GND	72	PIDE_D12	N.C.
73	SIDE_D11	N.C.	74	PIDE_D3	USB4_nEN
75	SIDE_D4	N.C.	76	PIDE_D11	N.C.
77	SIDE_D10	GND	78	PIDE_D4	N.C.
79	SIDE_D5	N.C.	80	PIDE_D10	N.C.
81	VCC	VCC	82	VCC	VCC
83	SIDE_D9	N.C.	84	PIDE_D5	N.C.
85	SIDE_D6	LAN_GND	86	PIDE_D9	N.C.
87	SIDE_D8	N.C.	88	PIDE_D6	N.C.
89	GPE2#	N.C.	90	CBLID_P#	N.C.
91	RXD#	RX-_0	92	PIDE_D8	N.C.
93	RXD	RX+_0	94	SIDE_D7	N.C.
95	TXD#	TX-_0	96	PIDE_D7	N.C.
97	TXD	TX+_0	98	HDRST#	BUTTON_MRESET#
99	GND	LAN_GND	100	GND	GND

ETX standard:	ETX Fire Engine:
X4 – 11 = RSMRST#	DSPI_CS0
X4 – 13 = ROMKBCS	DSPI_CS2
X4 – 4 = PWGIN	DSPISCK
X4 – 6 = SPEAKER	DSPI_DIN
X4 – 8 = BATT	DSPI_DOUT

These pins are assigned to accommodate the “DMA Serial Peripheral Interface” that is available from the MCF7x/8x. There were no pins available for this interface in the ETX standard.

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ETX standard:	ETX Fire Engine:
X4 - 47 = SIDE_IOR#	LNKLED1
X4 – 51 = SIDE_IOW#	ACTLED1
X4 – 55 = SIDE_D15	GND
X4 – 57 = SIDE_D0	RX-_1
X4 – 59 = SIDE_D14	RX+_1
X4 – 61 = SIDE_D1	TX-_1
X4 – 63 = SIDE_D13	TX+_1
X4 – 10 = LILED	LNKLED2
X4 – 12 = ACTLED	ACTLED2
X4 – 85 = SIDE_D6	LAN_GND

The ETX standard provides for one Ethernet controller. The MCF7x/8x processor provides for two Ethernet controllers. The above pins are assigned to provide external connectivity for the second Ethernet Controller.

ETX standard:	ETX Fire Engine:
X4 - 37 = SIDE_A1	CANTX0
X4 – 39 = SIDE_INTRQ	CANRX0
X4 – 43 = SIDE_AK#	CANRX1
X4 – 45 = SIDE_RDY	CANTX1

The above pins are assigned to accommodate the two available CAN controllers from the MCF7x/8x. The ETX standard has no other provisions for these pins.

ETX standard:	ETX Fire Engine:
X4 - 36 = PIDE_A2	J_FB_AD1
X4 – 38 = PIDE_A0	J_FB_AD1
X4 – 40 = PIDE_A1	FB_CS0#

These signals are assigned to provide a future capability for accessing off-board memories.

ETX standard:	ETX Fire Engine:
X4 - 42 = GPE1#	TIN3
X4 – 21 = EXTSMI#	TOUT1
X4 – 23 = SMBCLK	TOUT3
X4 – 25 = SIDE_CS3#	TOUT0
X4 – 27 = SIDE_CS1#	GND

These signals are assigned to provide capability to externally make use of the Programmable timers available on the MCF547x/8x.

ETX standard:	ETX Fire Engine:
X4 – 56 = PIDE_DRQ	USB1_nEN
X4 – 62 = PIDE_D14	USB2_nEN
X4 – 68 = PIDE_D13	USB3_nEN
X4 – 74 = PIDE_D3	USB4_nEN

These pins are used as USB Host port enable pins.

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8 General Purpose I/O

Many of the MCF547x/8x pins whose primary function is to serve as the external interface to off-chip resources also may be used for general-purpose digital I/O (GPIO) access and for one or two secondary functions. The Primary reference for this subject is the Freescale MCF547X or MCF548X Reference Manual. This section will present which pins can be interchanged between their standard function and General Purpose I/O. For the methods on how this is accomplished, please consult the appropriate Reference Manual.

The table on the following page, taken from the MCF548x Preliminary Freescale Reference Manual, shows the signal pinouts along with their functional groupings. As can be seen, the pins can have as many as 4 functions.

Exception: The ETX Fire Engine has dedicated the pin assignments for the CAN interface when used with LogicPD's Mini-ITX baseboard even though the CAN signals can optionally be assigned to several possibilities in the processor. This was a wiring requirement for the X4 connector. The dedicated assignments are:

CANTX1 = DSPICS2
CANRX1 = TIN2
CANTX0 = PSC2RTS
CANRX0 = PSC2CTS

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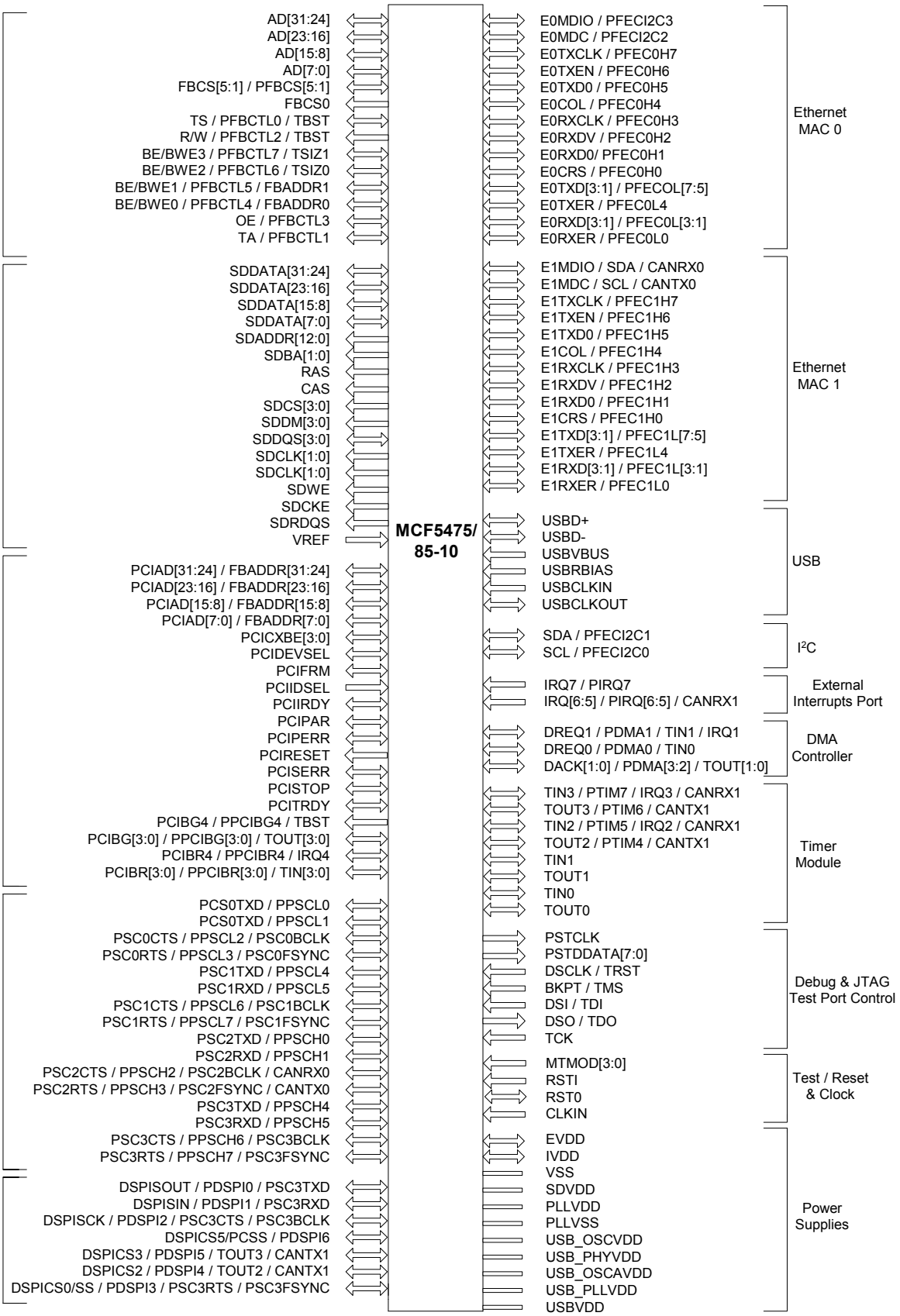

Figure 8.1: GPIO Table

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9 Mechanical Specifications

9.1 ETX Footprint

The Fire Engine complies with the following ETX Footprint:

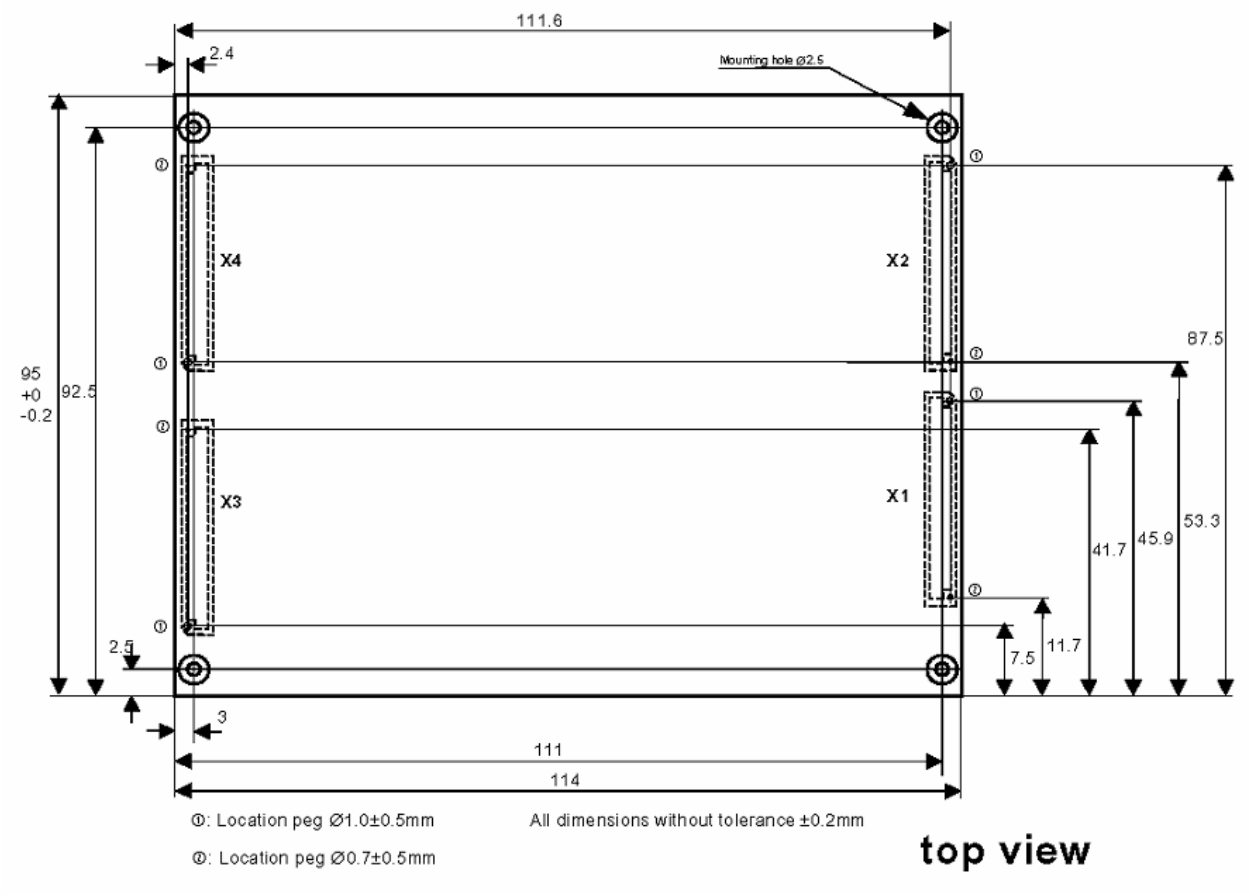

Figure 9.1: Fire Engine ETX Footprint Mechanical Drawing

Note: Dimensions are NOT the same for the mating ETX footprint for the baseboard. Specifically, the footprints for the top and bottom side connectors have different alignment pin locations. Please refer to Section 9.2 for the mechanical drawing of the mating ETX footprint.

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9.2 Mating ETX Footprint

The Fire Engine mating ETX Footprint for the baseboard complies with the following:

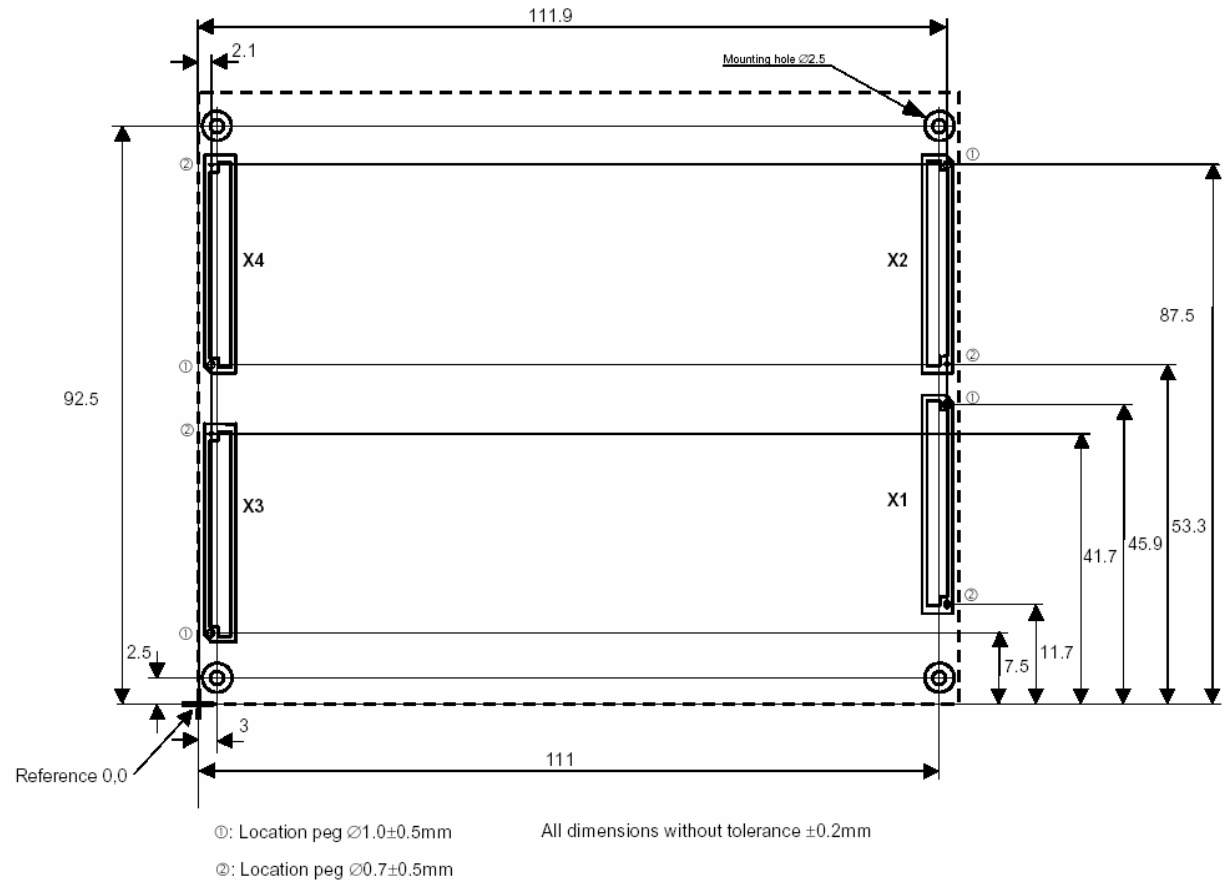

Figure 9.2: Fire Engine Mating ETX Footprint Mechanical Drawing

Note: Dimensions are NOT the same for the ETX footprint. Specifically, the footprints for the top and bottom side connectors have different alignment pin locations. Please refer to Section 9.1 for the mechanical drawing of the ETX footprint.

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