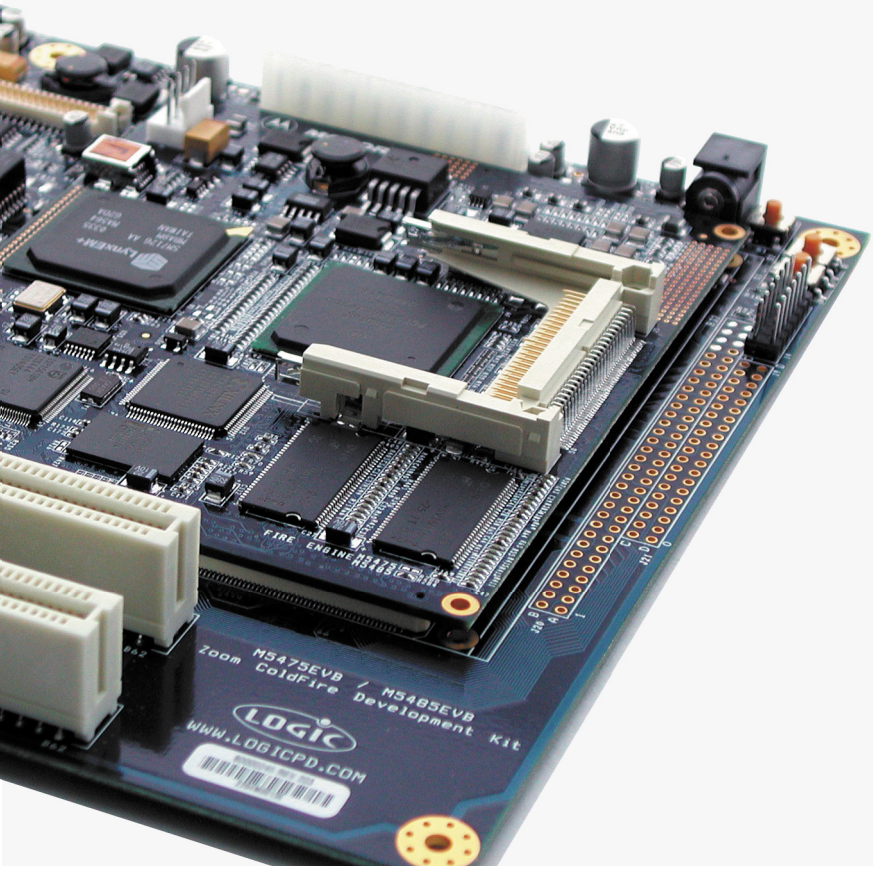
Zoom™

ColdFire Development Kit

Mini-ITX LITEKIT
Hardware Specification



developed by LOGIC

Launched by Motorola
freescale semiconductor

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
A	Ron Ross, Kurt Larson	Release	KTL	8/30/2004
B	Nathan Kro	Updated Section 6	KTL	12/17/2004
C	Nathan Kro	Swapped CAN0 with CAN1 signals	KTL	04/08/2005

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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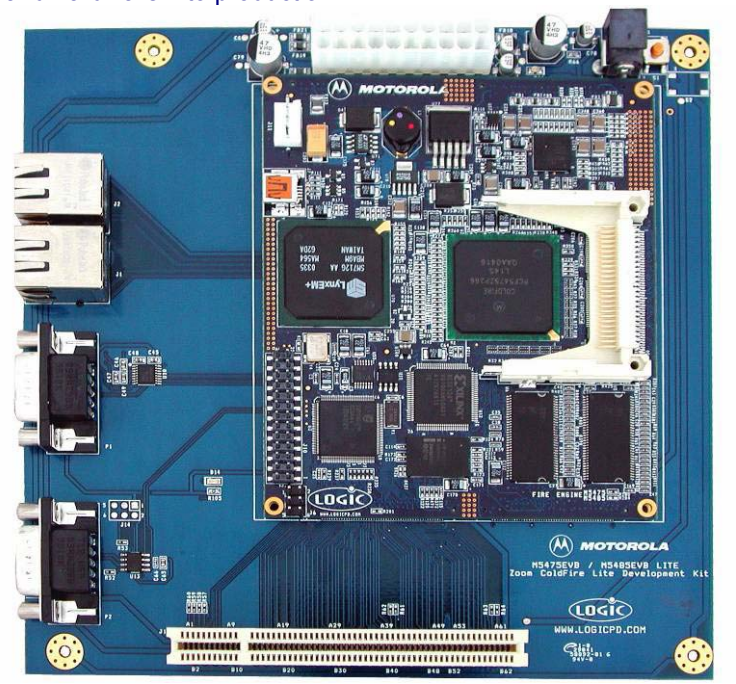
1 Introduction

1.1 Product Brief

The Zoom™ ColdFire Development Kit is a low-cost Application Development Kit for evaluating the functionality of the ColdFire processor and Fire Engine. This results in an embedded product development cycle with **less time, less cost, less risk ... more innovation.**

Application development is performed directly on the product-ready Mini-ITX/Fire Engine and software Board Support Packages included in the kit. This enables customers to seamlessly transfer their application code and hardware into production.



Actual Size: 6.7" x 6.7" x 1.3"

Network Support

- Two RJ45 Ethernet jack connectors

PC Card Expansion

- 1 PCI 2.2 slot (32 Bit, 33 or 66MHz, 3.3V)

Serial Ports

- 1 115.2Kbps RS-232 serial port

Can 2.0b

- 1 port (MCF548x kit only)

Software

- LogicLoader™ (bootloader/monitor)
- ARC MQX RTOS[1]
- Freescale Debug ROM Monitor
- Green Hills Integrity[1]

Mechanical Mini-ITX

- 6.7" (170 mm) long x 6.7" (170 mm) wide x 1.3" (33 mm) high

Cables

- Serial cable (null modem)
- Ethernet Crossover

- 5 volt power supply
- BDM cable

[1]*Third party ports available from Freescale*

1.2 Acronyms

ADC	Analog to Digital Converter
BDM	Background Debug Mode
BoLo	Boot Loader
BSP	Board Support Package
CMOS	Complimentary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSPI	DMA Serial Peripheral Interface
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
ETX	Embedded Technology Extended
FEC	Fast-Ethernet Controller
FET	Field Effect Transistor
FIFO	First In First Out
FIR	Fast Infrared
GPIO	General Purpose Input Output
IC	Integrated Circuit
I²C	Inter-Integrated Circuit
I/O	Input/Output
IRED	Infrared Device
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MBAR	Module Base Address Register
MIR	Mid Infrared
MMC	Multimedia Card
NC	No Connect
PC	Personal Computer
PCI	Peripheral Component Interconnect
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
POTS	Plain Old Telephone System
PSC	Programmable Serial Controller
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System-on-Chip
SoM	System-on-Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

1.3 Technical Specification

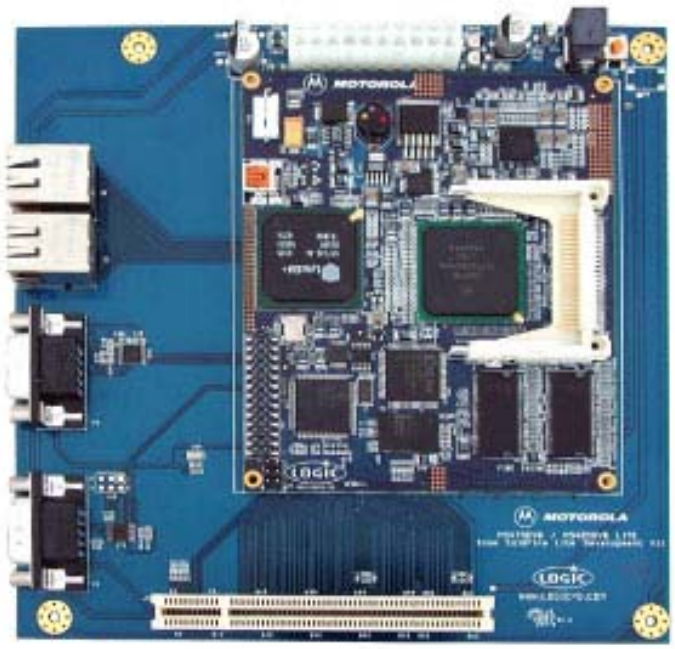
Please refer to the following component specifications and data sheets.

- Freescale ColdFire Microcontroller MCF548x
- Freescale ColdFire Microcontroller MCF547x
- Logic Document: MCF547x/8x Fire Engine Hardware Specification
- Logic Document: Application Note 228: Fire Engine Design Guideline

Note: *All users implementing the Fire Engine module should reference Logic's* Application Note 228: Fire Engine Design Guideline *document.*

For further Freescale documentation please visit: http://www.freescale.com/.

1.4 Fire Engine Advantages

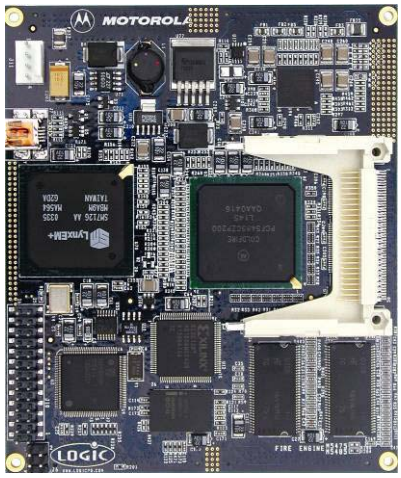


- Logic's Fire Engines accelerate your product's time-to-market, and provide the following advantages:
  - Product Ready Hardware and Software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – Allows you to focus on other aspects of your design
- Common SOM-ETX form factor:
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations are available to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

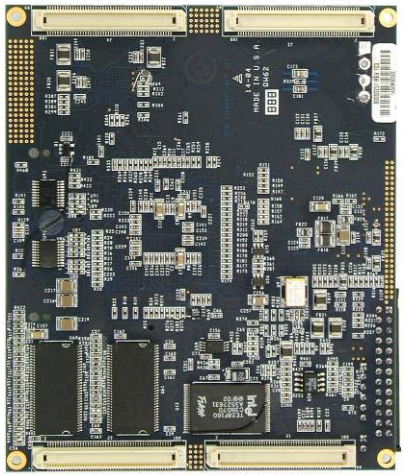
1.5 Fire Engine Interface

The ETX interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common ETX footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of your design onto the Fire Engine reduces any long-term risk of obsolescence. If a component on the Fire Engine design becomes obsolete, Logic will simply design for alternative part that is transparent to your product. Furthermore, Logic tests all Fire Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.



Fire Engine Top View



Fire Engine Bottom View

Figure 1.1: Logic's Fire Engine

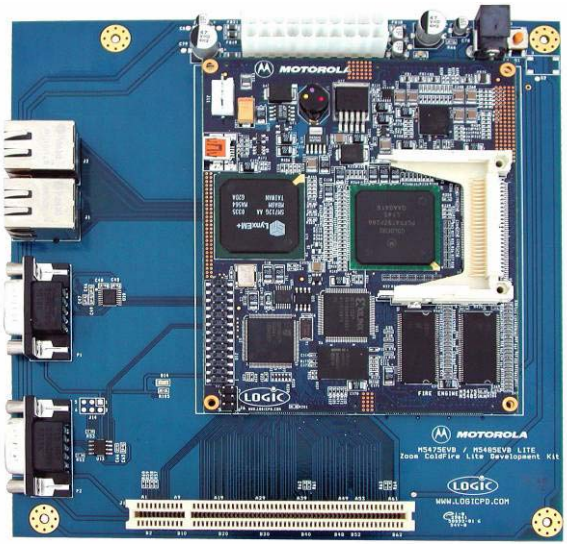


Figure 1.2: Logic's Fire Engine Advantage: ETX Board Installed On Mini-ITX Lite Host Platform

1.6 ITX Block Diagram

The following is a block diagram of the Mini ITX Lite Baseboard showing all major components. Each major component will be discussed as it applies to its appropriate external connector

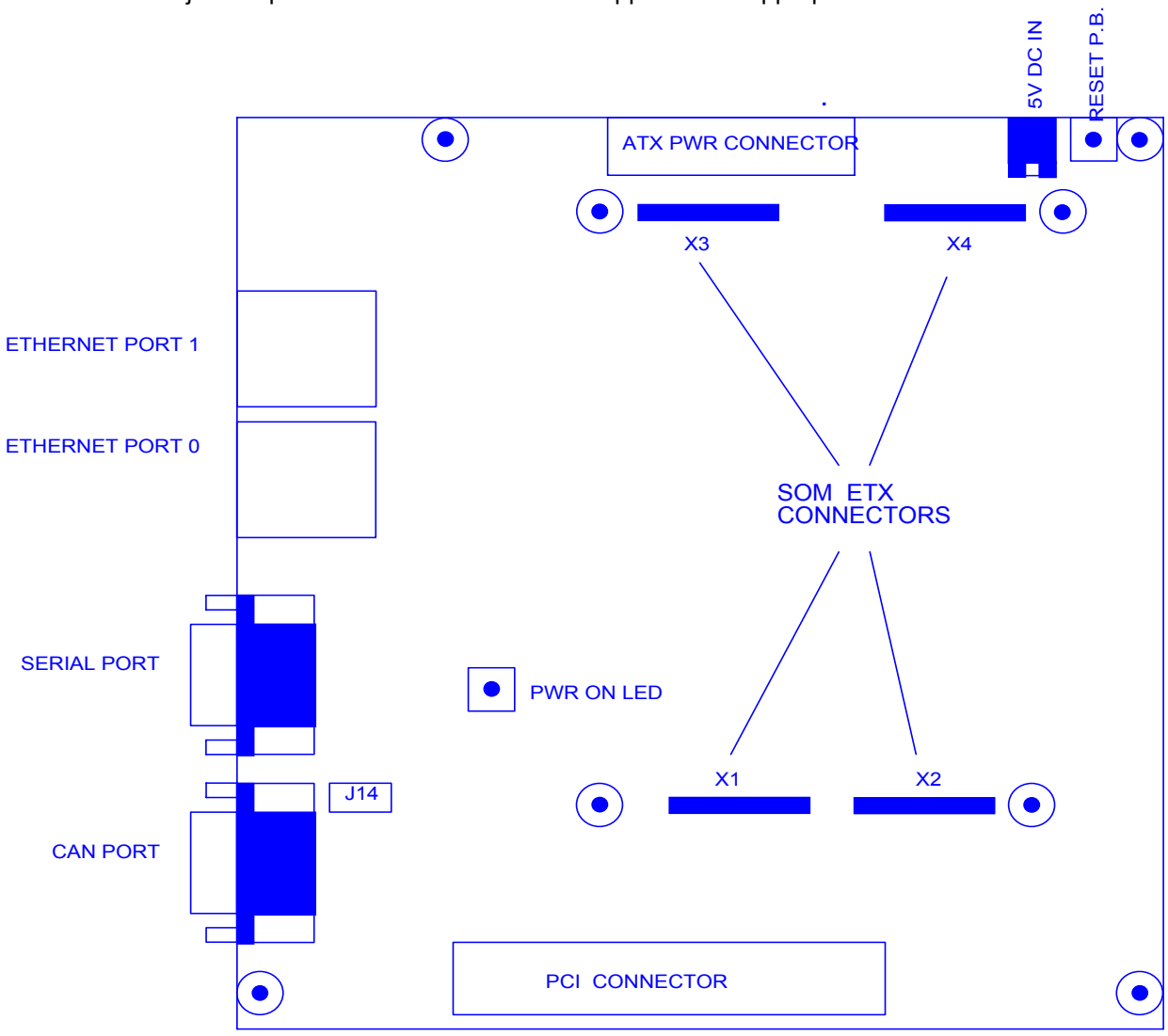


Figure 1:3: Mini ITX Lite Baseboard Block Diagram

2 ITX Baseboard Connectors

This section includes the connectors that accept an ETX module.

The mechanical characteristics comply with the ETX standard.

2.1 X1: (J7 on PCB)

The X1 connector is dedicated to the functions of the PCI ports and the USB host ports. USB host is not supported on this baseboard and therefore the signals associated with USB host are not connected. If USB host ports are required, order the M5475EVB or M5485EVB kits from Freescale.

The following is the X1 pin out:

	J7		J7
Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCI_CLK3	4	N.C.
5	GND	6	GND
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	PCI_BG3#	12	3.3V_ETX
13	PCIREQ3#	14	N.C.
15	N.C.	16	3.3V_ETX
17	N.C.	18	N.C.
19	5V	20	5V
21	N.C.	22	N.C.
23	PCI_AD0	24	3.3V_ETX
25	PCI_AD1	26	PCI_AD2
27	PCI_AD4	28	PCI_AD3
29	PCI_AD6	30	PCI_AD5
31	PCI_C/BE0#	32	PCI_AD7
33	PCI_AD8	34	PCI_AD9
35	GND	36	GND
37	PCI_AD10	38	N.C.
39	PCI_AD11	40	M66EN
41	PCI_AD12	42	N.C.
43	PCI_AD13	44	N.C.
45	PCI_AD14	46	N.C.
47	PCI_AD15	48	N.C.
49	PCI_C/BE1#	50	N.C.
51	5V	52	5V
53	PCI_PAR	54	PCI_SERR#
55	PCI_PERR#	56	N.C.
57	N.C.	58	N.C.
59	PCI_LOCK#	60	PCI_DEVSEL#
61	PCI_TRDY#	62	N.C.
63	PCI_IRDY#	64	PCI_STOP#
65	PCI_FRAME#	66	N.C.

67	GND	68	GND
69	PCI_AD16	70	PCI_C/BE2#
71	PCI_AD17	72	N.C.
73	PCI_AD19	74	PCI_AD18
75	PCI_AD20	76	N.C.
77	PCI_AD22	78	PCI_AD21
79	PCI_AD23	80	N.C.
81	PCI_AD24	82	PCI_C/BE3#
83	5V	84	5V
85	PCI_AD25	86	PCI_AD26
87	PCI_AD28	88	N.C.
89	PCI_AD27	90	PCI_AD29
91	PCI_AD30	92	N.C.
93	PCI_RESET#	94	PCI_AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

The X1 connector is compliant with the ETX standard with an exception of pin 40. M66EN is a signal that allows PCI boards to give notification (when high) that they can run at 66MHZ. This replaces the MICIN (Microphone input) signal as identified by the ETX standard.

The schematic diagram of the X1 connector is as shown below:

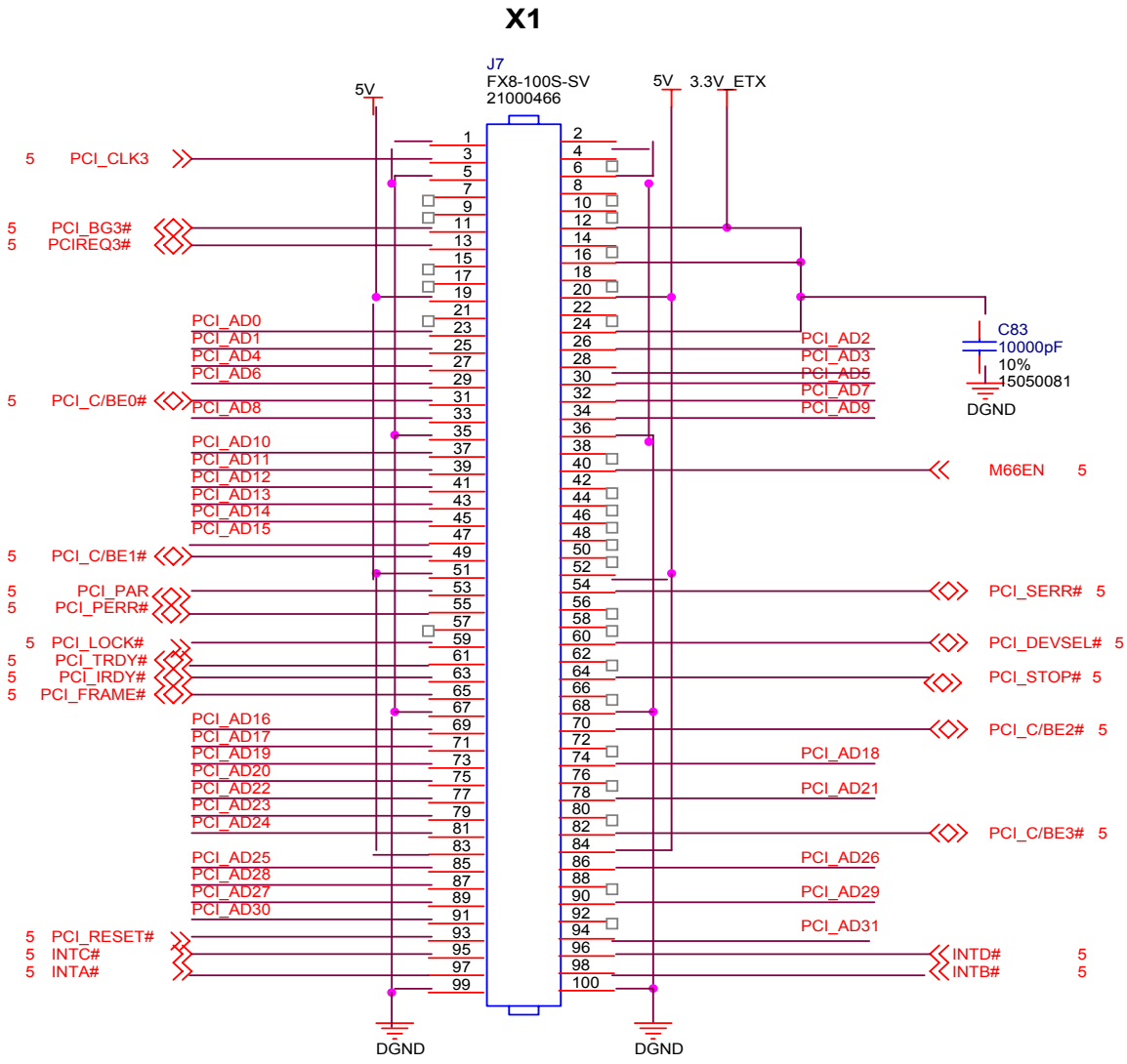


Figure 2.1: X1 Connector

2.2 X2: (J6 on PCB)

According to the ETX standard, this connector is dedicated to ISA functionality.
ISA is not supported on this baseboard. Therefore, all nets are un-connected except for power and ground. If ISA support is required, the M5475EVB or M5485EVB kit can be ordered from Freescale.

The following is the X2 pin out:

	J6		J6
Pin	Signal	Pin	Signal
1	GND	2	GND
3	N.C.	4	N.C.
5	N.C.	6	N.C.
7	N.C.	8	N.C.

9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	N.C.
19	N.C.	20	N.C.
21	N.C.	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	N.C.
27	N.C.	28	N.C.
29	N.C.	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	N.C.
35	GND	36	GND
37	N.C.	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	N.C.
43	N.C.	44	N.C.
45	N.C.	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	N.C.
51	5V	52	5V
53	N.C.	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	N.C.
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.
65	N.C.	66	N.C.
67	GND	68	GND
69	N.C.	70	N.C.
71	N.C.	72	N.C.
73	N.C.	74	N.C.
75	N.C.	76	N.C.
77	N.C.	78	N.C.
79	N.C.	80	N.C.
81	N.C.	82	N.C.
83	5V	84	5V
85	N.C.	86	N.C.
87	N.C.	88	N.C.
89	N.C.	90	N.C.
91	N.C.	92	N.C.
93	N.C.	94	N.C.
95	N.C.	96	N.C.
97	N.C.	98	N.C.
99	GND	100	GND

The schematic diagram of the X2 connector is as shown below:

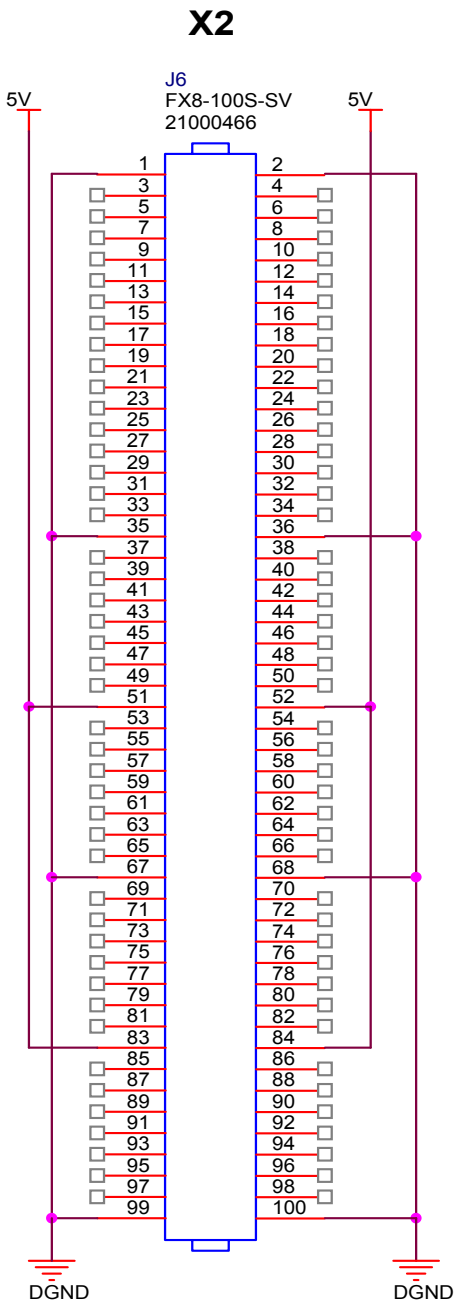


Figure 2.2: X2 Connector

2.3 X3: (J8 on PCB)

This connector is dedicated to Video and Serial ports. One serial port is available on this baseboard. If LCD or CRT video support is required or more serial ports, a M5475EVB or M5485EVB kit can be ordered from Freescale.

The following is the X3 pin out:

	J8		J8
Pin	Signal	Pin	Signal
1	GND	2	GND
3	N.C.	4	N.C.
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	N.C.
15	GND	16	GND
17	N.C.	18	N.C.
19	N.C.	20	N.C.
21	GND	22	GND
23	N.C.	24	N.C.
25	N.C.	26	N.C.
27	GND	28	GND
29	N.C.	30	N.C.
31	N.C.	32	N.C.
33	GND	34	GND
35	N.C.	36	N.C.
37	N.C.	38	N.C.
39	5V	40	5V
41	N.C.	42	N.C.
43	N.C.	44	N.C.
45	N.C.	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	N.C.
51	N.C.	52	N.C.
53	5V	54	GND
55	N.C.	56	N.C.
57	N.C.	58	N.C.
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.
65	GND	66	GND
67	N.C.	68	N.C.
69	N.C.	70	N.C.
71	N.C.	72	GND
73	N.C.	74	N.C.
75	N.C.	76	N.C.
77	N.C.	78	N.C.

79	N.C.	80	N.C.
81	5V	82	5V
83	PSC0_RXD	84	N.C.
85	PSC0_RTS#	86	N.C.
87	N.C.	88	N.C.
89	N.C.	90	N.C.
91	N.C.	92	N.C.
93	PSC0_CTS#	94	N.C.
95	PSC0_TXD	96	N.C.
97	N.C.	98	N.C.
99	GND	100	GND

The schematic diagram of the X3 connector is as shown below:

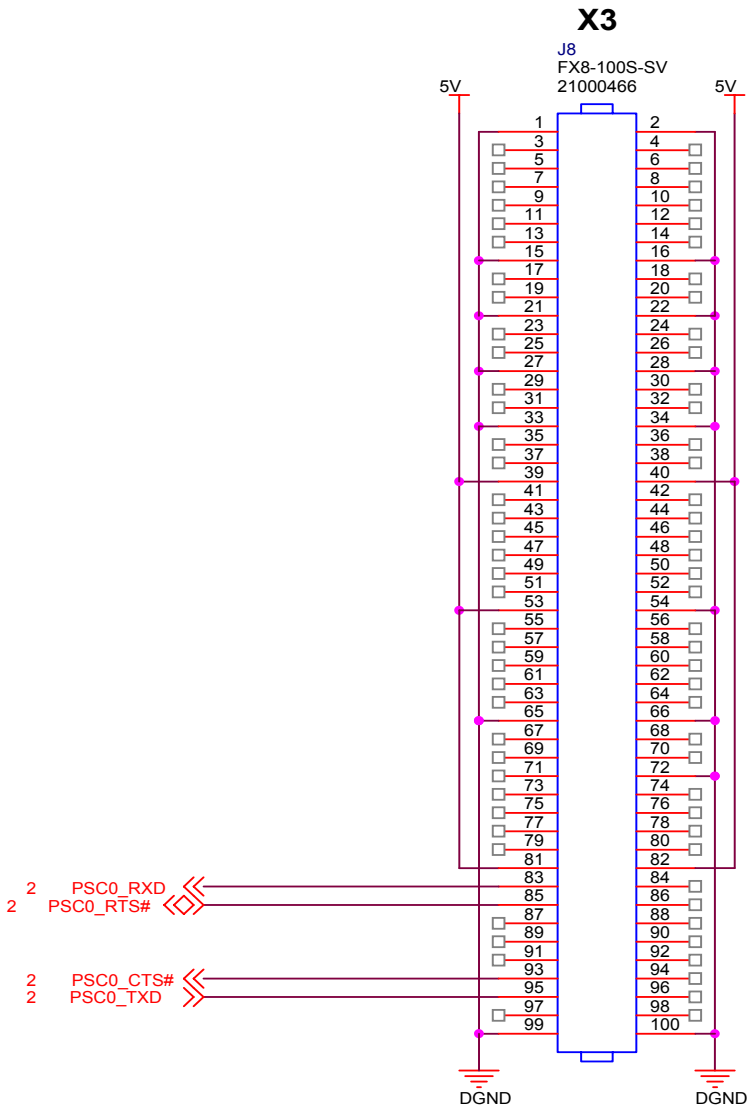


Figure 2.3: X3 Connector

2.4 X4: (J9 on PCB)

This connector is dedicated to the functions of the CAN interface, DSPI, I2C, Ethernet interface, ATX Power Control and Programmable timers.

The following is the X4 pinout:

J9		J9	
Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	N.C.
5	PS_ON#	6	N.C.
7	PWRBTN#	8	N.C.
9	N.C.	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	N.C.
15	N.C.	16	N.C.
17	5V	18	5V
19	N.C.	20	N.C.
21	N.C.	22	N.C.
23	N.C.	24	N.C.
25	TOUT0	26	N.C.
27	GND	28	N.C.
29	N.C.	30	N.C.
31	N.C.	32	N.C.
33	GND	34	GND
35	N.C.	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	N.C.
43	TIN2	44	N.C.
45	TOUT2	46	N.C.
47	N.C.	48	N.C.
49	5V	50	5V
51	N.C.	52	N.C.
53	N.C.	54	N.C.
55	GND	56	N.C.
57	RX-_1	58	N.C.
59	RX+_1	60	N.C.
61	TX-_1	62	N.C.
63	TX+_1	64	N.C.
65	GND	66	GND
67	N.C.	68	N.C.
69	N.C.	70	N.C.
71	GND	72	N.C.
73	N.C.	74	N.C.
75	N.C.	76	N.C.
77	GND	78	N.C.
79	N.C.	80	N.C.
81	5V	82	5V

83	N.C.	84	N.C.
85	LAN_GND	86	N.C.
87	N.C.	88	N.C.
89	N.C.	90	N.C.
91	RX-_0	92	N.C.
93	RX+_0	94	N.C.
95	TX-_0	96	N.C.
97	TX+_0	98	BUTTON_MRESET#
99	LAN_GND	100	GND

The shaded pins shown above denote differences between this connector and the ETX standard. These include additional Logic Product Development ETX module supported peripherals.

The schematic diagram of the X4 connector is as shown below:

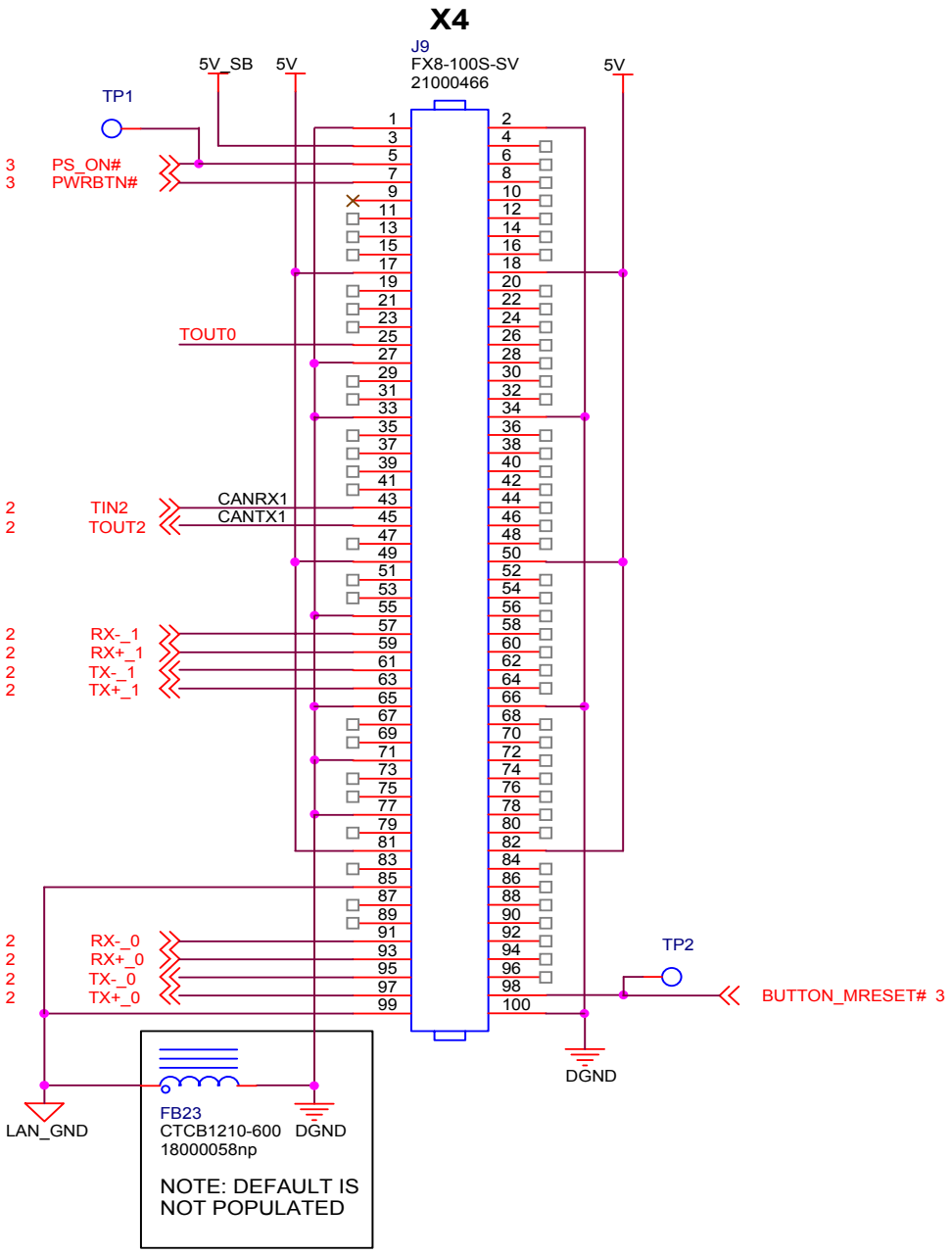


Figure 2.4: X4 Connector

3 Connectors

3.1 Ethernet Connectors

Up to 2 Ethernet ports are available from the ETX standard module, which must contain a physical interface (PHY). From the PHY, (ETX connector X4) the Ethernet signals go J1 and J2, which have internal isolation transformers.

Both ports are full-duplex, 10BASE-T/100BASE-TX compatible.

The ETX standard provides support for only 1 Ethernet port. Modifications have been made to the X4 connector so the Logic Product Development ETX Fire Engine is able to support both Ethernet ports. Please see the section on the X4 connector for details.

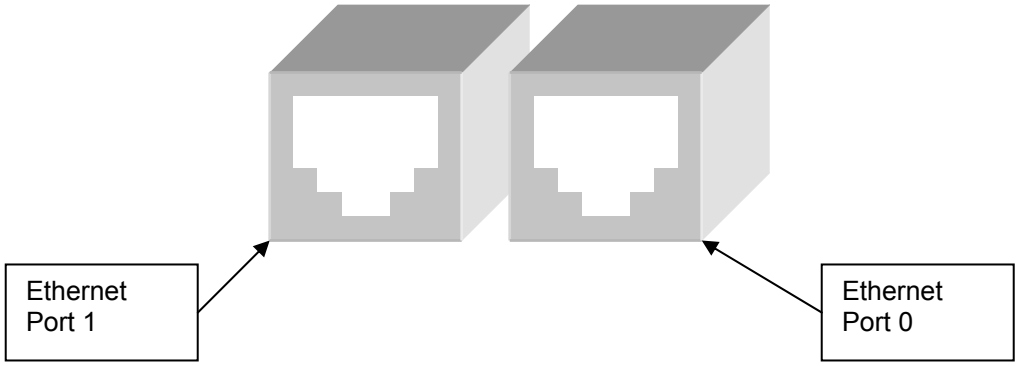


Figure 3.1: Ethernet Connectors

3.2 CAN Connector

The Controller Area Network (CAN) interface operates from the ETX module through connector X4. The ETX standard does not provide for CAN interfaces. Deviations from the standard were made to accommodate these processor specific supported interfaces. Please refer to the Logic Document: MCF547x/8x Fire Engine Hardware Specification for details.
On this baseboard, jumper J14 allows for daisy chaining of CAN devices. When J14 pins 4 and 6 are jumpered, a termination resistor is connected across the differential data lines. This is appropriate for the CAN port when it is at the end of a daisy chain. When J14 pins 4 and 6 are NOT jumpered, there is no termination resistor. This is appropriate for the port being in the middle of the daisy chain. Connector X4, Pins 43 and 45 have been assigned to CANRX1 and CANTX1 respectively. The CAN port is supported by Logic Product Development's Fire Engine.

Note: Only the MCF548x processor supports CAN.

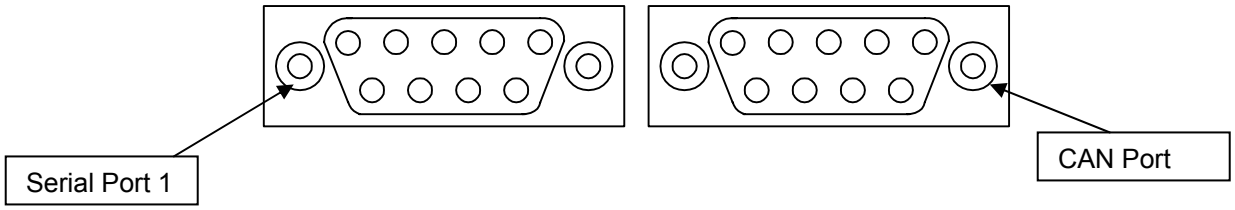


Figure 3.2: CAN Connector

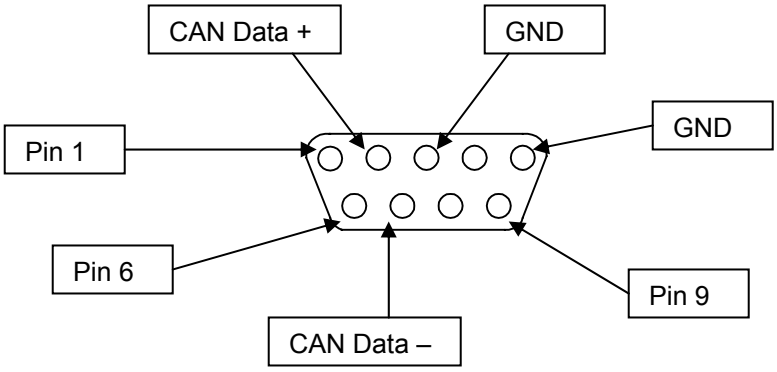


Figure 3.3: Connector Pin-out for the CAN Connector

3.3 RS232 Serial Port Connector

The standard RS232 serial port is provided from the ETX module's X3 connector. Support is provided for RTS and CTS "flow control". All signals from the X3 connectors are CMOS logic levels and are converted to RS232 logic levels on the Mini ITX Lite board.

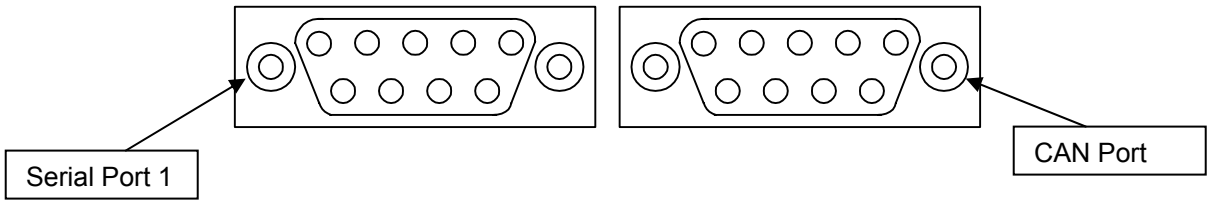


Figure 3.4: Serial Port Connector

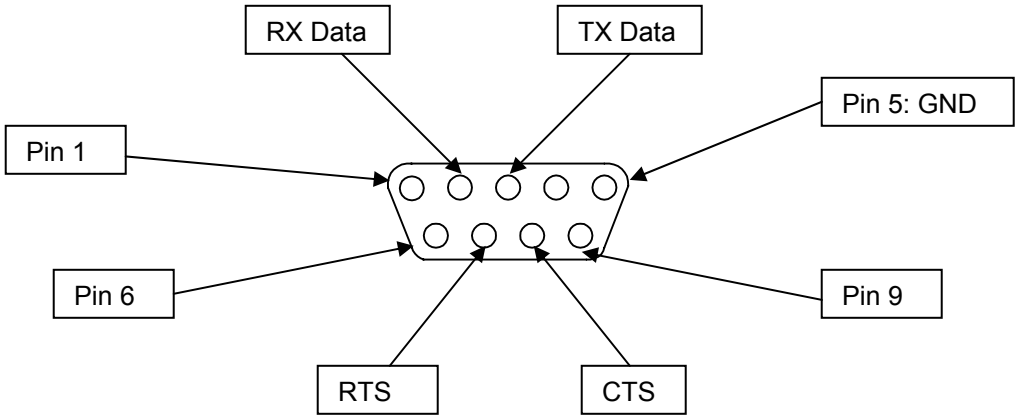


Figure 3.5: Serial Port Connector Pin-out

	RS-232	9 Pin Connector			
Pin No.	Pin Name	Full Name	Type	Description	Supported on
					Mini ITX Lite
1	DCD	Data Carrier Detect	Input	Typically from a Modem or Data Set. Indicates a data carrier is being received.	No
2	RxD	Receive Data	Input	Serial data from external device	Yes
3	TxD	Transmit Data	Output	Serial Data to external device	Yes
4	DTR	Data Terminal Ready	Output	Indication to external device that this port is ready to establish a communication link.	No
5	GND	Signal Ground	Ground	Reference	Yes
6	DSR	Data Set Ready	Input	Indication from the external device that it is ready to establish a communication link.	No
7	RTS	Request to Send	Output	Indication to external device that this port is ready to exchange data. (Typically used with CTS to provide data "flow control")	Yes
8	CTS	Clear to Send	Input	Indication from the external device that it is ready to exchange data. (Typically used with RTS to provide data "flow control")	Yes
9	RI	Ring Indicator	Input	Typically from a Modem or Data Set. Indicates a "Ring" signal is being received.	No

3.4 PCI Connector

The PCI connector is located at J15. It is an industry standard 32-bit, 3.3V only slot. It may run at 25MHz, 33MHz, 50MHz or 66MHz depending on how the ETX module is configured.

All signal connections are made directly between the X1 connector to the ETX board and the PCI connector.

The PCI connector obtains all of its power from an ATX type supply. It will not operate when the baseboard is powered from the modular 5V supply.

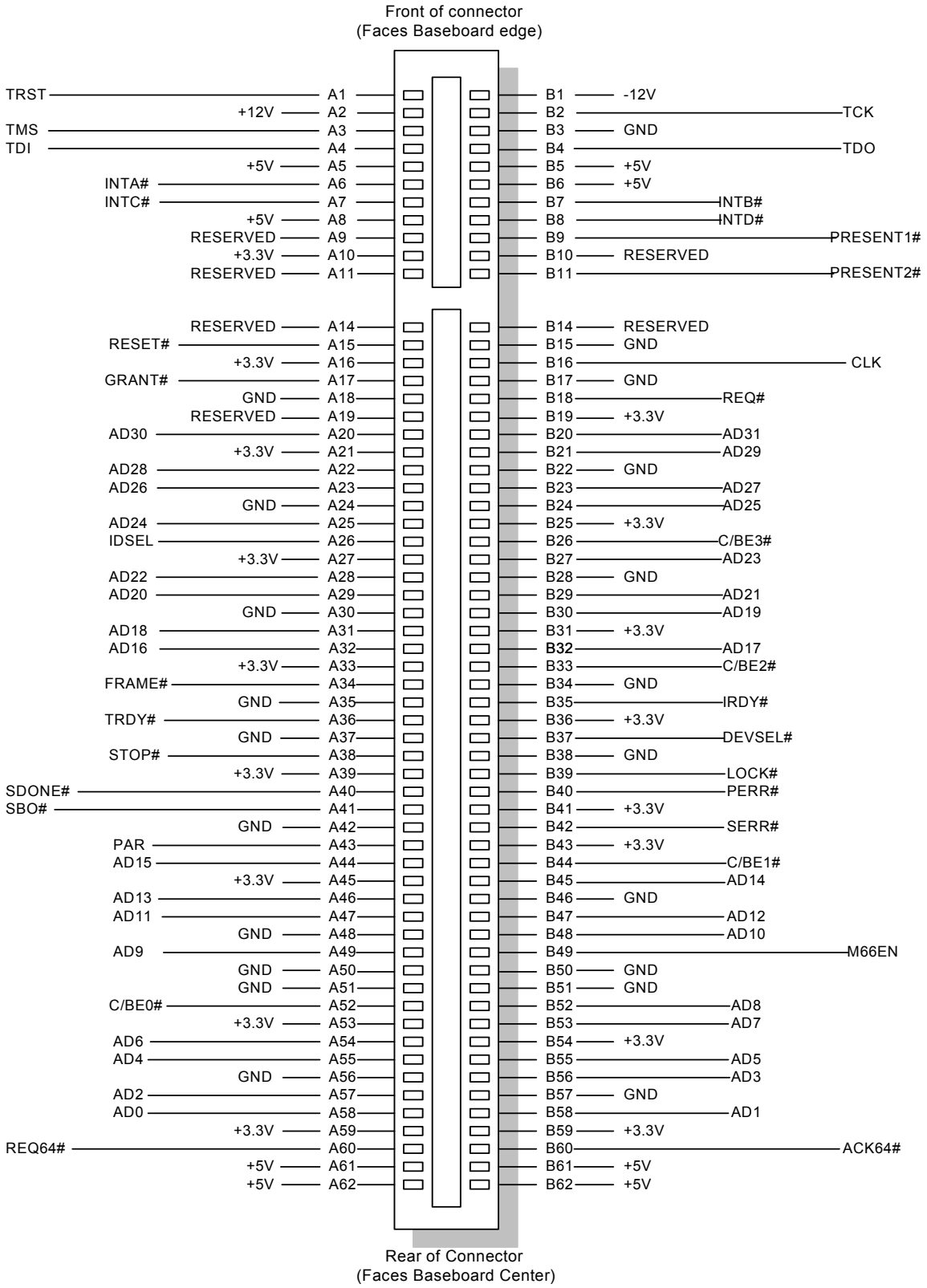


Figure 3.6: Typical 32 Bit PCI Connector

3.5 PCI Pin Definitions:

ADDRESS/DATA		
Pin Name	Direction	Description
PCI_AD[31:0]	Bidir	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase PCI_AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases PCI_AD[7:0] contain the least significant byte (lsb) and PCI_AD[31:24] contain the most significant byte (msb). Write data is stable and valid when PCI_IRDY# is asserted and read data is stable and valid when PCI_TRDY# is asserted. Data is transferred during those clocks where both PCI_IRDY# and PCI_TRDY# are asserted.
PCI_C/BE[3:0]#	Bidir	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI_C/BE[3:0]# define the bus command. During the data phase, they are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which bytes carry meaningful data. PCI_C/BE[0]# applies to byte 0 (lsb) and PCI_C/BE[3]# applies to byte 3 (msb).
PCI_PAR	Bidir	Parity is even parity across PCI_AD[31:0] and PCI_C/BE[3:0]#. Parity generation is required by all PCI devices. PCI_PAR is stable and valid one clock after the address phase. For data phases, PCI_PAR is stable and valid one clock after either PCI_IRDY# is asserted on a write transaction or PCI_TRDY# is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as PCI_AD[31:0], but is delayed by one clock.) The initiator drives PCI_PAR for address and write phases; the target drives PCI_PAR for read data phases.
BUS ARBITRATION		**(Initiators, (I.e. Bus Masters) Only)**
PCIREQ3#	PCI device to Arbiter	Bus Request. If the PCI device is capable of becoming an initiator (master), it can only do so by asserting this line to request use of the bus. It cannot drive the PCI bus until it receives a PCI_BG3#and it must tri-state the PCIREQ3# line while the PCI_RESET# line is active. Every device in the system that is capable of becoming an initiator will have its own unique PCIREQ3# line.
PCI_BG3#	Arbiter to PCI device	Bus Grant. When active, the PCI device may drive the PCI bus an Initiator (Bus Master). This signal must be ignored when the PCI_RESET# line is active. Every PCI device in the system that is capable of becoming an initiator will have its own unique PCI_BG3#signal.
INTERFACE CONTROLS		

Pin Name	Direction	Description
PCI_FRAME#	Initiator to Target	The PCI_FRAME# signal is driven by the initiator to indicate the beginning and duration of an access. PCI_FRAME# is asserted to indicate a bus transaction is beginning. While PCI_FRAME# is asserted, data transfers continue. When PCI_FRAME# is deasserted, the transaction is in the final data phase or has completed.
IDSEL	Initiator to Target	Initialization Device Select is used as a chip select during configuration read and write transactions. This line is typically connected to an PCI_AD[20:16] signal and a different signal is connected to each PCI slot or device which makes it unique. PCI_AD20 is connected to IDSEL on this baseboard.
PCI_DEVSEL#	Target to Initiator	Device Select, when driven by a target, indicates that it has decoded the initiator's address as its own. The Initiator uses this input to determine if any device on the bus has been selected.
PCI_IRDY#	Initiator to Target	Initiator Ready indicates the initiator’s ability to complete the current data phase of the transaction. PCI_IRDY# is used in conjunction with PCI_TRDY#. A data phase is completed on any clock when both PCI_IRDY# and PCI_TRDY# are asserted. During a write, PCI_IRDY# indicates that valid data is present on PCI_AD[31:0]. During a read, it indicates the initiator is prepared to accept data. Wait cycles are invoked until both PCI_IRDY# and PCI_TRDY# are asserted together.
PCI_TRDY#	Target to Initiator	Target Ready indicates the target's ability to complete the current data phase of the transaction. PCI_TRDY# is used in conjunction with PCI_IRDY#. A data phase is completed on any clock when both PCI_TRDY# and PCI_IRDY# are asserted. During a read, PCI_TRDY# indicates that valid data is present on PCI_AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are invoked until both PCI_IRDY# and PCI_TRDY# are asserted together.
PCI_STOP#	Target to Initiator	Stop indicates a request from the current target for the initiator to terminate the current transaction.
PCI_LOCK#	Initiator to Target	Lock indicates an atomic operation that may require multiple transactions to complete. When PCI_LOCK# is asserted, nonexclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of PCI_LOCK#. Control of PCI_LOCK# is obtained under its own protocol in conjunction with PCI_BG3#. It is possible for different initiators to use the PCI bus while a single initiator retains ownership of PCI_LOCK#. For more information, please refer to the PCI bus specification.
ERROR REPORTING		
Pin Name	Direction	Description

PCI_PERR#	Bidir	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PCI_PERR# pin is sustained tri-state and must be driven active by the device receiving data two clocks following the data when a data parity error is detected. The minimum duration of PCI_PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PCI_PERR# signal will be asserted for more than a single clock.) PCI_PERR# must be driven high for one clock before being tri-stated as with all tri-state signals. There are no special conditions when a parity error may be lost or when reporting of an error may be delayed. A device cannot report a PCI_PERR# until it has claimed the access by asserting PCI_DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
PCI_SERR#	Bidir	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. This usually results in a non-maskable interrupt (NMI) generated by the processor. PCI_SERR# is pure open drain and is actively driven for a single PCI clock by the device reporting the error. The assertion of PCI_SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR# to the deasserted state is accomplished by a pullup resistor. This pullup may take two to three clock periods to fully restore PCI_SERR#.
Interrupts		
Pin Name	Direction	Description
INTA# INTB# INTC# INTD#	PCI device to Host	Interrupts on PCI are optional and defined as "level sensitive", assertive low and use open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Multi-function devices may use all interrupts but they must be used in order. i.e. INTA# must be used before INTB# can be used; INTB# must be used before INTC# can be used; etc.
Other Pins		
Pin Name	Direction	Description
CLK	System to PCI slot	PCI Clock. This signal provides a 25MHz, 33MHz, 50MHz or 66MHz clock signal for the PCI slot depending on which ETX board is used and how it is configured. It must consist of a dedicated clock driver on the ETX board and terminates only at this slot.

PCI_RESET#	System to all PCI devices and slots	PCI System Reset. This signal, when asserted, resets the entire PCI bus. It can be activated from the processor on the ETX board and is also activated by the Power-on Master Clear as well as the pushbutton reset on the baseboard.
M66EN	From all slots and devices to system	66 MHz Clock enable. The intent of this signal is to determine if all attached devices are capable of operating at 66 MHz. On power up, if this static line is high, it is an indication that the CLK can be set to 66 MHZ. However, if any device pulls this line low, the maximum CLK speed that can be used is 33MHz.
PRESENT1# PRESENT2#	Not Used	Card present signals. These signals can be used to indicate whether or not a card is inserted into the connector and how much power it is expected to consume. These signals are not supported on this baseboard.
REQ64# ACK64#	Disabled via pullup resistors	These signals are used to support 64 bit wide data transfer capability. This baseboard operates in 32bit mode only.
SDONE# SBO#	Disabled via pullup resistors	These signals (Snoop Done, Snoop Backoff), have been redefined as "Reserved" pins in the PCI 2.2 Specification. They have been included here only for backwards compatibility.
TRST TMS TCK TDI TDO	Not Used	These signals are for JTAG testing and do not apply to the functional operation of the PCI bus.

3.6 PCI Board Compatibility

3.6.1 Voltage

The PCI connector provided on this baseboard is intended to accommodate only 3.3V or Universal type PCI boards. As a general rule, the ETX board installed may not be tolerant of 5V logic signals. Therefore, 5V PCI boards must not be inserted into this baseboard. The figure below shows how the type of PCI board can be determined.

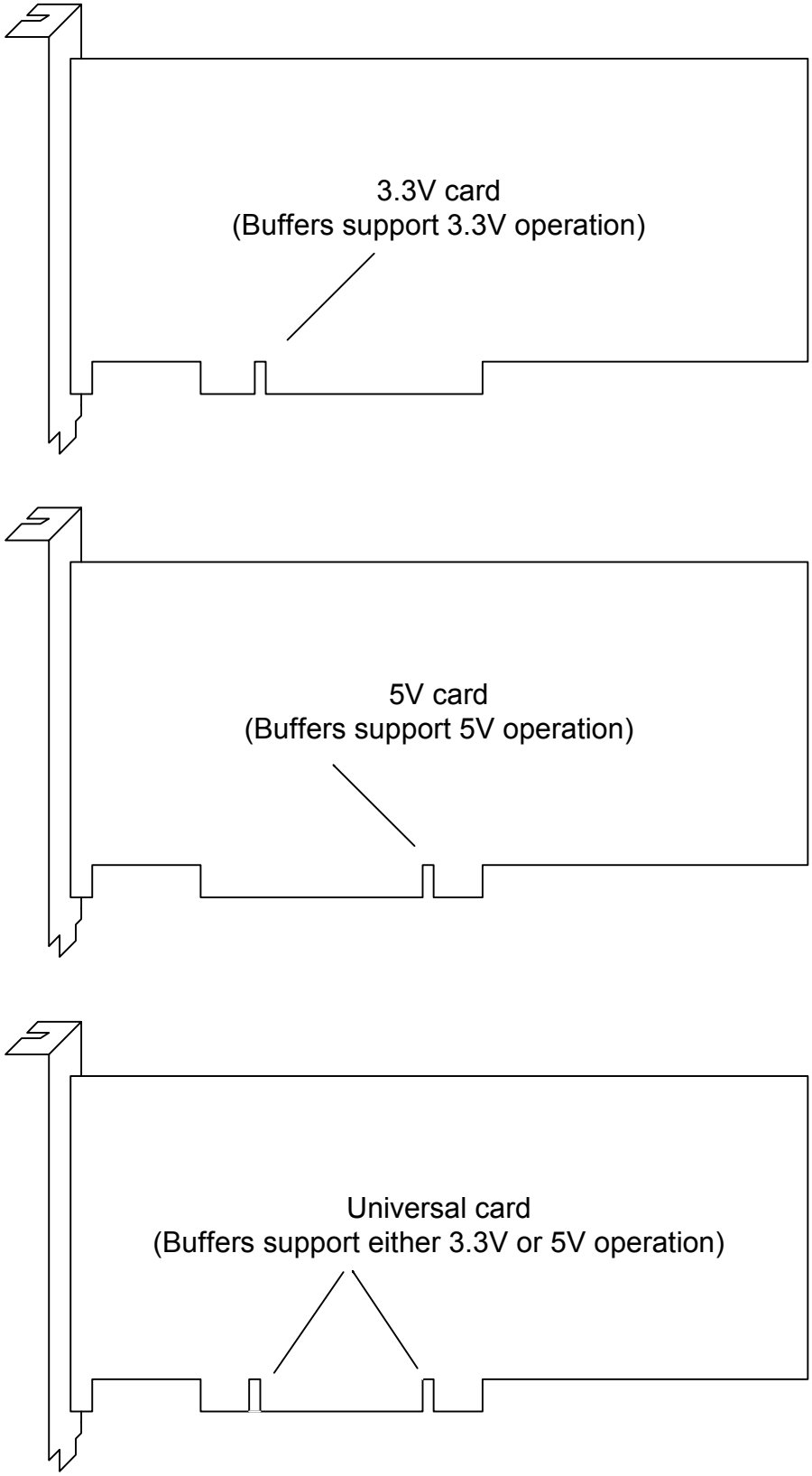


Figure 3.7: How to Determine a PCI Board Diagram

3.6.2 Current

The PCI Standard defines the maximum power allowable for any PCI slot including all voltages is 25W. This sets the maximum amount of current on 3.3V to 7.5A.

Note: Only an ATX supply connected to the baseboard will provide current to the PCI slot.

4 Push Buttons and Indicators

1. Master Reset (S1)

This momentary push button causes a System Reset to the ETX board. .

2. Power On Indicator (D14)

This indicator will illuminate when the 3.3V supply is active.

5 Power Supply

The Mini ITX Lite Baseboard may be powered in either of two ways: ATX Power supply or the supplied 5VDC Modular supply.

ATX POWER Supply: A standard 20 pin ATX power supply connector is provided at J10. Its pin configuration is as shown below:

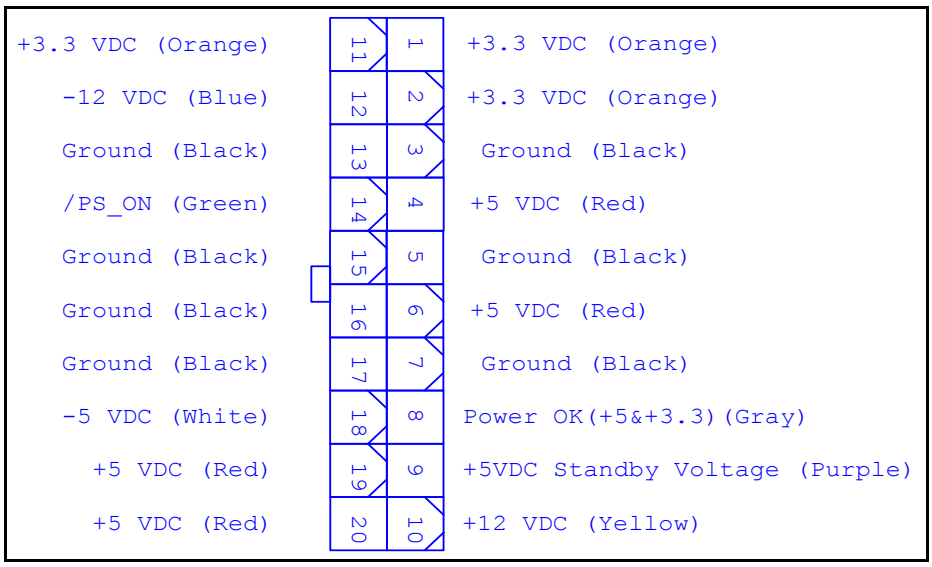


Figure 5.1: Power Connector

From this connector, the +5V is the primary voltage used. The –5V is not used. The 3.3V and the +/- 12V are used only on the PCI Slots.

5VDC Modular supply:

J11 is a standard 2.5 mm barrel jack connector, which accepts a standard power supply plug. NOTE: the center post is the +5V and the sleeve is ground.

5.1 Power Supply Requirements

The Mini-ITX Lite baseboard uses power from the +5V on either the ATX connector or the modular power connector. The current requirement for the Mini-ITX Lite board only is <50mA. Depending on the ETX module used, the total current is expected to be approximately 1.5 Amps to 2 Amps. The Mini-ITX Lite baseboard acquires its 3.3V from the ETX board to power its on-board components. The 3.3V necessary to power the PCI slot is obtained only from the ATX power connector.

6 Mechanical Drawings

6.1 Mini-ITX Lite Baseboard

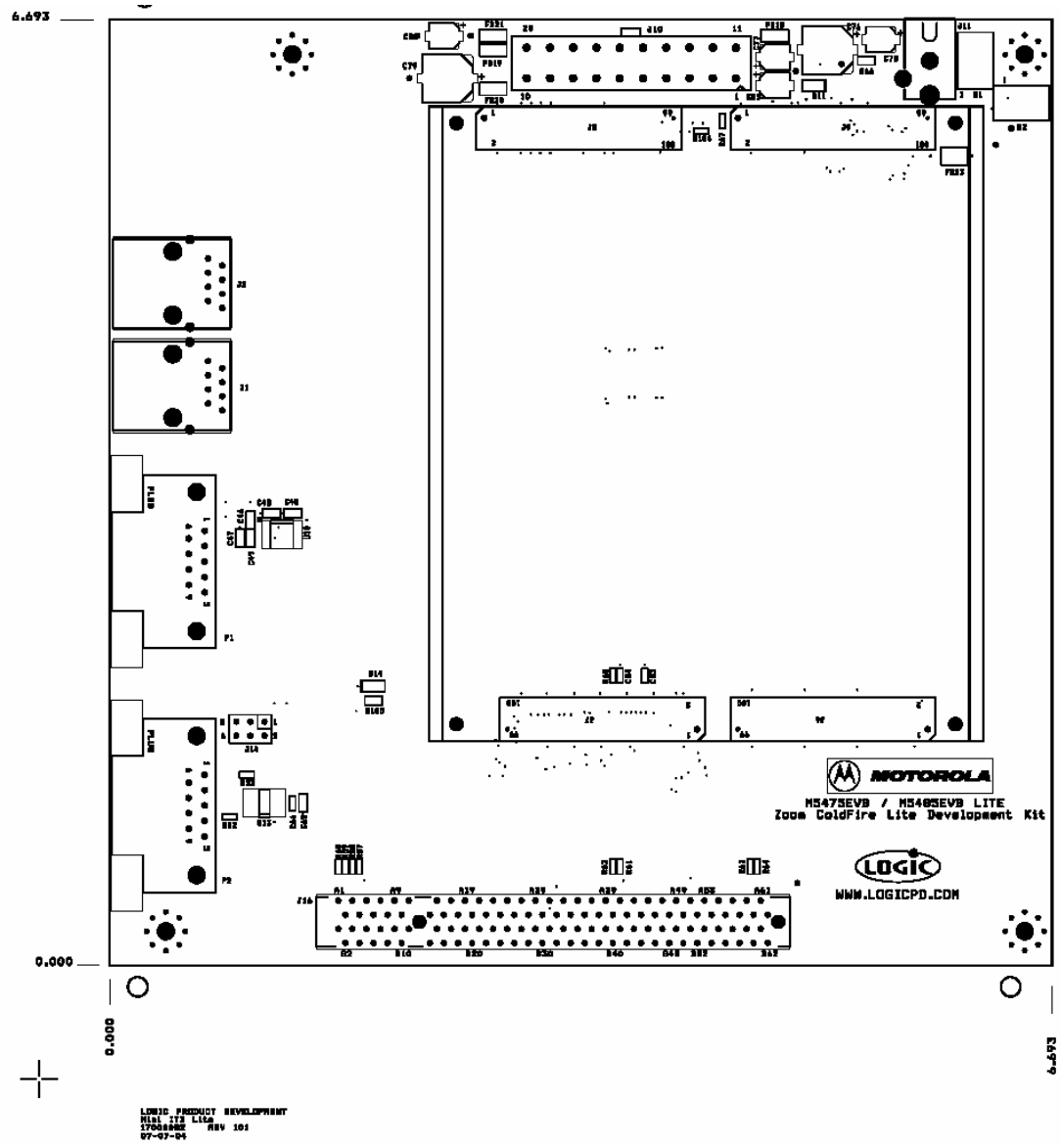


Figure 6.1: Mini-ITX Lite Baseboard

6.2 Mating ETX Footprint

The Fire Engine mating ETX Footprint for the baseboard complies with the following:

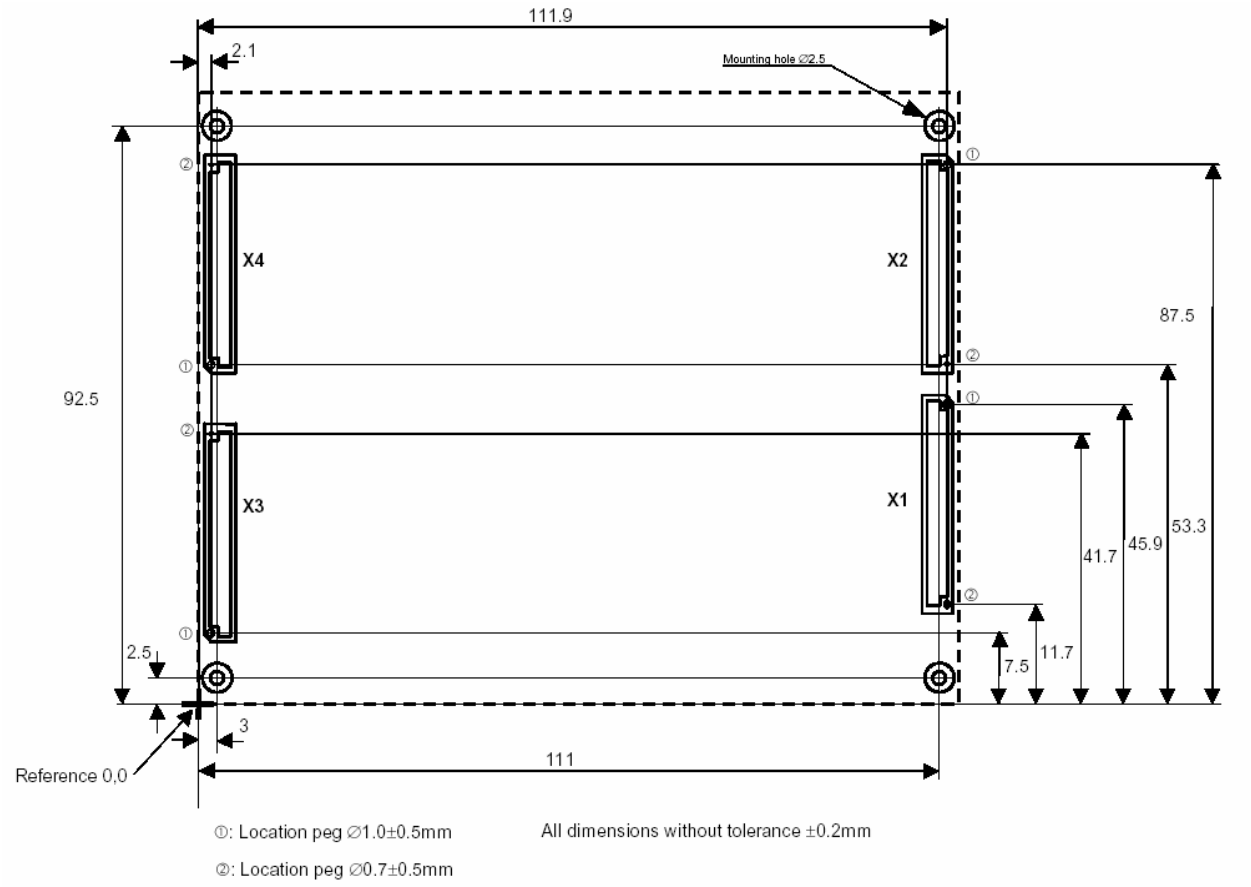


Figure 6.2: Fire Engine Mating ETX Footprint Mechanical Drawing

Note: Dimensions are NOT the same for the ETX footprint. Specifically, the footprints for the top and bottom side connectors have different alignment pin locations. Please refer to the MCF547x/8x Hardware Specification for the mechanical drawing of the ETX footprint.

