MCF5373-10
Fire Engine

NANO

LOGIC

freescale semiconductor

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC REV	APPROVAL	DATE
A	Kurt Larson, Jed Anderson	Initial Release; Updated all processor references to indicate use of the MCF5373L	1002736 Rev3	KTL	10/17/06
B	Jed Anderson	Updated Product Brief	1002736 Rev3	JCA	10/22/06

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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PRODUCT BRIEF:
Logic :: Freescale

MCF5373 FIRE ENGINE System on Module

The MCF5373 Fire Engine is a compact, product-ready hardware and software solution that fast forwards your embedded product design.

The MCF5373 Fire Engine is a complete System on Module (SOM) that offers essential features for handheld and embedded networking applications. Use of custom baseboards makes the Fire Engine the ideal foundation for OEMs developing handheld and compact products. The Fire Engine provides a common reference pin-out on its expansion connectors, which enables easy scalability to next generation microprocessor Fire Engines when new functionality or performance is required.

Application development is performed right on the product-ready MCF5373 Fire Engine and software Board Support Packages (BSPs), which enables you to seamlessly transfer your application code and hardware into production.

The MCF5373 Fire Engine is ideal for applications in the medical, point-of-sale, industrial, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the MCF5373 Fire Engine allows for powerful versatility and long-life products.

FREESCALE MCF5373 FIRE ENGINE

MCF5373 FIRE ENGINE :: HIGHLIGHTS:

+ Product-ready System on Module with the MCF5373L ColdFire processor running at 240 MHz
+ Compact form factor 60.2 mm x 67.8 mm x 4.4 mm
+ Long product lifecycle
+ Multiple third-party software options
+ 0 ˚C to 70 ˚C (commercial temp)
+ RoHS compliant

ZOOM™ COLDFIRE M5373EVB :: FEATURES:

+ Application baseboard
+ MCF5373 Fire Engine
+ Necessary accessories to immediately get up and running
+ Kit available from Freescale (M5373EVB)
+ See Zoom™ ColdFire SDK product brief for more information

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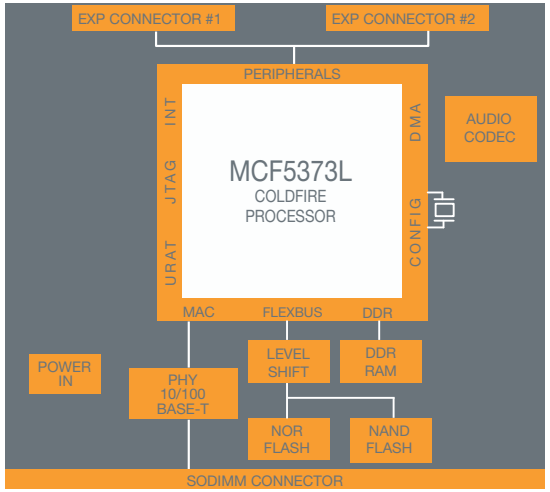
MCF5373 Fire Engine Block Diagram



MCF5329/73 Fire Engine Ordering Information

Freescale P/N	Speed (MHz)	DDR Mem (MB)	NOR Flash (MB)	NAND Flash (MB)	LCD/Touch	Audio	Ethernet
MCF5373*	240	32	2	16	--	Y	Y
MCF5329AFEE	240	32	2	0	Y	Y	Y
MCF5329BFEE	240	32	2	16	Y	Y	Y

*MCF5373 Fire Engines are only available as part of the M5373EVB kit. For production volumes, please use MCF5329 Fire Engines.

ZOOM™ ColdFire M5373EVB Ordering Information

Freescale P/N	SOM Configuration	Recommended Resale
M5373EVB	MCF5373	$699

LOGIC WEBSITE :: DESIGN RESOURCES:

+ Logic Technical Support : http://www.logicpd.com/support/
+ Technical Discussion Group : http://www.logicpd.com/support/tdg/
+ Frequently Asked Questions (FAQ) : http://www.logicpd.com/support/faq/
+ For more information contact Logic Sales : product.sales@logicpd.com

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PN: 1006342 Rev B

Product Features

Processor
+ Freescale MCF5373L 32-bit ColdFire RISC microprocessor running at 240 MHz

SDRAM Memory
+ 32 MB DDR SDRAM standard

Flash Memory
+ 2–4 MB scalable NOR flash (2 MB standard)
+ Scalable NAND flash (16 MB standard)

Network Support
+ 10/100 Base-T Ethernet controller for application/debug (National Semiconductor DP83848 PHY)

Audio
+ I2S compliant audio codec (Texas Instruments TLV320AIC23)

PC Card Expansion
+ CompactFlash Type I card (memory-mapped mode only)

USB
+ USB 2.0 full-speed host and device interface

Serial Ports
+ Three 16C550 compatible UARTs
+ Queued SPI interface w/selectable bit patterns

GPIO
+ Programmable I/O depending on peripheral requirements

Software
+ LogicLoader™ (bootloader/monitor)
+ Freescale dBUG ROM monitor
+ Multiple third-party software options

Mechanical
+ 60.2 mm wide x 67.8 mm long x 4.4 mm high

RoHS Compliant

freescale™ semiconductor

1.2 Acronyms

ACI	Audio Codec Interface
ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CDK	ColdFire® Development Kit
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FEC	Fast Ethernet Controller
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I2S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MMC	Multi Media Card
NC	No Connect
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RISC	Reduced Instruction Set Computer
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System on Chip
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

LogicLoader User's Manual (available from Logic at http://www.logicpd.com)
MCF5373 Reference Manual (available from Freescale® at http://www.freescale.com/coldfire)
Texas Instruments™ TLV320DAC23 Audio codec data sheet (available at http://www.TI.com)

1.4 Fire Engine Advantages

Logic's embedded solutions fast forward product development and helps your company stay focused on your high-value core technologies.

- Product-ready hardware and software solutions allow immediate application development that results in a shorter product development cycle.
  - Less time – time-to-market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – allows you to focus on other aspects of your design
- Common SOM footprint (see Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low-cost hardware solution – custom configurations are available to meet your design requirements and price points.

1.5 Fire Engine Interface

Logic's common Fire Engine (SOM-Card Engine) interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information (product.sales@logicpd.com).

In fact, encapsulating a significant amount of your design onto the Fire Engine reduces any long-term risk of obsolescence. If a component on the Fire Engine design becomes obsolete, Logic will simply design for an alternative part that is transparent to your product. Furthermore, Logic tests all Fire Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

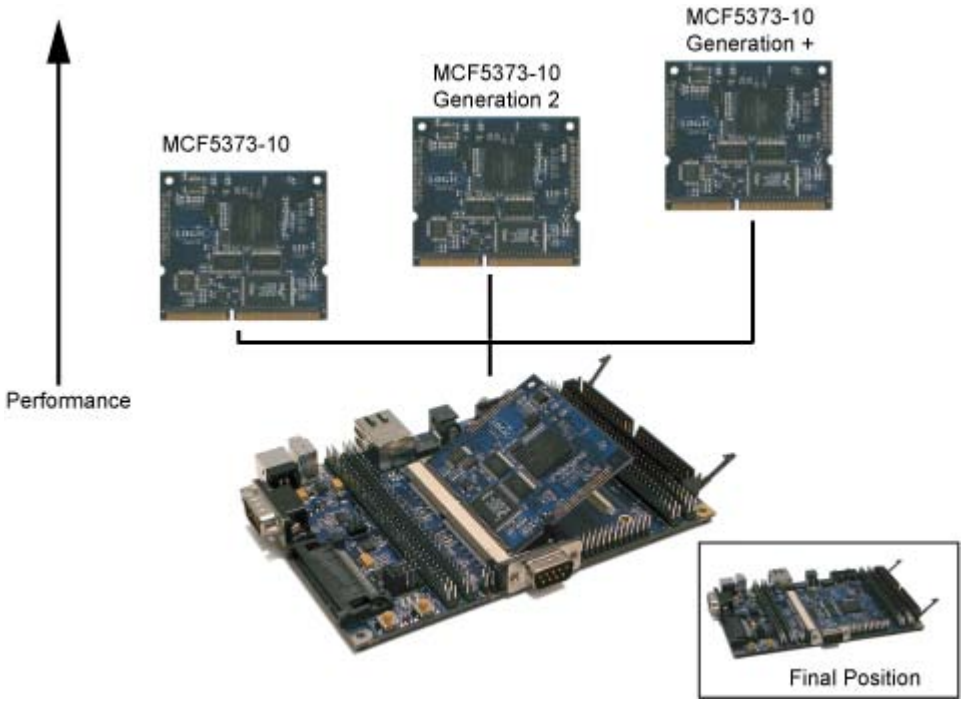
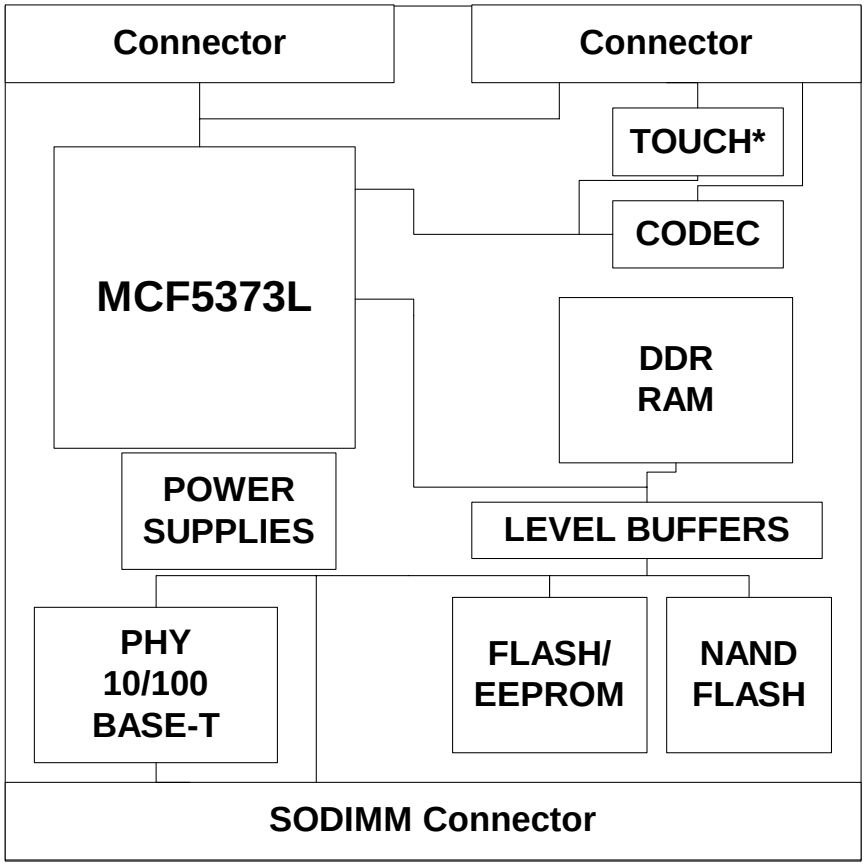


Figure 1.1: Fire Engine Advantages

1.6 Fire Engine Block Diagrams



*Touch is an optional device. By default, it is not populated.

Figure 1.2: MCF5373-10 Fire Engine Block Diagram

1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC IO and Peripheral Supply Voltage	3.3V	VSS-0.3 to 3.6	V
DC Core Supply Voltage	VCORE	VSS-0.3 to 2.7	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the Fire Engine and its components.

1.7.2 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	
DC 3.3V Active Current	68	236		mA	2,5,6
DC 3.3V Suspend Current		TBD		mA	2
DC 3.3V Standby Current		TBD		mA	2
DC Core Voltage	2.3	2.5	2.7	V	
DC Core Active Current	22	58		mA	2,5,6
DC Core Suspend Current		TBD		mA	2
DC Core Standby Current		TBD		mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input Signal High Voltage	0.8 x VCC			V	
Input Signal Low Voltage			0.2 x VCC	V	
Output Signal High Voltage	VCC – 0.3		VCC	V	
Output Signal Low Voltage	GND		GND + 0.3	V	

1. VCORE, SRAM, PLL, and 3.3V power are sequenced on the module.
2. Power consumption dependent on software state.
3. Contact Logic for more information on an industrial temperature MCF5373-10 Fire Engine.
4. May vary depending on Fire Engine configuration.
5. Minimum is average while CPU is in reset.
6. Typical is idle in LogicLoader with no activity and no display, Ethernet powered.

2 Electrical Specification

2.1 Microcontroller

2.1.1 MCF5373L Microcontroller

The MCF5373-10 Fire Engine uses Freescale's highly integrated MCF5373L ColdFire Microprocessor. This device features the V3 ColdFire core and provides many integrated on-chip peripherals, including:

Integrated ColdFire V3 Core
- 32-bit ColdFire V3 Core
- 4 stage instruction fetch pipeline
- 8 entry instruction buffer acceleration
- 16 kBytes instruction/data cache
- 32 kBytes on-chip SRAM

Three UARTs
AC97/I2S Codec Interface
One USB Client and One USB Host Interface (USB 2.0)
Many General Purpose I/O Signals
16 Independent DMA Channels
Four Programmable Timers
RTC
Low Power Modes

See Freescale's reference manual of the appropriate processor for additional information.
http://www.freescale.com/coldfire

IMPORTANT NOTE: Please visit http://www.freescale.com/coldfire for errata on the MCF5373L.

2.1.2 MCF5373L Microcontroller Block Diagram

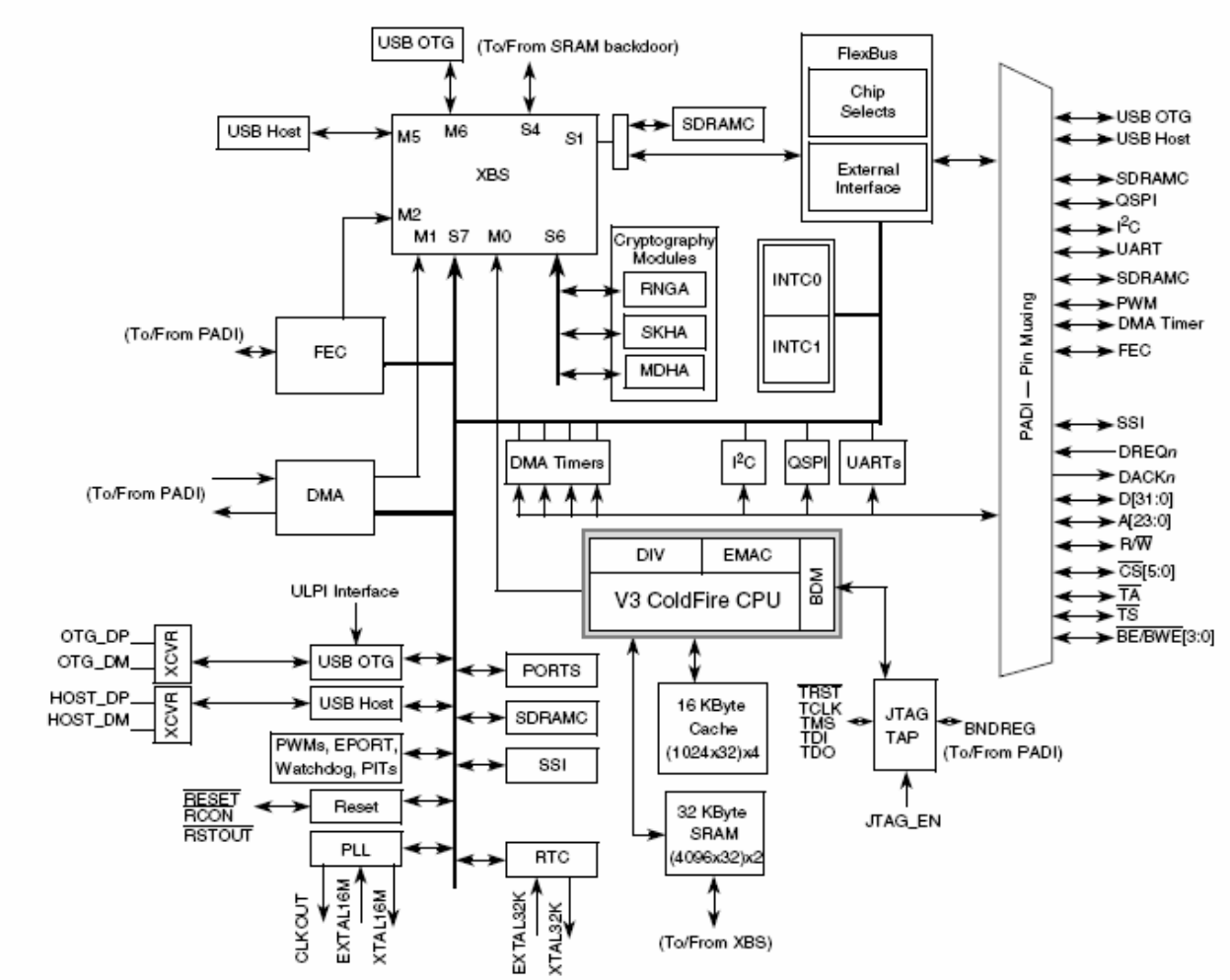


Figure 2.1: MCF5373L Microcontroller Block Diagram

2.2 Clocks

The MCF5373L requires two crystals in order to enable proper internal timing. A 16.000 MHz crystal is used to generate many of the processor's internal clocks via a series of PLLs and signal dividers. To generate the core CPU clock, the 16.000 MHz signal is run through a PLL controlled by the PLL Feedback Divider Register (PFDR). Divisors are used to divide down the internal bus frequency to set the memory controller, quick capture interface, and DMA controller.

IMPORTANT NOTE: Please see Freescale's *MCF5373 Reference Manual* for additional information about processor clocking.

The second required crystal runs at 32.768 kHz. The 32.768 kHz clock is used as a reference clock for the Real Time Clock (RTC) Module.

The MCF5373L's microcontroller core clock speed is initialized to 240 MHz on the Fire Engine. The SDRAM bus speed is set at 80 MHz in LogicLoader. Other clock speeds can be supported and modified in software for specific user applications, such as specific serial baud rates.

The MCF5373-10 Fire Engine provides an external bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector. The uP_BUS_CLK, which is connected to the processor's FB_CLK, is set to a

default of 80 MHz. uP_SD_CLK and uP_SD_nCLK serve as the SDRAM clocks on the MCF5373-10 Fire Engine.

MCF5373L Microcontroller Signal Name	MCF5373-10 Fire Engine Net Name	Default Software Value in LogicLoader
CORE	N/A	240 MHz
Internal bus	N/A	80 MHz
SD_CLK	uP_SD_CLK	80 MHz
SD_CLK_b	uP_SD_nCLK	80 MHz

2.3 Memory

2.3.1 DDR Synchronous DRAM

The MCF5373-10 Fire Engine uses a 16-bit memory bus to interface to DDR SDRAM. The memory can be configured as 16, 32, or 64 MB in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on the SDK board is specified as 32 MB.

2.3.2 Direct Memory Access (DMA)

The Freescale MCF5373L microcontroller has an internal DMA controller. These channels can be used to interface streams from internal peripherals to the system memory (including USB, I2S, etc.). The DMA controller can also be used to interface streams from memory-to-memory or memory-to-external-peripheral using two dedicated external channels. External handshake signals are available to support transfers to and from external peripherals. For more information on using the DMA interface refer to the *MCF5373 Reference Manual*.

2.3.3 NOR Flash

The MCF5373-10 Fire Engine uses a 16-bit memory bus to interface to NOR flash memory chips. The onboard Fire Engine memory can be configured as 1, 2, or 4 MB to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 2 MB on the SDK. Because flash is one of the most expensive components on the MCF5373-10 Fire Engine, it is important to contact Logic when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, CompactFlash, or NAND flash. See the Zoom ColdFire SDK Development Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND Flash

The MCF5373-10 Fire Engine uses an 8-bit memory bus to interface to NAND flash. The product supports configurations of 16, 32, 64 MB, and other sizes, depending on NAND availability. The standard development kit is provided with 16 MB of NAND flash. Please contact Logic for more information.

2.3.5 CompactFlash (memory-mapped mode only)

The MCF5373-10 Fire Engine supports a CompactFlash memory-mapped mode only slot. The MCF5373-10 Fire Engine uses internal logic to provide the necessary signals for a CompactFlash card interface in memory-mapped mode only. The internal logic delays the rising edge of CF_nCE by two clock cycles to meet CompactFlash timing. The address hold time for uP_nCS1 must be extended two clock cycles beyond deassertion of uP_nCS1 to prevent bus conflicts. The nCHRDY

input signal to the Fire Engine can be asserted by CompactFlash. When pulled low, the nCHRDY signal generates a low on the uP_nWAIT signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. The Zoom ColdFire SDK Development Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. If hot-swappable capability is desired, it can be achieved by adding additional hardware to the user's baseboard.

2.4 10/100 Ethernet Controller

The MCF5373-10 Fire Engine uses the Fast Ethernet Controller (FEC) on the MCF5373L processor combined with the National Semiconductor® DP83848 10/100 single-chip Ethernet Transceiver to provide an easy-to-use networking interface. To facilitate use, six signals from the DP83848 are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LEDs. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the Zoom ColdFire SDK Development Kit for reference. Please note the TX+/- and RX+/- pairs must be routed as differential pairs on the PCB.

2.5 Audio Codec

The MCF5373L processor has a Synchronous Serial Interface (SSI) controller that can support AC97 and I2S formats. This SSI controller implements a 5-pin serial interface to the I2S audio codec, in this case the Texas Instruments (TI) TLV320DAC23. From the TI codec on the MCF5373-10 Fire Engine, the outputs are CODEC_OUTL and CODEC_OUTR. These signals are available from the 80-pin expansion connectors.

The TI codec on the MCF5373-10 Fire Engine performs up to full-duplex 24-bit codec functions and supports variable sample rates from 8k to 96k samples per second.

NOTE: The Freescale MCF5373-10 Fire Engine also offers an SSI interface for other codec devices. This interface provides a digital interface that is multiplexed with the signals from the SSI controller. If you are looking for an alternative codec option, Logic has previously interfaced different high-performance audio codecs into other Fire Engines. Contact Logic for assistance in selecting an appropriate audio codec for your application.

2.6 Serial Interface

The MCF5373-10 Fire Engine comes with the following serial channels: UARTA, UARTB, UART2, and QSPI. If additional serial channels are required, please contact Logic for reference designs. Please see the *MCF5373 Reference Manual* for further information regarding serial communications.

2.6.1 UARTA

UARTA has been configured to be the MCF5373-10 development kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Fire Engine are TTL level signals not RS232 level signals. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Zoom ColdFire SDK Development Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2Kbits/sec, though it supports most common serial baud rates. UARTA is available off the J1C 144-pin SO-DIMM connector.

2.6.2 UARTB

Serial Port UARTB is an asynchronous 16C550-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Fire Engine are TTL level signals, not RS232 level signals. The ColdFire SDK baseboard has a RS232 level shifter and can be accessed on P3 when the J9 jumpers are installed connecting pins 1-2, 3-4, and 5-6. UARTB's baud rate can also be set to most common serial baud rates. UARTB is available off the J1B 80-pin expansion connector.

2.6.3 QSPI

The Queued SPI interface is used on the Fire Engine to communicate with the onboard touch interface, as well as the onboard audio codec.

There is an additional uP_SPI_FRM signal brought offboard for customer use. The serial format is used to interface between the parallel data inside the SoC and synchronous serial communications on peripheral devices. The signals are available off the 144-pin SO-DIMM connector. Please see the MCF5373 microprocessor's Reference Manual for further information.

2.7 USB Interface

The MCF5373-10 Fire Engine is configured with both USB host and device functionality. The USB device interface is compliant to the USB 2.0 and the EHCI 1.0 specifications. This USB client supports full-speed (12 Mbits/sec) operation. The USB device interface on the MCF5373 is able to transmit data, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector.

The USB host interface is compatible with both the USB 2.0 and EHCI 1.0 specifications. This controller also supports both low-speed and full-speed USB devices. The USB connector signals are available off the J1A 80-pin connector. For more information on using both the USB device and host interfaces, please see the *MCF5373 Reference Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the MCF5373-10 Fire Engine, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 2.0 requirements specify that the impedance on each driver must be between 28 Ω and 44 Ω. For reference, see the impedance matching circuit on the Logic ColdFire SDK baseboard.

2.8 General Purpose I/O

Logic designed the MCF5373-10 Fire Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Fire Engine that interface to the MCF5373L. See the "Pin Descriptions" section of this Hardware Specification for more information. If certain peripherals are not desired, such as chip selects, IRQs, or UARTS, then multiple GPIO pins become available. Please see the table in Section 5.4 "Multiplexed Signal Trade-Offs" for a list of the available GPIO trade-offs.

2.9 Onboard Logic Interfaces

The onboard Logic interfaces are used to create additional functionality on the Fire Engine with the support of a few discrete logic components. The logic interface serves four main purposes: modify MCF5373L flex-bus signal timing to support standard CompactFlash cards, add 8 general purpose inputs and 8 general purpose outputs, provide memory map selection between the GPIO interface and the CompactFlash interface, and provide chip select qualified read and write signals for onboard NAND flash.

Memory Map:
The onboard Logic creates a 2-part memory map for the CPU's chip select 1 area. The base address is determined by the CSAR1 register. The base address of chip select 1 is also the base address of the CompactFlash interface. When chip select 1 is asserted and A19 is low, onboard logic modifies the flex-bus hardware signal timing to meet the CompactFlash specification. The recommended flex-bus settings for accessing CompactFlash and the external general purpose input/output bits are:
CSCR1 = 0x002A3780
CSMR1 = 0x001F0001

Chip Select	Offset	Device/feature
nCS1	+ 0x00	CompactFlash Interface
nCS1	+ 0x80000	External 8 bit GPIO port
nCS2	+ 0x00	NAND flash area

Accessing chip select area 1 with an address that asserts address line 19 high will cause an access to the external onboard 8-bit GPIO port. The GPIO port bits are listed here and correspond to actual external signals on the Fire Engine PCB. Note that reading and writing to a single bit may have different functions. For example, reading from bit 7 returns the state of the nSTANDBY signal, but writing to bit 7 changes the state of the uP_STATUS_1 signal.

Bit	7	6	5	4
Input (read)	nSTANDBY	nSUSPEND	LATCH_GPO_1	LCD_VEEEN
Output (write)	uP_STATUS_1	uP_STATUS_2	LATCH_GPO_1	LCD_VEEEN
Output Reset value	tri-state	tri-state	tri-state	tri-state

Bit	3	2	1	0
Input (read)	LATCH_GPO_2	WRLAN_nINT	nIRQD	uP_MODE2
Output (write)	LATCH_GPO_2	NAND_nGPIO	uP_USB2_PWR_EN	uP_USB1_PWR_EN
Output Reset value	tri-state	tri-state	tri-state	tri-state

GPIO port initialization:
The 8 GPIO outputs are in tri-state by default after a CPU reset. To enable the GPIO outputs, first write the desired state of the outputs to the GPIO port at address chip select 1 + 0x80000. Then the processor GPIO TIN3/PTIMER3 signal should be driven low, which will enable all 8 GPIO outputs. This can be accomplished by clearing bits 6 and 7 in the PAR_TIMER register and clearing bit 3 in the PODR_TIMER register.

GPIO port signal definitions:

uP_MODE2 - Read only. Logic Loader software reads this pin to determine whether or not to skip user abort from any stored scripts. Tying this signal low will disable user aborts from scripts over the serial port. Refer to the *LogicLoader User's Manual* for additional information. This pin can also be used as a General Purpose input and read from the 8-bit GPIO port. This signal is pulled up to 3.3V through a 1.5K resistor.

uP_USB1_PWR_EN – Write only. Active low. Enables power supply for USB port 1.

nIRQD – Input only. Software can use as a hardware interrupt on MCF5373-10. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_USB2_PWR_EN – Write only. Active high. Enables USB port 2.

WRLAN_nINT – Read only. Active low. Hardware interrupt from the onboard Ethernet PHY. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

NAND_nGPIO – Write only. Active low. Driving this signal low will hold the NAND flash chip select low (NAND_nCE). See the following section for more details.

LATCH_GPO_2 – Read/Write. Writing to this bit will drive the external signal LATCH_GPO_2 to the desired state. Reading from this bit will return the current state of the LATCH_GPO_2 output.

LCD_VEEEN – Read/Write. Writing to this bit will drive the external signal LCD_VEEEN to the desired state. Reading from this bit will return the current state of the LCD_VEEEN output. This signal is typically used for controlling power to LCD backlight displays.

LATCH_GPO_1 – Read/Write. Writing to this bit will drive the external signal LATCH_GPO_1 to the desired state. Reading from this bit will return the current state of the LATCH_GPO_1 output.

nSUSPEND – Read only. Software can use as a hardware interrupt on the MCF5373-10. See Section 3.5.4.2 for suggested software implementation of the nSUSPEND signal. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_STATUS_2 – Write only. Writing to this bit will drive the external signal uP_STATUS_2 to the desired state. The uP_STATUS_1 and uP_STATUS_2 signals are used to drive the LEDs on the ColdFire SDK baseboard. Driving this signal low will turn on the LED.

nSTANDBY - Read only. Software can use as a hardware interrupt on the MCF5373-10. See section 3.5.4.3 for suggested software implementation of the nSTANDBY signal. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_STATUS_1 – Write only. Writing to this bit will drive the external signal uP_STATUS_1 to the desired state. The uP_STATUS_1 and uP_STATUS_2 signals are used to drive the LEDs on the ColdFire SDK baseboard. Driving this signal low will turn on the LED.

NAND flash:

The NAND flash chip base address is defined by chip select 2. Any reads or writes to the NAND flash chip are qualified by AND gates in U16. Using the NAND_nGPIO output defined in the onboard "GPIO port signal definitions" section above, software can hold the NAND chip select (NAND_nCE) signal low to allow for devices which require the chip select to be active during address pointer changes. The onboard logic allows the NAND address pointer change to occur without issues even while other devices chip selects are active.

2.10 Expansion/Feature Options

The MCF5373-10 Fire Engine was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. It is possible for a user to expand the Fire Engine's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the MCF5373L, but are not discussed herein, include: RTC, pulse width modulation (PWM), crypto unit, random number generator, enhanced multiply-accumulate (EMAC), and the debug module. See the *MCF5373 Reference Manual* and MCF5373L schematics for more details. Logic has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on Fire Engine boards. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The MCF5373-10 Fire Engine was designed to meet multiple applications for specific users and budget requirements. As a result, this Fire Engine supports a variety of embedded operating systems and supports the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64 MB DDR SDRAM
- Flexible NOR flash footprint: 1, 2, or 4 MB NOR flash
- Flexible NAND flash footprint: 0, 16, 32, 64 MB, or larger NAND flash.
- Optional National Semiconductor DP83848 10/100 Ethernet controller
- Optional Texas Instruments TLV320DAC23 audio codec
- Optional Texas Instruments ADS7843 touch controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all Fire Engine peripheral hardware reset pins are connected to the MSTR_nRST_INT net. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the MCF5373-10 Fire Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power-on reset event to the MCF5373L and resets the entire CPU.

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details. The following two conditions will cause a system-wide reset: power on or a low pulse on the MSTR_nRST signal.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 1.0V and 3.08V. Once the 3.3V supply surpasses 3.08V the reset chip will trigger a rising edge of MSTR_nRST after a 140-460 ms delay (240 ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the MSTR_nRST signal, analog or digital, de-bouncing be used to generate a clean, one-shot reset signal.

3.3 Interrupts

The MCF5373L incorporates two interrupt controllers (INTC0 and INTC1). Through these two interrupt controllers the MCF5373L can prioritize and process up to 128 interrupts (not all used on this device). Each interrupt has its own unique vector number and its own unique interrupt control register (ICRnx) to define software-assigned levels. Refer to Freescale's Reference Manual covering the appropriate microprocessor for further information on using IRQ interrupts.

3.4 BDM Debugger Interface

The BDM connection on the MCF5373L allows recovery of corrupted flash memory and real-time application debug. When choosing a debugger board, remember that many different third-party BDM debuggers are available for Freescale ColdFire microcontrollers. The following signals make up the BDM interface to the MCF5373L: PST[3:0], DDATA[3:0], uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 26-pin 0.1" through-hole connector as shown on the ColdFire SDK baseboard reference schematics.

IMPORTANT NOTE: When laying out the 26-pin connector, realize it may not be numbered as a standard 26-pin 0.1" IDC through-hole connector. See MCF5373-10 ColdFire SDK Development Kit reference design for further details. Different BDM tool vendors define the 26-pin IDC connector pin-out differently.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the MCF5373-10 Fire Engine was designed to have the following power areas: 3.3V, 3.3VA, 3.3V_WRLAN, and 2.5V. All power areas are inputs to the Fire Engine with the exception of 3.3V_WRLAN, which is an output from the Fire Engine.

3.5.1.1 2.5V

The 2.5V input pins are connected to a 2.5V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 2.5V supply should be maintained above the minimum level at all costs (see "Electrical Specification", Section 2). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in Section 3.5.4.3 below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the MCF5373-10 Fire Engine. This supply must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification," unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the MCF5373L processor on the MCF5373-10 Fire Engine. The 3.3VA supply must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification", unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This “power” supply net is an output from the Fire Engine. The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the Fire Engine will try to power itself through the impedance matching resistors. Please see Logic’s ColdFire SDK reference design schematics for details.

3.5.1.5 1.5V (Internal to Fire Engine Only)

The module creates a 1.5V power plane for the CORE_VDD inputs on the MCF5373L. The 1.5V plane is powered from the 3.3V supply and is always on when 3.3V is available.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The MCF5373-10 Fire Engine was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the MCF5373L there are many different software configurations that drastically effect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes, microcontroller power management states (Run, Wait, Doze, and Stop), peripheral power states and modes, product user scenarios, and interrupt handling. These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents, such as the *LogicLoader User’s Manual* or the specific BSP manual.

3.5.3 Peripherals

Most peripherals provide software programmable power states. However, sometimes these programmable power states may not be the best solution.

The MCF5373-10 Fire Engine was designed to have the following four power areas: 3.3V, 3.3V_WRLAN, 3.3VA, and 2.5V for a flexible hardware design. See Figure 3.1, below.

Logic Net Name	Required Input VDC	Notes
3.3V	3.3VDC	Connects to the digital peripherals on the Fire Engine.
3.3VA	3.3VDC	Connects to the audio codec on the Fire Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
2.5V	2.5VDC	Connects to the onboard memory bus and DDR SDRAM.
3.3V_WRLAN	3.3V (this pin is an output, see Section 3.5.1.4)	Output from the Fire Engine that provides power to the offboard Ethernet circuitry.

Figure 3.1: Power Plane Diagram

3.5.4 Microcontroller

The MCF5373L processor power management's scheme was designed to be easy to use. There are four power management modes provided in the MCF5373L microcontroller: Run, Wait, Doze, and Stop. Logic Product Development BSPs have simplified the power management scheme to three power states: Run, Suspend, and Standby. Please see the descriptions of all three states below, as well as the *MCF5373 Reference Manual*, for more details.

3.5.4.1 Run State

Run is the MCF5373-10 Fire Engine's normal operating state in which both oscillator inputs and all clocks are hardware enabled. The MCF5373L can enter Run mode from any state. A Standby to Run transition occurs on any valid wake up event. The assertion of MSTR_nRST or any enabled interrupt signal qualifies. All power supplies are active in this state. Please see the *MCF5373 Reference Manual* for further information.

3.5.4.2 Suspend State

Suspend state is the MCF5373-10 Fire Engine's hardware power down state, allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the MCF5373L is waiting for an event such as a keyboard input. The Suspend state is entered using Logic BSPs by asserting the nSUSPEND signal or through software. The Stop, Wait, or Doze state is entered. All power supplies remain active. System context is retained. An internal or external wakeup event can cause the processor to transition back to Run Mode. Please see the *MCF5373 Reference Manual* for further information.

3.5.4.3 Standby State

Standby state is the MCF5373-10 Fire Engine's lowest power state. This state is entered in Logic BSPs by asserting the nSTANDBY signal or through software. The MCF5373L processor is put into Stop state. All clocks are stopped. System reboot is required if 3.3V power is removed. 3.3V power can be removed from the Fire Engine. The 2.5V power rail should be maintained if the DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause transition back to run state if 3.3V is not powered down, otherwise a system reset is required because context is lost when 3.3V power is removed.

3.6 ESD Considerations

The MCF5373-10 Fire Engine was designed to interface to a customer's peripheral board. The Fire Engine was designed to be low cost and adaptable to many different applications. The MCF5373-10 Fire Engine does not provide any onboard ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

On the Freescale ColdFire MCF5373L microcontroller, all address mapping is accomplished through the use of several Address pointer registers. Please consult the *MCF5373 Reference Manual* for details.

FlexBus:

Mapped “Chip Select” signals for the FlexBus are available as outputs from the microcontroller and are assigned as follows:

FB_CS0# = NOR flash (boot, 1 MB, 2 MB, 4 MB, or 8 MB)
FB_CS1# = CompactFlash and registers
FB_CS2# = NAND flash (16 MB, 32 MB, or 64 MB)
FB_CS3# = Available for use by an external device (VIDEO_nCS, host board)
FB_CS4# = Available for use by an external device (FAST_nCS, host board)
FB_CS5# = Available for use by an external device (SLOW_nCS, host board)

DDR RAM Chip Select lines:
SD_CS0 = DDR RAM
SD_CS1 = Not used

Please consult the *LogicLoader User’s Manual* and the *LogicLoader User’s Manual Addendum* for the MCF5373-10 for complete memory map information.

5 MCF5373-10 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of LogicLoader (bootloader). Many of the signals defined in the tables below can be configured as input or outputs—all GPIOs on the MCF5373L can be configured as either inputs or outputs—and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

In addition, keep in mind that the following mode line numbers on the Fire Engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of volatile memory. Refer to the reset description found in Section 3.2.1 for more information on how this signal is driven. Every peripheral on the Fire Engine with a reset line is reset with the assertion of this signal because the MCF5373 asserts MSTR_nRST_INT (RST_OUT_b) when MSTR_nRST (nRESET) is driven low. Refer to MCF5373L processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V through a 1.5K resistor.
3	ETHER_RX(+)	I	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4		NC	No internal connection (not implemented on the MCF5373-10)
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nCS	O	Active Low. Chip select for area 4 of MCF5373-10 memory, the "fast" peripheral chip select area. See memory map for details. This signal is connected to the FB_CS4_b signal of the processor. This signal is not used by Logic BSPs and is available for users. See memory map for details.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8	SLOW_nCS	O	Active Low. Chip select for area 5 of MCF5373-10 memory, the “slow” peripheral chip select area. See memory map for details. This signal is connected to the FB_CS5_b signal of the processor. This signal is not used by Logic BSPs and is available for users. See memory map for details.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nMCS	O	Active Low. Chip select for area 3 of MCF5373-10 memory. This is the "video" chip select area. This signal is not used by Logic BSPs and is available for users. See memory map for details.
11	nACT_LED/LAN_LED1	O	Active Low output. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
2	BOOT_nCS	O	Active Low. This signal is the chip select for boot ROM in area 0 when uP_MODE3 is low. When uP_MODE3 is high, this signal is inactive. See memory map for addressing details.
13	nLNK_LED/LAN_LED2	O	Active Low output. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR (uP_nMWE1)	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in.

Pin #	Signal Name	I/O	Description
15	nSTANDBY	O	Active Low. CPU power mode signal. Software can use nSTANDBY signal to make the Fire Engine enter a standby state (hardware power down), MCF5373 Deep Sleep Mode, where the contents of the SDRAM are placed in self-refresh and will be maintained. From standby, run is entered in response to an internal or external wakeup events. Software must be implemented in order for this signal to operate properly. This signal is pulled up to 3.3V through a 1.5K resistor.
16	nIORD (uP_nMRD)	O	Active Low. This signal is driven by the CPU request for an I/O resource to drive data onto the data bus during the cycle.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else.
19	3.3V	I	Power Supply (3.3V)
20		NC	No internal connection (not implemented on the MCF5373-10)
21	uP_nIRQC	I	This CPU power mode signal causes Run state to be entered from Suspend or Standby state if implemented in software. This signal is tied to the processor's uP_nIRQC signal when R74 is present (default). This signal is pulled up to 3.3V through a 10K resistor.
22	nCHRDY	I	Active Low. The I/O channel ready signal line serves to drive the asynchronous ready signal on the CompactFlash circuit low when additional cycle time is required. Push/Pull or open drain assertion of this signal are acceptable. This signal is pulled up to 3.3V through a 10K resistor.
23	nIRQD	I	Software can use as a hardware interrupt on MCF5373-10. This signal is pulled up to 3.3V through a 1.5k resistor.
24	uP_TEST1	I	This signal is connected to JTAG_EN on the processor. This signal needs to be pulled low for background debug mode (BDM) or pulled high for JTAG mode. Please see the *MCF5373 Reference Manual* for more details. This signal is pulled down to DGND through a 10k resistor.
25	uP_nIRQC	I	Software can use as a hardware interrupt on MCF5373-10. May also be configured as a GPIO pin. Note: This signal is connected to uP_nWAKEUP when R74 is present. This signal is pulled up to 3.3V through a 10K resistor.
26		NC	No internal connection (not implemented on the MCF5373-10)
27	uP_nIRQC	I	R75 not populated by default. Software can use as a hardware interrupt on MCF5373-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 10K resistor.
28	uP_nTRST	I	Active Low. This signal is pulled up to 3.3V through a 10K resistor.
29	uP_nIRQA	I	Software can use as a hardware interrupt on MCF5373-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 10K resistor.
30	uP_TMS	I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
31		NC	No internal connection (not implemented on the MCF5373-10)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use. This signal is pulled up to 3.3V through a 10K resistor.
33		NC	No internal connection (not implemented on the MCF5373-10)
34	uP_TDI	I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
35		NC	No internal connection (not implemented on the MCF5373-10)
36	uP_TCK	I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
37	uP_nWAIT	O	Active low. This is the processor's TA signal. This signal is used by the FlexBus memory area to extend bus cycles beyond standard wait state cycles. This signal is also driven low by the CF I/O Ready signal (nCHRDY). This signal is pulled up to 2.5V through a 1.5K resistor.
38	uP_MODE3	I	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished by onboard logic: if signal uP_MODE3 is high, then FLASH_nCS = uP_nCS0; if signal uP_MODE3 is low, then BOOT_nCS = uP_nCS0. This defaults to the onboard flash if left unconnected (pulled to 3.3V through a 10K resistor).

Pin #	Signal Name	I/O	Description
39	uP_UARTA_RTS	O	Ready to Send line for the UART 0 interface.
40	uP_MODE2	I	LogicLoader software reads this pin to determine whether or not to skip user abort from any stored scripts. Tying this signal low will disable user aborts from scripts over the serial port. Refer to the *LogicLoader User's Manual* for additional information. This pin can also be used as a General Purpose input and read from the CPLD register. This signal is pulled up to 3.3V through a 1.5K resistor.
41	uP_UARTA_CTS	I	UART 0 clear to send on the MCF5373L.
42		NC	No internal connection (not implemented on the MCF5373-10)
43	uP_UARTA_TX	O	UART 0 transmit output signal on the MCF5373L.
44		NC	No internal connection (not implemented on the MCF5373-10)
45	uP_UARTA_RX	I	UART 0 receive input signal on the MCF5373L.
46		NC	No internal connection (not implemented on the MCF5373-10)
47		NC	No internal connection (not implemented on the MCF5373-10)
48	MFP12 – TIN0/TOUT0/DREQ0	I/O	The DMA Request 0 line.
49		NC	No internal connection (not implemented on the MCF5373-10)
50		NC	No internal connection (not implemented on the MCF5373-10)
51	nSUSPEND	I	Active low. Software can use this signal to suspend MCF5373L operations. This pin is pulled up to 3.3V by a 1.5k resistor. Software is required for proper suspend operation.
52		NC	No internal connection (not implemented on the MCF5373-10)
53	uP_AUX_CLK	O	This signal is connected to FB_CLK on the processor, which is also connected to uP_BUS_CLK. This clock operates at 80 MHz.
54		NC	No internal connection (not implemented on the MCF5373-10)
55	DGND	I	Digital Ground (0V)
56	uP_DACK0	O	The DMA Acknowledge 0 line.
57	VCORE (2.5V)	I	CPU core voltage supply (on during low power). VCORE should be set to 2.5V.
58	VCORE (2.5V)	I	CPU core voltage supply (on during low power). VCORE should be set to 2.5V.
59	VCORE (2.5V)	I	CPU core voltage supply (on during low power). VCORE should be set to 2.5V.
60	VCORE (2.5V)	I	CPU core voltage supply (on during low power). VCORE should be set to 2.5V.
61	3.3V	I	Power Supply (3.3V)
62	3.3V	I	Power Supply (3.3V)
63	3.3V	I	Power Supply (3.3V)
64	3.3V	I	Power Supply (3.3V)
65	uP_SPI_FRM	O	Software controlled QSPI framing signal. This signal may be used by application software to frame QSPI data transmission or reception.
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 80 MHz and is connected to the uP_AUX_CLK.
67	uP_SPI_TX	O	This output transmits synchronous QSPI data.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_RX	I	This input receives synchronous QSPI data.
70		NC	No internal connection (not implemented on the MCF5373-10)
71	uP_SPI_SCK	O	QSPI clock signal.
72		NC	No internal connection (not implemented on the MCF5373-10)
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74	uP_nMWE3	O	This is the buffered Byte Lane Enable 3 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2	O	This is the buffered Byte Lane Enable 2 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
77	uP_MD2	I/O	Buffered Data Bus bit 2.

Pin #	Signal Name	I/O	Description
78	uP_nMWE1	O	This is the buffered Byte Lane Enable 1 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0	O	This is the buffered Byte Lane Enable 0 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active low for Writes. This buffered signal is the processor's RW_b signal.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	Active low. This buffered signal is the processor's read enable line.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the MCF5373-10)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection (not implemented on the MCF5373-10)
89	DGND	I	Digital Ground (0V)
90	uP_MA0	O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	O	Buffered Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)
108	uP_MA9	O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	O	Buffered Address Bus bit 10.
111		NC	No internal connection (not implemented on the MCF5373-10)
112	uP_MA11	O	Buffered Address Bus bit 11.
113		NC	No internal connection (not implemented on the MCF5373-10)
114	uP_MA12	O	Buffered Address Bus bit 12.
115		NC	No internal connection (not implemented on the MCF5373-10)
116	uP_MA13	O	Buffered Address Bus bit 13.
117		NC	No internal connection (not implemented on the MCF5373-10)
118	uP_MA14	O	Buffered Address Bus bit 14.
119		NC	No internal connection (not implemented on the MCF5373-10)
120	uP_MA15	O	Buffered Address Bus bit 15.
121		NC	No internal connection (not implemented on the MCF5373-10)
122	uP_MA16	O	Buffered Address Bus bit 16.
123		NC	No internal connection (not implemented on the MCF5373-10)
124	uP_MA17	O	Buffered Address Bus bit 17.
125		NC	No internal connection (not implemented on the MCF5373-10)
126	uP_MA18	O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)

Pin #	Signal Name	I/O	Description
128	uP_MA19	O	Buffered Address Bus bit 19.
129		NC	No internal connection (not implemented on the MCF5373-10)
130	uP_MA20	O	Buffered Address Bus bit 20.
131		NC	No internal connection (not implemented on the MCF5373-10)
132	uP_MA21	O	Buffered Address Bus bit 21.
133		NC	No internal connection (not implemented on the MCF5373-10)
134	uP_MA22	O	Buffered Address Bus bit 22.
135		NC	No internal connection (not implemented on the MCF5373-10)
136	uP_MA23	O	Buffered Address Bus bit 23.
137		NC	No internal connection (not implemented on the MCF5373-10)
138	DGND	I	Digital Ground (0V)
139		NC	No internal connection (not implemented on the MCF5373-10)
140	uP_MA23	O	Buffered Address Bus bit 23.
141		NC	No internal connection (not implemented on the MCF5373-10)
142		NC	No internal connection (not implemented on the MCF5373-10)
143		NC	No internal connection (not implemented on the MCF5373-10)
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1		NC	No internal connection (not implemented on the MCF5373-10)
2		NC	No internal connection (not implemented on the MCF5373-10)
3		NC	No internal connection (not implemented on the MCF5373-10)
4		NC	No internal connection (not implemented on the MCF5373-10)
5		NC	No internal connection (not implemented on the MCF5373-10)
6	LCD_VEEEN	O	Active high. This signal is the enable for the LCD panel Vee.
7		NC	No internal connection (not implemented on the MCF5373-10)
8		NC	No internal connection (not implemented on the MCF5373-10)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the MCF5373-10)
11		NC	No internal connection (not implemented on the MCF5373-10)
12		NC	No internal connection (not implemented on the MCF5373-10)
13		NC	No internal connection (not implemented on the MCF5373-10)
14		NC	No internal connection (not implemented on the MCF5373-10)
15		NC	No internal connection (not implemented on the MCF5373-10)
16		NC	No internal connection (not implemented on the MCF5373-10)
17	uP_STATUS_1	O	This signal is attached to onboard logic. LoLo uses this signal to output status information on the SDK LEDs. This signal can be accessed through the onboard latch, see the “Onboard Logic Interfaces” Section for further information.
18	uP_STATUS_2	O	This signal is attached to onboard logic. LoLo uses this signal to output status information on the SDK LEDs. This signal can be accessed through the onboard latch, see the “Onboard Logic Interfaces” Section for further information.
19	uP_UARTB_CTS-uP_I2S_BCK	O	Clock signal to an I2S compliant audio codec.
20		NC	No internal connection (not implemented on the MCF5373-10)
21	uP_UARTB_RTS-uP_I2S_SWS	O	This signal is the I2S sync output to an I2S compliant audio codec.
22	uP_UARTB_RX-uP_I2S_RX	I	This signal is the I2S input to the processor from the I2S compliant audio codec.
23	uP_UARTB_TX-uP_I2S_TX	O	This signal is the I2S output from the processor to the I2S compliant audio codec.
24	DGND	I	Digital Ground (0V)
25	A/D1	I	This signal is the input to channel 3 of the touch chip’s 12-bit A/D converter.
26	A/D2	I	This signal is the input to channel 4 of the touch chip’s 12-bit A/D converter.
27	AGND	I	Analog Ground (0V)
28	HP_OUTL	O	Left stereo mixer-channel amplified headphone output. Please see the Texas Instruments TLV320DAC23 Data Manual for more details.
29	HP_OUTR	O	Right stereo mixer-channel amplified headphone output. Please see the Texas Instruments TLV320DAC23 Data Manual for more details.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio codec.
32	CODEC_INR	I	Right channel stereo line input of the audio codec.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Texas Instruments TLV320DAC23 Data Manual for more details.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Texas Instruments TLV320DAC23 Data Manual for more details.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch screen controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch screen controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch screen controller.
39	TOUCH_TOP	I	This is the X- position input to the four-wire resistive touch screen controller.
40	3.3VA	I	Analog Power Supply (3.3V)
41		NC	No internal connection (not implemented on the MCF5373-10)
42		NC	No internal connection (not implemented on the MCF5373-10)
43		NC	No internal connection (not implemented on the MCF5373-10)

Pin #	Signal Name	I/O	Description
44	DGND	I	Digital Ground (0V)
45		NC	No internal connection (not implemented on the MCF5373-10)
46		NC	No internal connection (not implemented on the MCF5373-10)
47		NC	No internal connection (not implemented on the MCF5373-10)
48		NC	No internal connection (not implemented on the MCF5373-10)
49		NC	No internal connection (not implemented on the MCF5373-10)
50		NC	No internal connection (not implemented on the MCF5373-10)
51		NC	No internal connection (not implemented on the MCF5373-10)
52		NC	No internal connection (not implemented on the MCF5373-10)
53		NC	No internal connection (not implemented on the MCF5373-10)
54		NC	No internal connection (not implemented on the MCF5373-10)
55	DGND	I	Digital Ground (0V)
56		NC	No internal connection (not implemented on the MCF5373-10)
57		NC	No internal connection (not implemented on the MCF5373-10)
58		NC	No internal connection (not implemented on the MCF5373-10)
59		NC	No internal connection (not implemented on the MCF5373-10)
60		NC	No internal connection (not implemented on the MCF5373-10)
61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. This signal can be accessed through the onboard logic devices, see the “Onboard Logic Interfaces” Section for further information.
62		NC	No internal connection (not implemented on the MCF5373-10)
63	LATCH_GPO_1	O	This signal is a general purpose output. It is controlled by a memory-mapped address on the onboard latch. This signal can be accessed through the onboard latch, see the “Onboard Logic Interfaces” Section for further information.
64	LATCH_GPO_2	O	This signal is a general purpose output. It is controlled by a memory-mapped address on the onboard latch. This signal can be accessed through the onboard latch, see the “Onboard Logic Interface” Section for further information.
65	uP_USB2_nOVR_CRNT-VBUS	I	Active low. This signal indicates an over current condition on the USB host. See ColdFire SDK application board schematics for recommended external USB circuitry. This signal is pulled up to 3.3V through a 10K resistor.
66	DGND	I	Digital Ground (0V)
67	uP_USB1_nOVR_CRNT-VBUS	I	Active high. This is the data carrier detect signal for the main USB port. It is used to determine whether or not the USB interface is currently in use. This signal is pulled down to DGND through a 100K resistor.
68	uP_USB2_PWR_EN	O	Active high. Enables USB port 2.
69	uP_USB1_PWR_EN	O	Active low. Enables power supply for USB port 1.
70	uP_USB2_M	I/O	USB port 2 data I/O minus. Route as a differential pair with uP_USB2_P.
71	uP_USB2_P	I/O	USB port 2 data I/O plus. Route as a differential pair with uP_USB2_M.
72	uP_USB1_M	I/O	USB port 1 data I/O minus. Route as a differential pair with uP_USB1_P.
73	uP_USB1_P	I/O	USB port 1 data I/O plus. Route as a differential pair with uP_USB1_M.
74	BUFF_nOE	I	Active low. This signal is the output enable for the data and address buffers on the Fire Engine. This signal is pulled down to DGND.
75	BUFF_DIR_ADDRESS	I	The BUFF_DIR_ADDRESS is low for the MCF5373-10 Fire Engine. This signal is pulled down to DGND.
76	BUFF_DIR_DATA (uP_nMWR)	O	Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle).
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the I2S compliant audio codec. Please see the Texas Instruments TLV320DAC23 Data Manual for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the Fire Engine. Please reference the Zoom ColdFire SDK reference schematics for details on implementation if the design may require support for different Fire Engines.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the Fire Engine. Please reference the Zoom ColdFire SDK reference schematics for details on implementation if the design may require support for different Fire Engines.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1		NC	No internal connection (not implemented on the MCF5373-10)
2		NC	No internal connection (not implemented on the MCF5373-10)
3		NC	No internal connection (not implemented on the MCF5373-10)
4		NC	No internal connection (not implemented on the MCF5373-10)
5		NC	No internal connection (not implemented on the MCF5373-10)
6		NC	No internal connection (not implemented on the MCF5373-10)
7		NC	No internal connection (not implemented on the MCF5373-10)
8		NC	No internal connection (not implemented on the MCF5373-10)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the MCF5373-10)
11	nCE1B	O	Tied to 3.3V on the Fire Engine.
12	nCE2B	O	Tied to 3.3V on the Fire Engine.
13		NC	No internal connection (not implemented on the MCF5373-10)
14		NC	No internal connection (not implemented on the MCF5373-10)
15		NC	No internal connection (not implemented on the MCF5373-10)
16		NC	No internal connection (not implemented on the MCF5373-10)
17		NC	No internal connection (not implemented on the MCF5373-10)
18		NC	No internal connection (not implemented on the MCF5373-10)
19		NC	No internal connection (not implemented on the MCF5373-10)
20		NC	No internal connection (not implemented on the MCF5373-10)
21	DGND	I	Digital Ground (0V)
22		NC	No internal connection (not implemented on the MCF5373-10)
23		NC	No internal connection (not implemented on the MCF5373-10)
24		NC	No internal connection (not implemented on the MCF5373-10)
25		NC	No internal connection (not implemented on the MCF5373-10)
26		NC	No internal connection (not implemented on the MCF5373-10)
27		NC	No internal connection (not implemented on the MCF5373-10)
28		NC	No internal connection (not implemented on the MCF5373-10)
29		NC	No internal connection (not implemented on the MCF5373-10)
30		NC	No internal connection (not implemented on the MCF5373-10)
31		NC	No internal connection (not implemented on the MCF5373-10)
32	DGND	I	Digital Ground (0V)
33	MFP1 - PST3	O	Processor status output 3. This signal can be used to read the core status. See MCF5373L processor datasheet for more information.
34	MFP2 - PST2	O	Processor status output 2. This signal can be used to read the core status. See MCF5373L processor datasheet for more information.
35	MFP3 - PST1	O	Processor status output 1. This signal can be used to read the core status. See MCF5373L processor datasheet for more information.
36	MFP4 - PST0	O	Processor status output 0. This signal can be used to read the core status. See MCF5373L processor datasheet for more information.
37	MFP5 – DDATA3	O	Debug data 3. This signal displays captured processor data and breakpoint status. See MCF5373L processor datasheet for more information.
38	MFP6 – DDATA2	O	Debug data 2. This signal displays captured processor data and breakpoint status. See MCF5373L processor datasheet for more information.
39	MFP7 – DDATA1	O	Debug data 1. This signal displays captured processor data and breakpoint status. See MCF5373L processor datasheet for more information.
40	MFP8 – DDATA0	O	Debug data 0. This signal displays captured processor data and breakpoint status. See MCF5373L processor datasheet for more information.
41	uP_UARTB_TX-uP_I2S_TX	O	High Speed UART transmit output signal on the MCF5373-10.
42	uP_UARTB_RX-uP_I2S_RX	I	High Speed UART receive input signal on the MCF5373-10.
43	uP_UARTB_CTS-uP_I2S_BCK	I	High Speed UART clear to send on the MCF5373-10.
44	DGND	I	Digital Ground (0V)

Pin #	Signal Name	I/O	Description
45	uP_UARTB_RTS-uP_I2S_SWS	O	High Speed UART request to send on the MCF5373-10.
46		NC	No internal connection (not implemented on the MCF5373-10)
47		NC	No internal connection (not implemented on the MCF5373-10)
48	MFP9 - TIN3/TOUT3	I/O	DMA timer input/output 3. This signal can be used for either a DMA timer input or a DMA timer output.
49	MFP10 - TIN2/TOUT2	I/O	DMA timer input/output 2. This signal can be used for either a DMA timer input or a DMA timer output.
50	MFP11 - TIN1/TOUT1	I/O	DMA timer input/output 1. This signal can be used for either a DMA timer input or a DMA timer output.
51	MFP12 - TIN0/TOUT0/DREQ0	I/O	DMA timer input/output 0. This signal can be used for either a DMA timer input or a DMA timer output.
52	MFP13 - WR_LAN_25CLK	O	This signal is a 25 MHz clock out from the National Semiconductor DP83848 Ethernet Controller. Refer to the National Semiconductor DP83848 datasheet for more information. Note: R17 needs to be populated for this signal to be sent off-board; R17 is not populated by default.
53		NC	No internal connection (not implemented on the MCF5373-10)
54		NC	No internal connection (not implemented on the MCF5373-10)
55	DGND	I	Digital Ground (0V)
56	MFP16/23 - CANTX/SCL	I/O	This signal is a mux of I2C Serial Clock Line and CAN transmit. See MCF5373L processor datasheet for muxing information.
57	MFP17/24 - CANRX/SDA	I/O	This signal is a mux of I2C Data/Address and CAN receive. See MCF5373L processor datasheet for muxing information.
58		NC	No internal connection (not implemented on the MCF5373-10)
59	MFP19 - PWM5	I/O	Pulse Width Modulated signal, channel 5.
60	nCE1A	O	Tied to 3.3V on the Fire Engine.
61	MFP21 - PWM1	I/O	Pulse Width Modulated signal, channel 1.
62	nCE2A	O	Tied to 3.3V on the Fire Engine.
63	MFP16/23 - CANTX/SCL	I/O	This signal is a mux of I2C Serial Clock Line and CAN transmit. See MCF5373L processor datasheet for muxing information.
64	MFP17/24 - CANRX/SDA	I/O	This signal is a mux of I2C Data/Address and CAN receive. See MCF5373L processor datasheet for muxing information.
65		NC	No internal connection (not implemented on the MCF5373-10)
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection (not implemented on the MCF5373-10)
68	MFP27 - PWM3	I/O	Pulse Width Modulated signal, channel 3.
69		NC	No internal connection (not implemented on the MCF5373-10)
70		NC	No internal connection (not implemented on the MCF5373-10)
71		NC	No internal connection (not implemented on the MCF5373-10)
72		NC	No internal connection (not implemented on the MCF5373-10)
73		NC	No internal connection (not implemented on the MCF5373-10)
74	MFP33 - PWM7	I/O	Pulse Width Modulated signal, channel 7.
75	MFP34 - nSYSEN	O	Active low. This signal activates the onboard voltage planes. This signal is pulled down to DGND through a 4.75K resistor.
76	MFP35 - CODEC_CLKOUT	O	This is the Clock Output from the Audio codec. Please see the Texas Instruments TLV320DAC23 Data Manual for more details. Note: This signal only goes offboard if R102 is present. Default is not present.
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the MCF5373-10)
79		NC	No internal connection (not implemented on the MCF5373-10)
80		NC	No internal connection (not implemented on the MCF5373-10)

5.4 Multiplexed Signal Trade-Offs

5.4.1 J1C Connector SODIMM 144-Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
6	FAST_nCS (FB_CS4_b)	FAST_nCS (FB_CS4_b)	Available Fast Chip Select	PCS4	GPIO PCS4
8	SLOW_nCS (FB_CS5_b)	SLOW_nCS (FB_CS5_b)	Available Slow Chip Select	PCS5	GPIO PCS5
10	VIDEO_nMCS (FB_CS3_b)	VIDEO_nMCS (FB_CS3_b)	Available Chip Select	PCS3	GPO PCS3
21,25	uP_IRQC	INT3	Interrupt 3 input	PINT3	GPIO PINT3
27	uP_IRQC	INT2	Interrupt 2 input	PINT2	GPIO PINT2
29	uP_IRQA	INT1	Interrupt 1 input	PINT1	GPIO PINT1
39	uP_UARTA_RTS	uP_UARTA_RTS	RTS signal for UART	PUARTL2	GPIO PUARTL2
41	uP_UARTA_CTS	uP_UARTA_CTS	CTS signal for UART	PUARTL3	PUARTL3
43	uP_UARTA_TX	uP_UARTA_TX	TX signal for UART	PUARTL1	PUARTL1
45	uP_UARTA_RX	uP_UARTA_RX	RX signal for UART	PUARTL0	PUARTL0
48	MFP-TIN0/TOUT0/DREQ0	uP_DREQ0	DREQ0 signal	PTIMER0	GPIO PTIMER0
65	uP_SPI_FRM	uP_SPI_FRM	QSPI framing signal	PQSPI3	GPIO PQSPI3

5.4.2 J1A Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
19	uP_UARTB_CTS-uP_I2S_BCK	uP_I2S_BCK	I2S Clock	PSSI3	GPIO PSSI3
21	uP_UARTB_RTS-uP_I2S_SWS	uP_I2S_SWS	I2S sync signal	PSSI2	GPIO PSSI2
22	uP_UARTB_RX-uP_I2S_RX	uP_I2S_RX	I2S in signal	PSSI1	GPIO PSSI1
23	uP_UARTB_TX-uP_I2S_TX	uP_I2S_TX	I2S out signal	PSSI0	GPIO PSSI0
65	uP_USB2_nOVR_CRNT-VBUS	uP_USB2_nOVR_CRNT-VBUS	USB Port 2 Over Current Detect	PIRQ7	GPIO PIRQ7
67	uP_USB1_nOVR_CRNT-VBUS	uP_USB1_nOVR_CRNT-VBUS	USB Port 1 VBUS	PIRQ6	GPIO PIRQ6

5.4.3 J1B Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
41	uP_UARTB_TX	uP_UARTB_TX	High Speed UART TX Output Only	PUART5	GPIO PUART5
42	uP_UARTB_RX	uP_UARTB_RX	High Speed UART RX Input Only	PUART4	GPIO PUART4
43	uP_UARTB_CTS	uP_UARTB_CTS	High Speed UART RX Clear To Send	PUART7	GPIO PUART7
45	uP_UARTB_RTS	uP_UARTB_RTS	High Speed UART Request To Send	PUART6	GPIO PUART6
48	MFP9-TIN3/TOUT3	PTIMER3	GPIO PTIMER3		
49	MFP10-TIN2/TOUT2	PTIMER2	GPIO PTIMER2		
50	MFP11-TIN1/TOUT1	PTIMER1	GPIO PTIMER1		
51	MFP12-TIN0/TOUT0/DREQ0	DREQ0	External DMA request 0	PTIMER0	GPIO PTIMER0
56,63	MFP16/23-CANTX/SCL	PFECI2C1	GPIO PFECI2C1		
57,64	MFP17/24-CANRX/SDA	PFECI2C0	GPIO PFECI2C0		
59	MFP19-PWM5	PWM5	PWM5 signal	PPWM5	GPIO PPWM5
61	MFP21-PWM1	PWM1	PWM1 signal	PPWM1	GPIO PPWM1
68	MFP27-PWM3	PWM3	PWM3 signal	PPWM3	GPIO PPWM3
74	MFP33-PWM7	PWM7	PWM7 signal	PPWM7	GPIO PPWM7

6 Mechanical Specifications

6.1 Interface Connectors

The MCF5373-10 Fire Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM connector must be 3.7mm mating height. Also in your baseboard design, please leave at least 7.65mm (0.3") of clearance between the Fire Engine's back edge (opposite of the SODIMM connector) and any board components in order to use an extractor tool for safe removal of the Fire Engine. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details on the extractor tool.

REF	Manufacturer	Fire Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(81)	DF12(3.0)-80DS-0.5V(81)
J1C	Amp	Card edge	390112-1

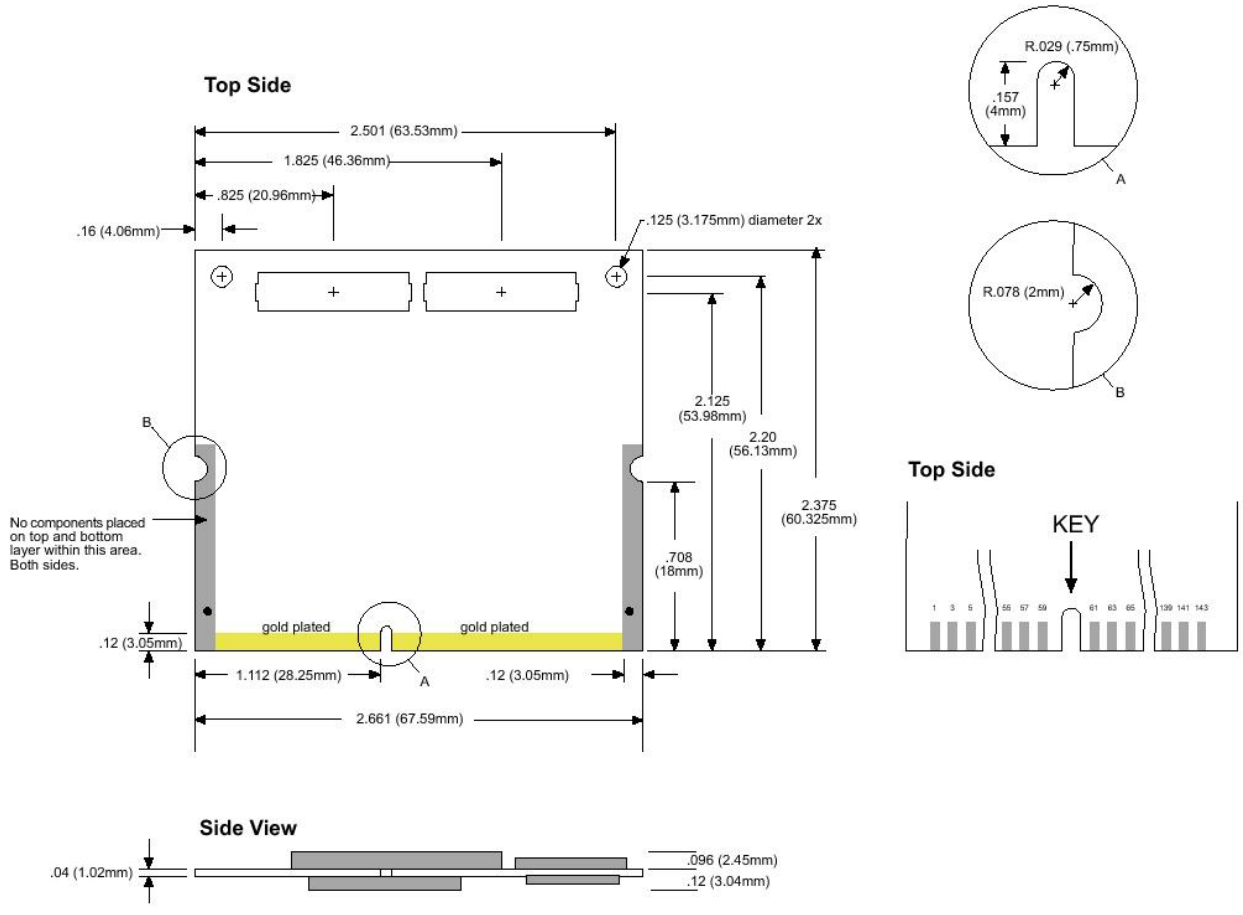


Figure 6.1: Fire Engine Mechanical Drawing

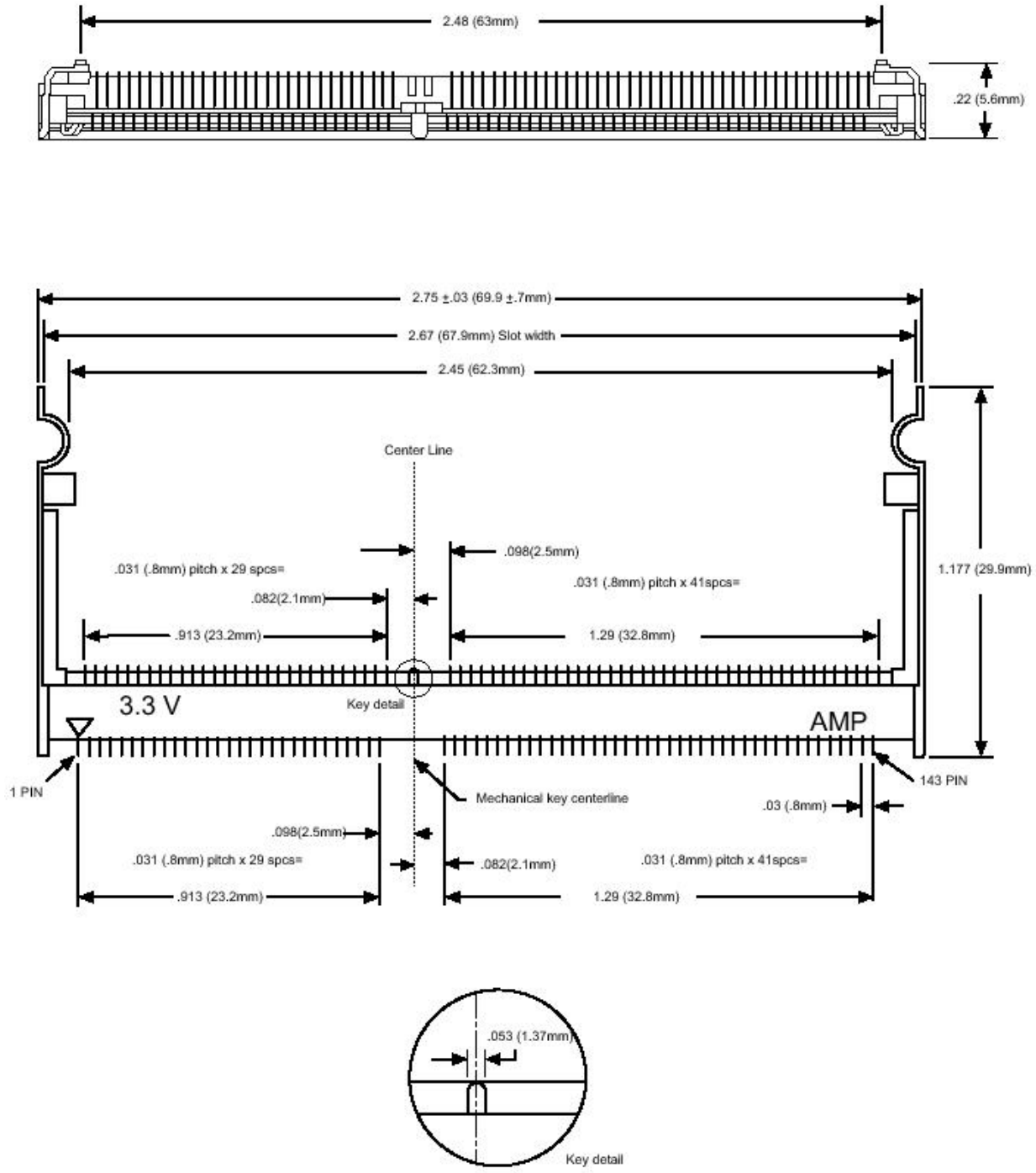


Figure 6.2: SODIMM Connector Specification

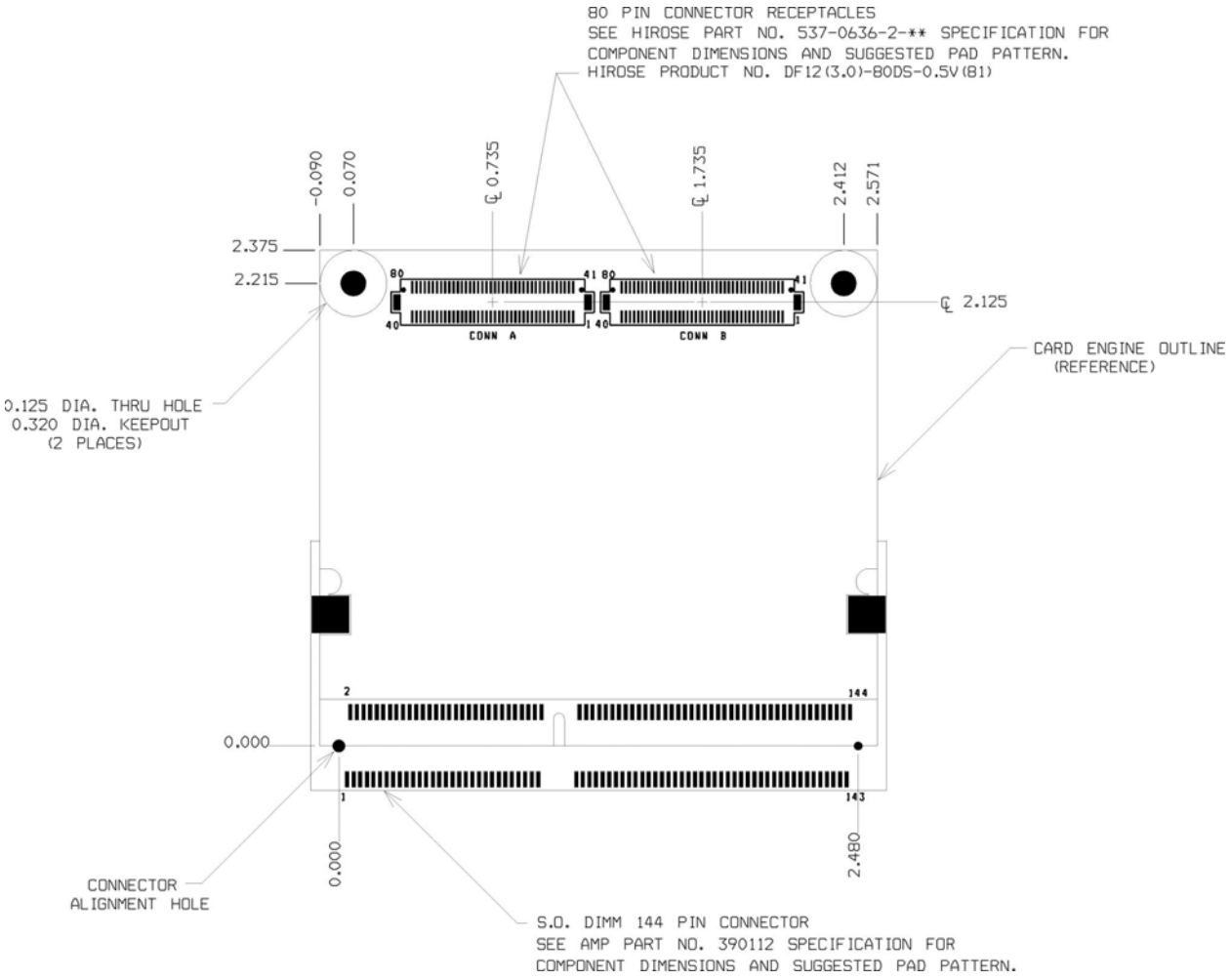


Figure 6.3: Recommended PCB Layout

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