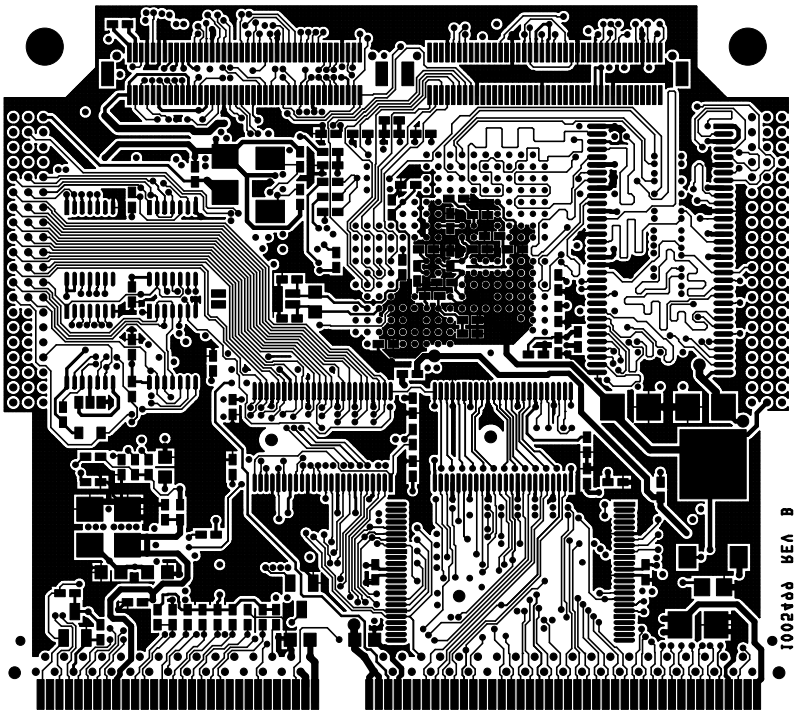
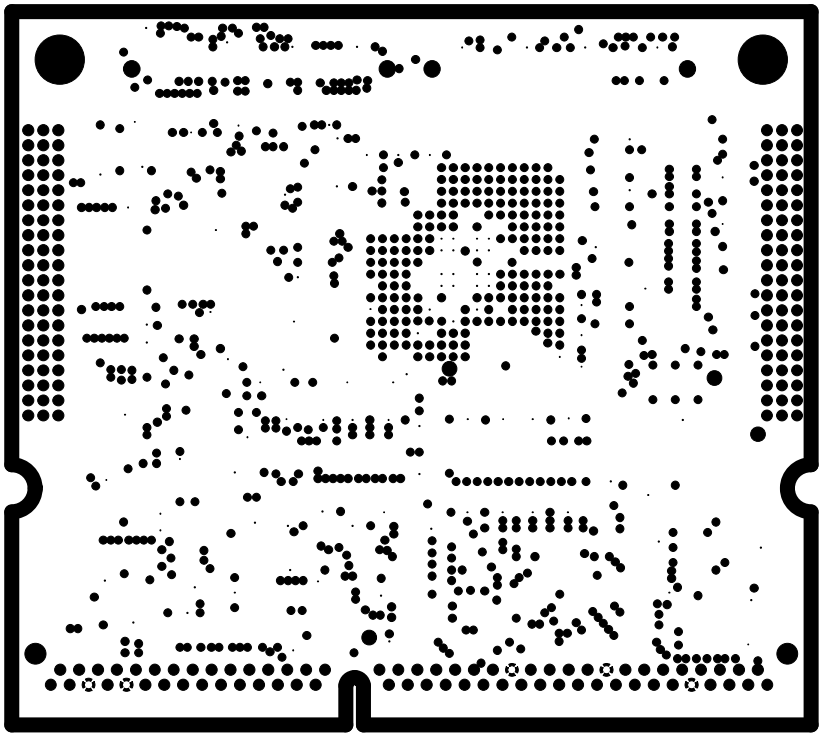


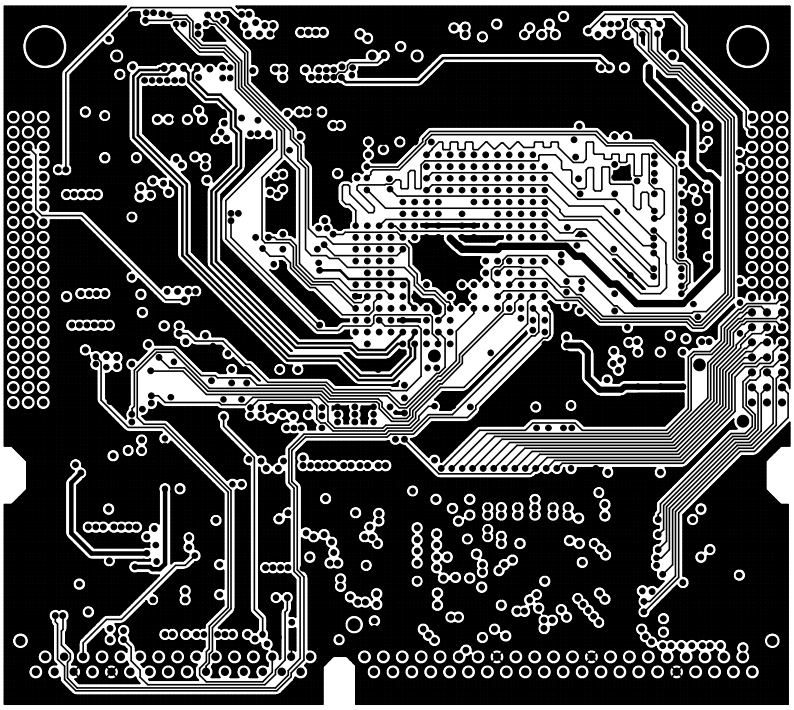
LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

LAYER 8 CIRCUIT BOTTOM SIDE



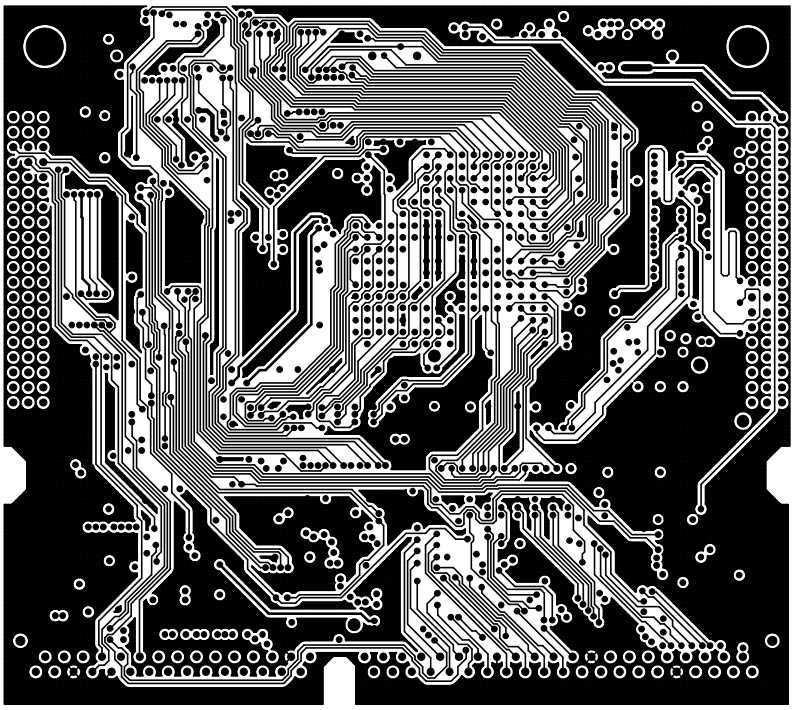
LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

LAYER 2 PLANE GND



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

LAYER 3 CIRCUIT



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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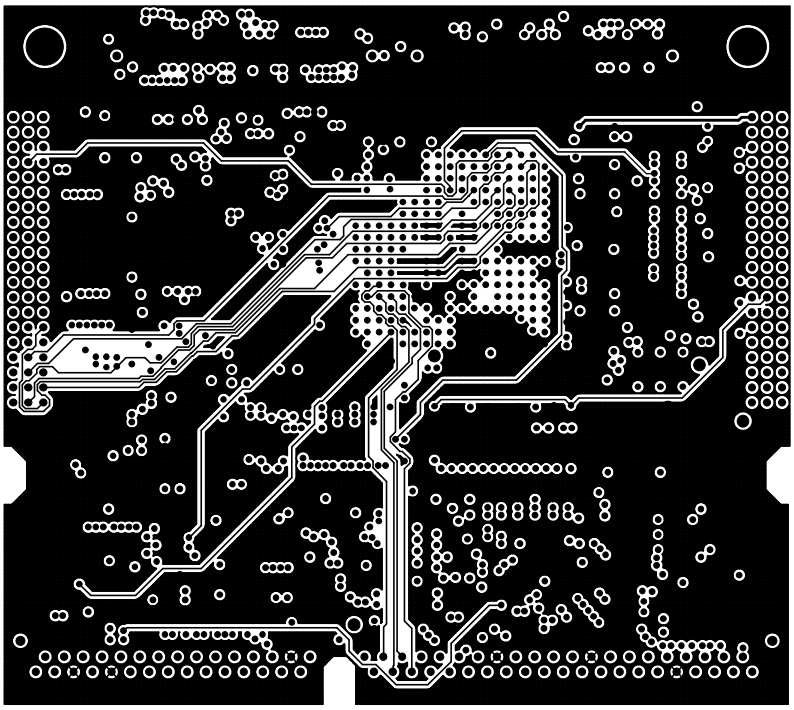
LAYER 6 CIRCUIT



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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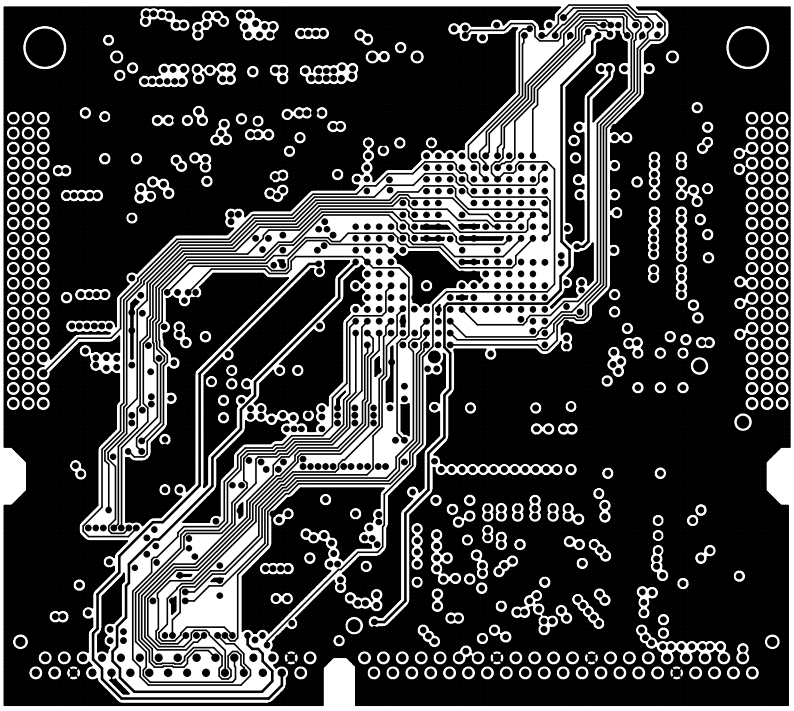
LAYER 5 CIRCUIT



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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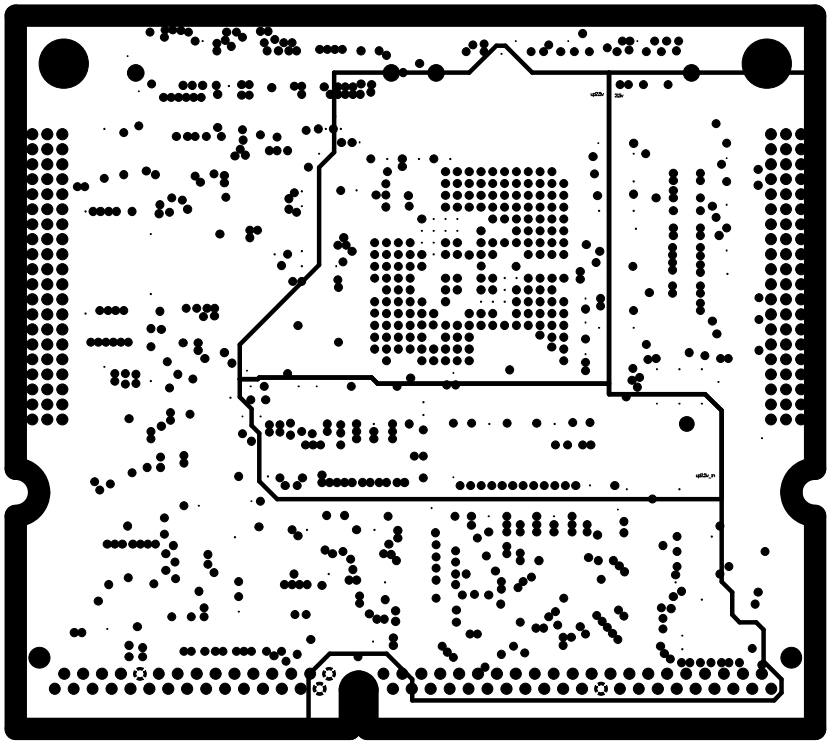
LAYER 4 CIRCUIT



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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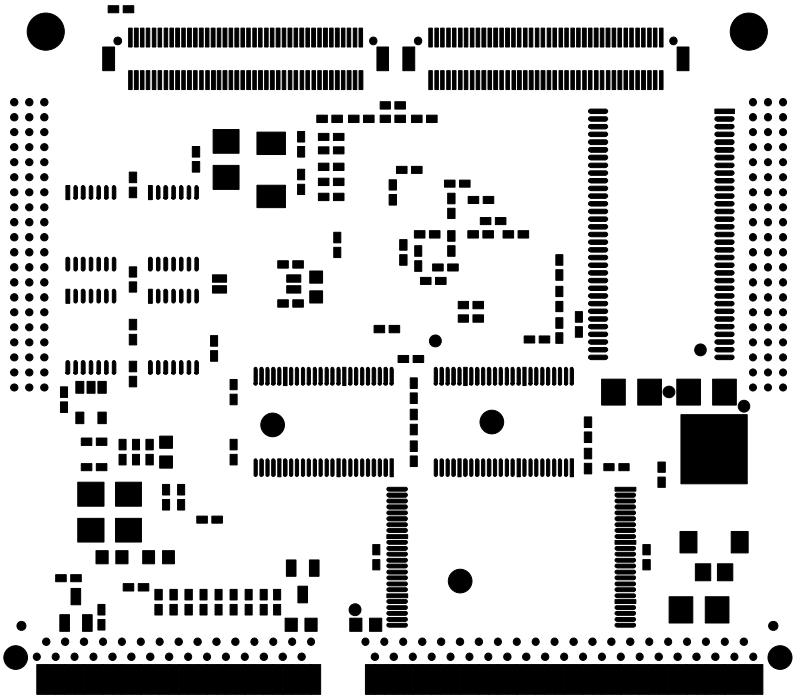
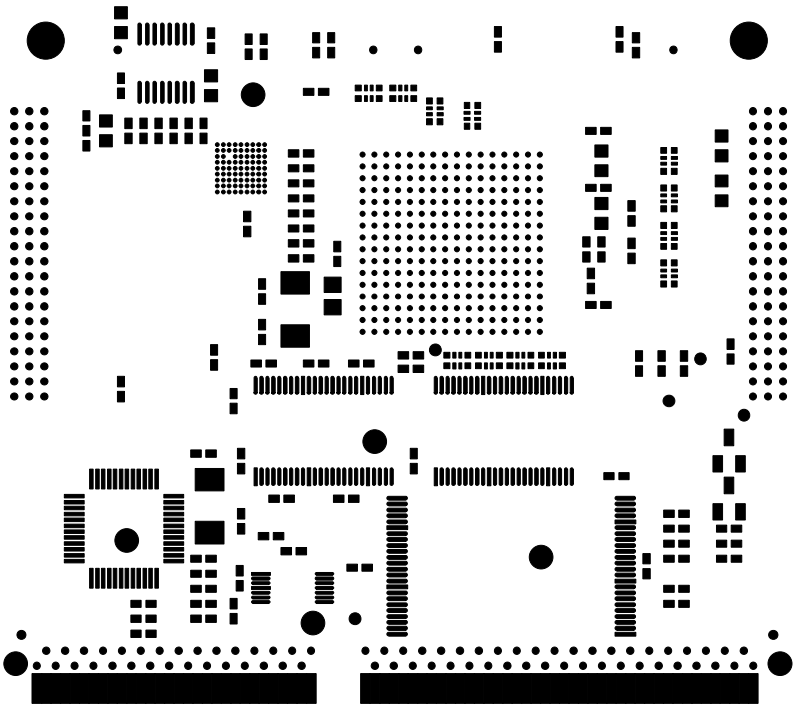
LAYER 7 PLANE POWER



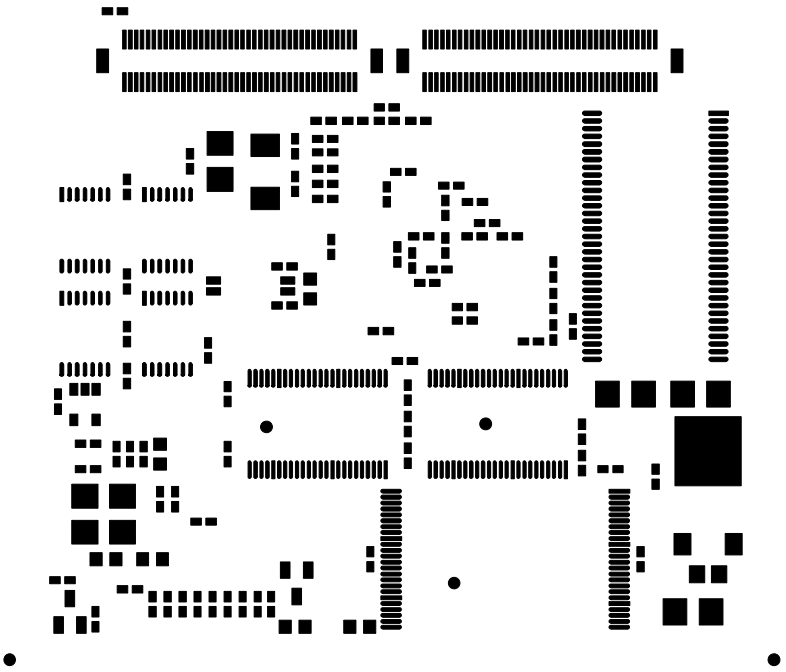
LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

SOLDER MASK BOTTOM SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

SOLDER MASK TOP SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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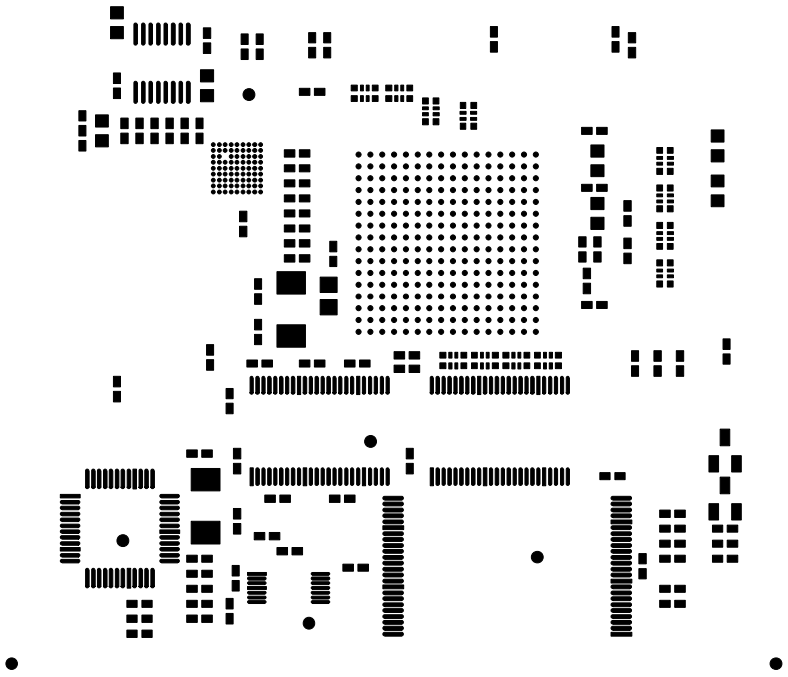
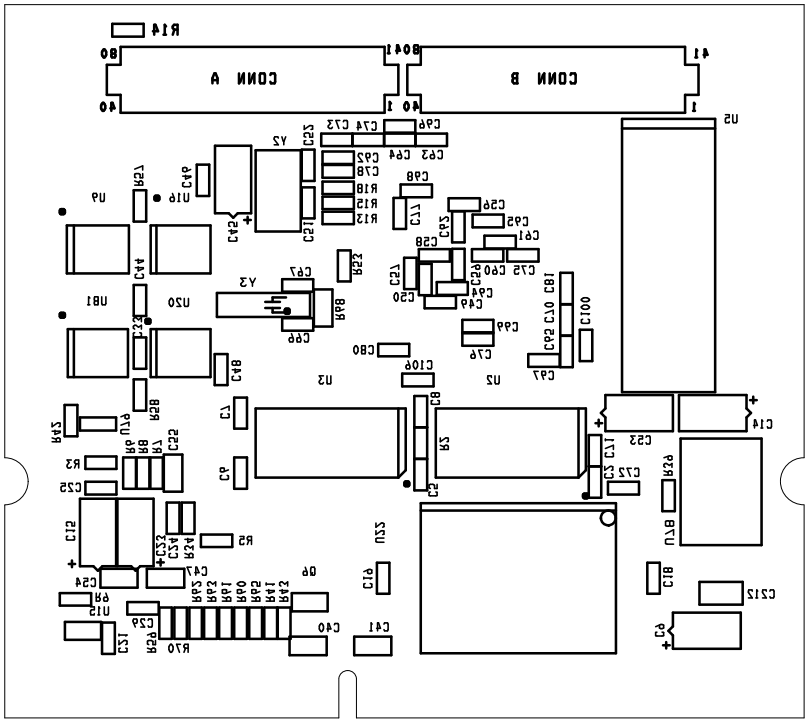
SOLDERPASTE BOTTOM SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

SOLDERPASTE TOP SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
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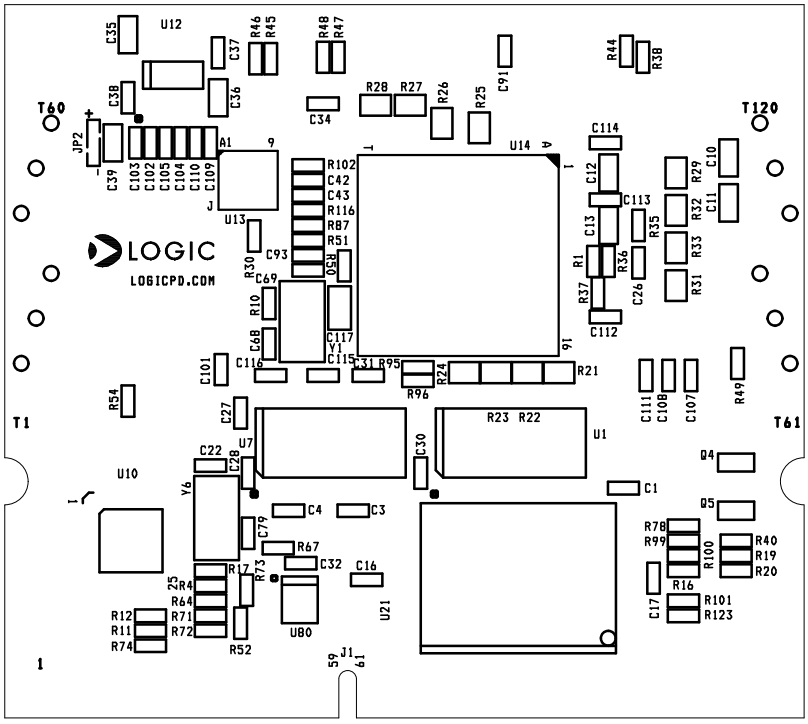
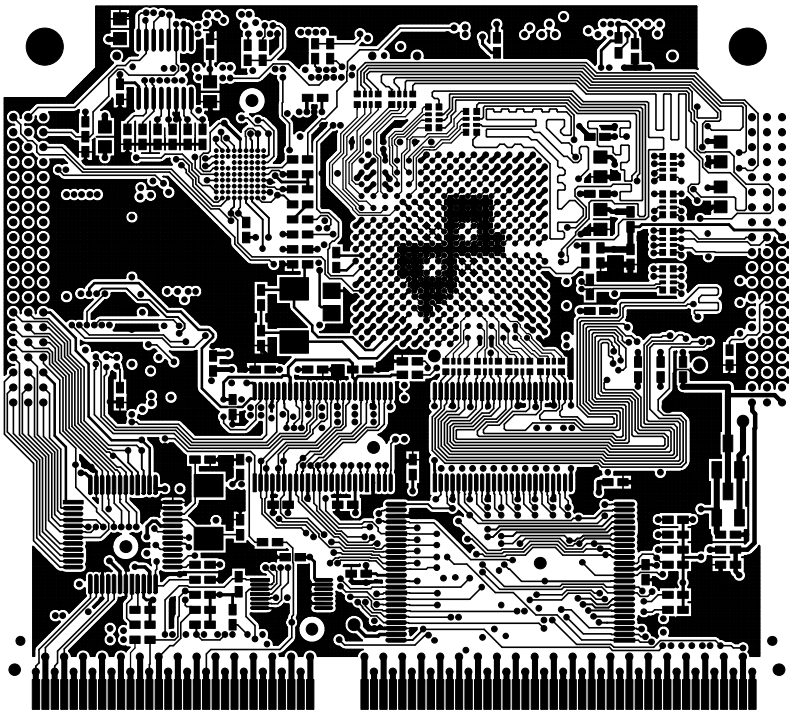
SILKSCREEN BOTTOM SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

SILKSCREEN TOP SIDE



LOGIC PRODUCT DEVELOPMENT
DRAGON FIRE CARD ENGINE
1005499 REV B
01-03-2007

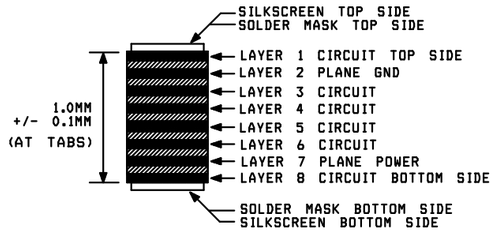
LAYER 1 CIRCUIT TOP SIDE

REVISION CHANGES

PART NO.	REV	DATE	CHANGES
1005499	A	12-29-2006	--
1005499	B	01-03-2007	SEE BELOW
1. REMOVED PB FREE MARKING FROM SILKSCREEN 2. CHANGED PLATING REQUIREMENT TO BE ImAg 3. UPDATED LOGIC LOGO TO NEW STYLE 4. CHANGED REVISION OF PCB FROM REV A TO REV B IN COPPER 5. INCREASED PAD WIDTH OF BGA FOOTPRINTS 2-4 MILS 6. INCREASED PASTE AND MASK LAYERS TO MATCH NEW BGA PAD SIZE 7. INCREASED FAN OUT TRACE WIDTH OF BGA CORNER PADS			

DRILL CHART

SYM	DIAM	TOL	QTY	NOTE
+	0.010	+0.000 -0.010	873	PLATED
x	0.012	+/- 0.003	192	PLATED
◇	0.020	+/- 0.003	5	PLATED
⊠	0.026	+/- 0.003	4	NON-PLATED
⊞	0.031	+/- 0.003	2	NON-PLATED
◈	0.125	+/- 0.003	2	NON-PLATED
TOTAL			1078	



8 LAYER STACK-UP

NOTE:

1. MATERIAL SELECTION:
   8 LAYER. EPOXY GLASS, NEMA GRADE FR-4, 1.0MM +/- 0.1MM THICK AT THE TABS.
   0.5 OZ. MINIMUM COPPER WITH SMOBC.
   THE PRINTED CIRCUIT BOARDS MANUFACTURED TO THIS DRAWING MUST BE RoHS COMPLIANT.
   ALTERNATIVE MATERIAL MUST BE APPROVED BY LOGIC/MDC PRIOR TO USE.
2. FINISH ON ALL SOLDERABLE SURFACES TO BE:
   IMMERSION SILVER (ImAg)
3. SOLDER RESIST: COLOR - BLUE (COLOR MUST BE APPROVED BY LOGIC PRIOR TO USE).
   THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH
   THE REQUIREMENTS OF IPC-SM-840.
   USE LIQUID PHOTOIMAGEABLE RESIST APPLIED OVER BARE COPPER.
   ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST.
   SOLDER RESIST BRIDGES 0.003" OR LESS MAY BE REMOVED.
4. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND
   TESTPOINT LANDS ARE TO BE FREE OF INK.
5. MANUFACTURER'S IDENTIFICATION: ADD TO SILKSCREEN ON BOTTOM SIDE.
6. ELECTRICAL BARE BOARD TEST REQUIRED.
7. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
8. BOARD VENDOR MAY REMOVE THERMALS FOR VIA'S ON PLANE LAYERS.
9. BOARD VENDOR MAY REMOVE NON FUNCTIONAL PADS ON INNER LAYERS.
10. BOARD VENDOR MAY ADD TEAR SHAPING TO INNER LAYERS.
    BOARD VENDOR TO ADD TEAR SHAPING TO OUTER LAYERS.
11. TABS TO BE GOLD PLATED 0.00003 (MINIMUM) THICK OVER
    NICKEL 0.0001 (MINIMUM) THICK.
12. BOARD IS A 4X ARRAY.
13. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG.
    AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
14. THEIVING STRUCTURES MAY BE ADDED TO COMPENSATE FOR VARIATIONS
    IN COPPER DENSITIES ACROSS THE PWB. SPACING BETWEEN THEIVING AND
    CONDUCTIVE PATTERN TO BE 0.020" MINIMUM.
15. 0.005" TRACE WIDTH TO BE IMPEDANCE CONTROLLED.
    45 OHM +/-10% SINGLE ENDED, 90 OHM +/-10% DIFFERENTIAL.
    SEE STACK-UP FOR LAYER THICKNESS.
    WIDTH OF TRACES ON SIGNAL LAYERS MAY BE ADJUSTED AS NECESSARY
    TO ACHIVE IMPEDANCE SPECIFIED.