

#### **REVISION HISTORY**

REV	EDITOR	DESCRIPTION	LoLo Ver.	APPROVAL	DATE
А	James Wicks	Release to accommodate LoLo v1.4	1.4	MAA	07/20/04
В	Aaron Stewart	Added supported options table	1.4	ME	12/3/04
С	Mike Aanenson	-Updated for LogicLoader 2.0.x -Updated Diagrams -Updated Supported Hardware Table	2.0	MAA	10/13/05

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## 1 SH7760-10 Memory Map Diagrams

#### 1.1 SH7760-10 Hardware Memory Map

The SH7760 processor has the ability to address the memory map as cached or uncached, depending on the value of the top nibble of the address. The Renesas SH7760 Manual should be consulted for full documentation of this feature.

#### 1.2 Physical Hardware Memory Map

SH7760-10 Logical Memory Map during execution of LogicLoader

0xFFFFFFF .	Uncached	Cached	
0xFC000000	Bus Control / Internal Peripheral Memory-Mapped Registers		NA
0x20000000	RESERVED	NA	NA
0x1C000000	RESERVED	NA	NA
0x18000000	AREA 6: PC Card/Compact Flash Primary Slot - NOT USED	Х	
0x14000000	AREA 5: PC Card/Compact Flash Secondary Slot - NOT USED 000000		
0x10000000	AREA 4: EXTERNAL I/O (FAST Area)	Х	
0x0C000000	AREA 3: SDRAM		Х
0x08000000	AREA 2: External CS2 - NOT USED		
0x04000000	AREA 1: EXTERNAL I/O (SLOW Area)	X	
0x00000000	AREA 0: FLASH MEMORY (mapped area depends on FLASH size)	WRITE	READ

Note:

Cached Addresses: 0x80000000 Uncached Addresses: 0xA0000000

Figure 1.1: SH7760-10 Hardware Memory Map

#### 1.3 LogicLoader and the Configuration Block in Flash Memory

LogicLoader is programmed into the card engine's resident flash array. The optional Configuration Block may be added with the 'config CREATE' command.

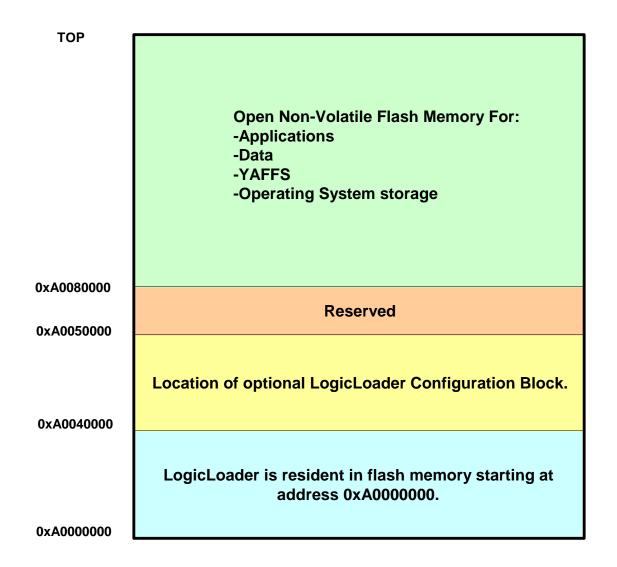


Figure 1.2: Flash Memory Layout

#### 1.4 LogicLoader's Location in RAM

LogicLoader executes out of RAM. The diagram below depicts run time location of LogicLoader.

Run-time location of LogicLoader:

At reset, LogicLoader relocates itself from flash memory to system SDRAM. LogicLoader then spends the remainder of its run-time executing out of system SDRAM. Note: the size of LogicLoader's code and variable sections are Free RAM estimates. This size depends on the exact features built into the LogicLoader image and may change with new releases. The location of LogicLoader's stack is dynamically determined at run-0x8C0C0000 time based on the size of the code and variable section. Therefore, the location of the stack is provided as an estimate in Heap and stack for use by LogicLoader this diagram. 0xA0040000 LogicLoader variable section Flash block zero LogicLoader code section 0xA0000000 0x8C000000 Flash memory System SDRAM

Figure 1.3: LogicLoader RAM Execution Environment

# 2 SH7760-10 LogicLoader Functionality

#### 2.1 Supported Hardware Peripherals

The table below lists SH7760-10-specific peripherals supported by LogicLoader.

Hardware Peripheral	Support (Y/N)	Details
Audio	N	
Display:	Y	LogicLoader supports 8 and 16 bits per pixel; custom displays can be supported by using the config block.
LCD-3.5-QVGA-10	N	Display kit with LCD part number LQ035Q7DB02
LCD-3.5-QVGA-20	Υ	Display kit with LCD part number LQ035Q7DB02 w/ASIC
LCD-5.7-QVGA-10	Υ	Display kit with LCD part number LQ057Q3DC02
LCD-6.4-VGA-10	Υ	Display kit with LCD part number LQ64D343
LCD-10.4-VGA-10	Υ	Display kit with LCD part number LQ10D368
LCD-12.1-SVGA-10	N	Display kit with LCD part number LQ121S1DG41
		10/100MBit support; MAC address stored in dedicated serial EEPROM; static IP address can be supported by using the
Ethernet	Υ	config block.
Flash Memory	Υ	NOR flash only
IrDA	N	<u></u>
Memory / IO Card		Compact Flash memory cards are only supported.
Expansion:	Υ	16 -> 256MB Compact Flash memory cards have been verified.
IO Mode PCMCIA/ CF	N	
Memory Mode CF	Υ	Recommended: SanDisk, Toshiba, PNY
MMC	N	
SmartCard	N	
Processor:		
Cache	Υ	
Clock	Υ	198 MHz CPU / 66MHz Bus
Power Management	N	
MMU	Υ	
I2C	N	
SDRAM	Υ	64 Mbytes
SPI	N	
Serial Port:		
		115200 baud standard, RTS flow only; 4800 to 460800 baud
UARTA	Υ	can be supported by using the config block
UARTB	N	
UARTC	N	
Touch Screen	N	
USB Host	N	
CAN	N	
Misc:		
GPIO	Y	Use 'w' and 'x' commands to access data direction and data registers to control GPIO lines per register description in processor and IO Controller specification documents.
Status	N	
Mode Line 2	Y	QuickBoot Feature details: LogicLoader will typically pause 500 mS to look for the 'q' key on UARTA. However, if the Mode Line 2 (uP_MODE2) is grounded, this 500 mS timeout is skipped and the boot script runs immediately.
Serial EEPROM	Υ	128 bytes
3011G1 EE1 110111		·== ~j·==

<sup>\*</sup>Note: If a peripheral is not mentioned on this list, is should be assumed there is no native support for it in LogicLoader besides the ability to read and write from registers.

### 3 Disclaimer

Logic strives to provide the most up to date information. However, the list of supported features in this document is partial and subject to change.

The "Supported Hardware Peripherals" list was created to describe the supported features for fully populated standard card engine builds. If the card engine in use is a custom build or has some hardware feature omitted, the commands related to those hardware features may not function.

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