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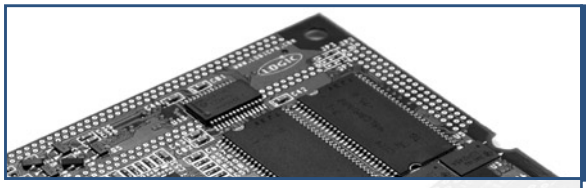

Zoom™

Card Engine

SH7760-10 Card Engine
IO Controller Specification

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CPLD REV	APPROVAL	DATE
1	Colette O'Brien	Document Created		C.O.	06/18/03
2	Hans Rempel James Wicks	Editing, Formatting, Technical Review		J.A.W.	10/13/03
3	James Wicks	GPIO Direction Register Edit		Ryan Hoium	11/05/03
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A	James Wicks	Pilot Release: Removed Preliminary References	1.B	HAR	10/22/04

Please check http://ww.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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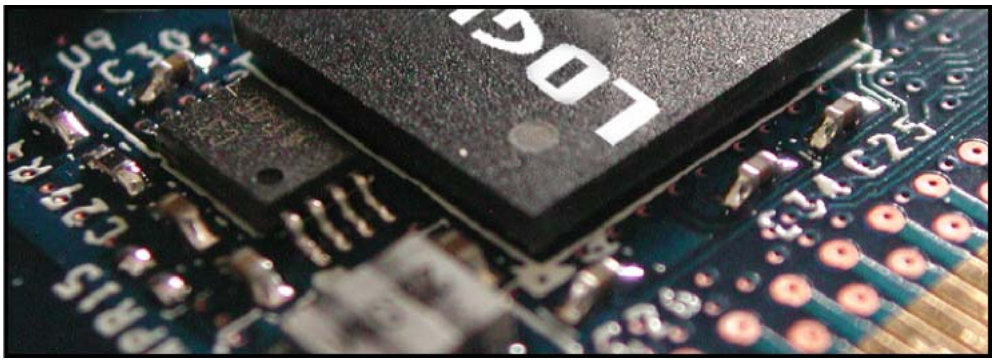
1 Introduction

1.1 Product Brief

Logic offers production-ready I/O controller devices and design packages for customers creating custom card engine designs and CPLD code for the SH7760 Card Engine. Logic has optimized the VHDL code to fit in the smallest possible programmable logic device. This results in an embedded product development cycle with **less time, less cost, less risk ... more innovation.**



- **The I/O Controller was written in VHDL and contains the following:**
  - SPI (parallel to SPI interface)
  - ISA-like bus interface
  - SMSC LAN91C111 wired LAN bus interface and power control logic
  - Buffer control logic
  - Chip select decoder logic
  - Interrupt encoder logic
  - Flash program control logic
  - Processor mode control logic
  - IC code revision register
  - PCMCIA control line interface
- **I/O Controller Device**
  - 100-pin FBGA package (Logic Part No. 31300181-P01-0110)
- **Source Code**
  - Includes all VHDL code (licensable .vhd source code files)
- **Support**
  - VHDL IP Core Source Code Design Package includes the Bronze level support package

1.2 Acronyms

BALE	Buffered Address Latch Enable
CF	CompactFlash
CS	Chip Select
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Electrically Programmable Read Only Memory
GPIO	General Purpose Input Output
IO	Input Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LAN	Local Area Network
LED	Light Emitting Diode
MB	Megabyte (2^20 bytes)
SPI	Serial Peripheral Interface

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Altera MAX 7000A PLD data sheet (EPM7128AFC100-10)
- Altera Device Package Information data sheet
- Altera Ordering Information
- Texas Instruments (Burr-Brown) ADS7843 data sheet

1.4 IO Controller Advantages

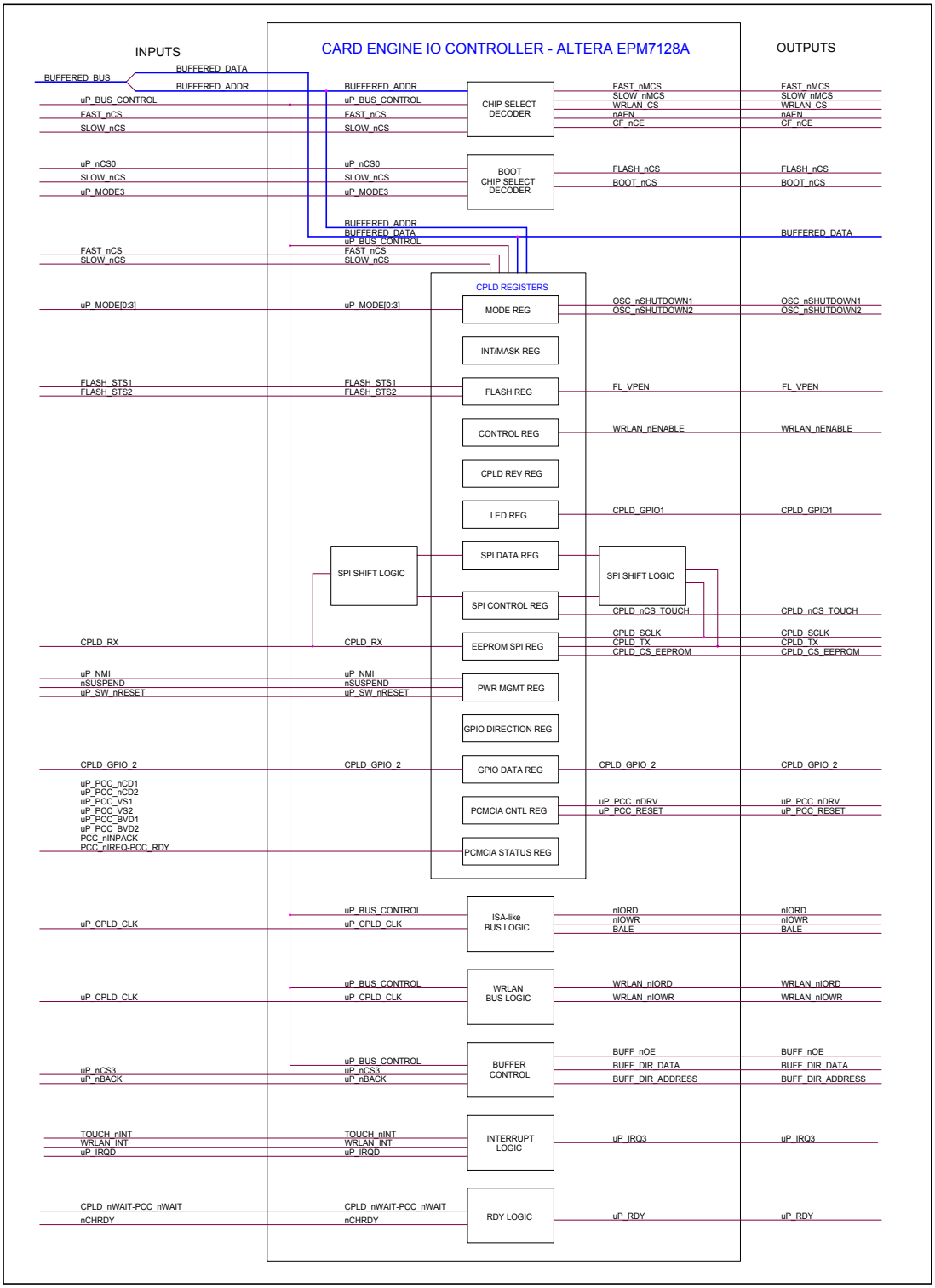
Some of the key features in the IO Controller include:

- Multiple Parallel to SPI Interface
- Chip Select Encoder
- Interrupt Decoder
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player
- PCMCIA control-line interface

The IO Controller VHDL source code is available for purchase. Contact Logic for more information.

1.5 IO Controller Block Diagram

Figure 2.1: IO Controller Block Diagram



2 IO Controller Address and Register Definitions

Address Range*	Memory Block Description	Size
0x1000 0000 – 0x13FF FFFF	Fast Peripherals Chip Select (Area 4)	64MB
0x0400 0000 – 0x07FF FFFF	Slow Peripherals Chip Select (Area 1)	64MB

***Note:** addresses used in the IO controller spec are absolute addresses and actual software access addresses may be different depending on the state of the CPU's MMU and the desired access area.

2.1 Fast Peripherals Chip Select (Area 4)

Address Range*	Memory Block Description	Size
0x1000 0000 – 0x101F FFFF	Wired LAN Chip Select	2MB
0x1020 0000 – 0x103F FFFF	Card Engine Control Reg	2MB
0x1040 0000 – 0x105F FFFF	Reserved	2MB
0x1060 0000 – 0x107F FFFF	SPI Data Reg	2MB
0x1080 0000 – 0x109F FFFF	SPI Control Reg	2MB
0x10A0 0000 – 0x10BF FFFF	EEPROM SPI Reg	2MB
0x10C0 0000 – 0x10DF FFFF	Interrupt/Mask Reg	2MB
0x10E0 0000 – 0x10FF FFFF	Mode Reg	2MB
0x1100 0000 – 0x111F FFFF	Flash Reg	2MB
0x1120 0000 – 0x113F FFFF	Power Management Reg	2MB
0x1140 0000 – 0x115F FFFF	IO Controller Code Revision Reg	2MB
0x1160 0000 – 0x117F FFFF	Extended GPIO Data Reg	2MB
0x1180 0000 – 0x119F FFFF	GPIO Data Reg	2MB
0x11A0 0000 – 0x11BF FFFF	GPIO Direction Reg	2MB
0x11C0 0000 – 0x11DF FFFF	PCMCIA Status Reg	2MB
0x11E0 0000 – 0x11FF FFFF	PCMCIA Control Reg	2MB
0x1200 0000 – 0x12FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x1300 0000 – 0x13FF FFFF	Open – Available for User	1MB (X16)

Each memory block for area 4 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

2.1.1 Wired LAN Chip Select

Address Range: 0x1000 0000 – 0x101F FFFF

- This area of memory is used when accessing the wired LAN chip (internal registers/memory).

2.1.2 Card Engine Control Register

Address Range: 0x1020 0000

- This register holds control bits for the card engine.

7	6	5	4	3	2	1	0	
SWINT	-	-	-	-	-	-	WLPEn	
1	-	-	-	-	-	-	0	reset
R/W	-	-	-	-	-	-	R/W	R/W

SWINT: Software settable interrupt source.
0 = Generate an interrupt on uP_IRQ3
1 = Do not generate an interrupt on uP_IRQ3

WLPEn: wired LAN power enable signal. This bit enables/disables power to the on-board wired LAN chip.
0 = Wired LAN enabled
1 = Wired LAN disabled

2.1.3 Reserved

Address Range: 0x1040 0000 – 0x105F FFFF

- This memory block is reserved.

2.1.4 SPI Data Register

Address Range: 0x1060 0000 – 0x107F FFFF

- This register holds the SPI data for transmit or receive. This SPI register is used in the interface to the touch chip. See Section 3.3 for a detailed description of the SPI interface and how to use it.

7	6	5	4	3	2	1	0	
8-bit SPI data								
0	0	0	0	0	0	0	0	reset
R/W								R/W

2.1.5 SPI Control Register

Address Range: 0x1080 0000

- This register controls transmission and reception of SPI data, to/from the 8-bit SPI data register (section 2.1.4).

7	6	5	4	3	2	1	0	
-	-	SPLD	SPST	SPDN	SPRW	STCS	SCCS	
		0	0	0	0	0	0	reset
-	-	R	R/W	R	R/W	R/W	R/W	R/W

SPLD: SPI load.
0 = SPI data register has not been loaded and shift count has not been reset
1 = SPI data register has been loaded and shift count has been reset

SPST: SPI start.
0 = transfer loaded data
1 = load SPI data register and reset shift count

SPDN: SPI done.
0 = SPI transfer pending not done
1 = SPI transfer done

SPRW: SPI read/write.
0 = execute SPI write cycle
1 = execute SPI read cycle

STCS: SPI touch chip select.
0 = not selected
1 = touch chip selected

SCCS: SPI CODEC chip select (not used).
0 = not selected
1 = CODEC chip selected

2.1.6 EEPROM SPI Interface Register

Address Range: 0x10A0 0000

- This register holds SPI data during a read/write between the processor and on-board EEPROM. The SPI interface used for the EEPROM is implemented by the processor (the timing and bit shifting is performed manually by the processor), not the IO Controller (as in the case of the touch chip).

7	6	5	4	3	2	1	0	
-	-	-	-	EECS	EECK	EETX	EERX	
-	-	-	-	0	0	0	0	reset
-	-	-	-	R/W	R/W	R/W	R	R/W

EECS: EEPROM chip select.
0 = not selected
1 = EEPROM chip selected

EECK: EEPROM SPI clock.

EETX: EEPROM SPI data transmit.

EERX: EEPROM SPI data receive.

2.1.7 Interrupt/Mask Register

Address Range: 0x10C0 0000

- This register contains the information used by the IO Controller to generate an interrupt to the processor on signal uP_IRQ3.

7	6	5	4	3	2	1	0	
DMSK	IRQD	-	RSVD	TMSK	WMSK	TIRQ	WIRQ	
0	-	-	1	0	0	1	1	reset
R/W	R	-	-	R/W	R/W	R	R	R/W

DMSK: application board signal uP_IRQD interrupt mask*.
0 = interrupt not masked
1 = interrupt masked

IRQD: state of uP_IRQD interrupt request (IRQ).
0 = interrupt is active
1 = interrupt is not active

TMSK: touch chip interrupt mask*.
0 = interrupt not masked
1 = interrupt masked

WMSK: wired LAN chip interrupt mask*.
0 = interrupt not masked
1 = interrupt masked

TIRQ: state of touch chip interrupt request (IRQ).
0 = interrupt is active
1 = interrupt is not active

WIRQ: wired LAN chip interrupt request (IRQ).
0 = interrupt is active
1 = interrupt is not active

*When the interrupt is masked, the interrupt will not be generated, but the interrupt status will still be reflected in the corresponding IRQ bit.

2.1.8 Mode Register

Address Range: 0x10E0 0000

- This register holds the values of the mode pins.

7	6	5	4	3	2	1	0	
-	-	OSD2	OSD1	MDP3	MDP2	MDP1	MDP0	
-	-	1	1	-	-	-	-	reset
-	-	R/W	R/W	R	R	R	R	R/W

OSD2: Oscillator 2 shutdown pin control.
0 = OSC_nSHUTDOWN2 pin is low (tristates 48MHz USB clock signal)
1 = OSC_nSHUTDOWN2 pin is high (enables 48MHz USB clock signal)

OSD1: Oscillator 1 shutdown pin control.
0 = OSC_nSHUTDOWN1 pin is low (tristates 40MHz LCD clock signal)
1 = OSC_nSHUTDOWN1 pin is high (enables 40MHz LCD clock signal)

MDP3: mode pin 3. Mode pin 3 selects between on-board and off-board boot device. See Section 3.2 for detailed information on mode pin 3.
0 = off-board boot device
1 = on-board boot device (32 bit NOR flash)

MDP2: mode pin 2. Mode pin 2 represents the endian setting for the processor.
0 = big endian
1 = little endian

MDP1, MDP0: mode pin 1 and mode pin2. These mode pins represent the bus width at boot. Bit MDP0 controls processor mode pin MD3 and bit MDP1 controls processor mode pin MD4. (Note: See SH7760 datasheet for specific setting options for processor mode pins.)

2.1.9 Flash Register

Address Range: 0x1100 0000

- This register holds status information for the on-board NOR flash chips.

7	6	5	4	3	2	1	0	
-	-	-	-	FPOP	FST2	FST1	FPEN	
-	-	-	-	1	-	-	0	reset
-	-	-	-	R/W	R	R	R/W	R/W

FPOP: flash populated bit.
0 = flash populated
1 = flash not populated

Note: This bit is used internal to the CPLD when generating the flash chip select, ISA chip select, and CompactFlash chip select. If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of ISA and CompactFlash

(area 1 will be occupied by flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low. If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is high, the ISA and CompactFlash chip selects will be available to the user. When the card engine flash is selected for boot (signal MODE 3 is high), bit (3) of the flash register is ignored, and the off-board EPROM is available to the user at address range 0x0400 0000 – 0x041F FFFF. See section 2.2.1

FST2: Flash status pin. This is the RY/BY# pin for the upper 16 bit flash chip.
0 = flash busy
1 = flash ready

FST1: Flash status pin. This is the RY/BY# pin for the lower 16 bit flash chip.
0 = flash busy
1 = flash ready

FPEN: Flash program enable.
0 = normal flash operations
1 = program flash enabled

2.1.10 Power Management Register

Address: 0x1120 0000

- This register holds the value of the power management input signals to the CPLD.

7	6	5	4	3	2	1	0	
-	-	-	nSTANDBY	-	nSUSPEND	uP_SW_nRESET	-	
-	-	-	-	-	-	-	-	reset
-	-	-	R	-	R	R	-	R/W

nSTANDBY: value of the nSTANDBY input signal to the CPLD. The nSTANDBY signal has a pull-up resistor on the card engine.
0 = nSTANDBY signal is low
1 = nSTANDBY signal is high

nSUSPEND: value of the nSUSPEND input signal to the CPLD. The nSUSPEND signal has a pull-up resistor on the card engine.
0 = nSUSPEND signal is low
1 = nSUSPEND signal is high

uP_SW_nRESET: value of the uP_SW_nRESET input signal to the CPLD. The uP_SW_nRESET signal has a pull-up resistor on the card engine.
0 = uP_SW_nRESET signal is low
1 = uP_SW_nRESET signal is high

2.1.11 IO Controller Code Revision Register

Address Range: 0x1140 0000

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								reset
R								R/W

2.1.12 Extended GPIO Data Register

Address Range: 0x1160 0000

- This register controls application board LED's.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	CPLD_GPIO_1	
-	-	-	-	-	-	-	1	reset
-	-	-	-	-	-	-	R/W	R/W

CPLD_GPIO_1: General purpose output-only bit.
0 = Set pin low
1 = Set pin high

2.1.13 GPIO Data Register

Address: 0x1180 0000

- This register holds data for the CPLD general purpose input/output pins. Note: The direction (input or output) of the CPLD pins are set in the GPIO Direction Register in section 2.1.14.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	CPLD_GPIO_2	
-	-	-	-	-	-	-	0	reset
-	-	-	-	-	-	-	R/W	R/W

CPLD_GPIO_2: General purpose input/output bit.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

2.1.14 GPIO Direction Register

Address: 0x11A0 0000

- This register controls the direction for the CPLD general purpose input/output pins. Note: The value (high or low) of the CPLD pins are read/written in the GPIO Data Register in section 2.1.13.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	GPDIR0	
-	-	-	-	-	-	-	1	reset
-	-	-	-	-	-	-	R/W	R/W

GPDIR0: CPLD GPIO direction control bit for CPLD_GPIO_2
0 = external CPLD signal CPLD_GPIO_2 is an output
1 = external CPLD signal CPLD_GPIO_2 is an input

2.1.15 PCMCIA Status Register

Address: 0x11C0 0000

- This register represents the state of the PCMCIA status signals for an external PCMCIA/CF slot. If a dual slot interface is being used, an external control must be implemented to select the slot that is driving the inputs to these status bits.

7	6	5	4	
-	PCC_nIREQ_RDY	uP_PCC_BVD2	uP_PCC_BVD1	
-	-	-	-	reset
-	R	R	R	R/W

3	2	1	0	
uP_PCC_VS2	uP_PCC_VS1	uP_PCC_nCD2	uP_PCC_nCD1	
-	-	-	-	reset
R	R	R	R	R/W

PCC_nIREQ_RDY: This is the “PCC_nIREQ – PCC_RDY” PCMCIA/CF slot status bit. This bit also generates an interrupt depending on the state of the interrupt control bits in the PCMCIA Control Register (section 2.1.16).
0 = PCC_nIREQ – PCC_RDY pin is low
1 = PCC_nIREQ – PCC_RDY pin is high

uP_PCC_BVD2: This is the “uP_PCC_BVD2” PCMCIA/CF slot status bit.
0 = uP_PCC_BVD2 pin is low
1 = uP_PCC_BVD2 pin is high

uP_PCC_BVD1: This is the “uP_PCC_BVD1” PCMCIA/CF slot status bit.
0 = uP_PCC_BVD1 pin is low
1 = uP_PCC_BVD1 pin is high

uP_PCC_VS2: This is the “uP_PCC_VS2” PCMCIA/CF slot status bit.
0 = uP_PCC_VS2 pin is low
1 = uP_PCC_VS2 pin is high

uP_PCC_VS1: This is the “uP_PCC_VS1” PCMCIA/CF slot status bit.
0 = uP_PCC_VS1 pin is low
1 = uP_PCC_VS1 pin is high

uP_PCC_nCD2: This is the “uP_PCC_nCD2” PCMCIA/CF slot status bit.
0 = uP_PCC_nCD2 pin is low
1 = uP_PCC_nCD2 pin is high

uP_PCC_nCD1: This is the “uP_PCC_nCD1” PCMCIA/CF slot status bit.
0 = uP_PCC_nCD1 pin is low
1 = uP_PCC_nCD1 pin is high

2.1.16 PCMCIA Control Register

Address: 0x11E0 0000

- This register controls output pins and RDY/nIREQ interrupt behavior for either a single slot PCMCIA/CF interface or “Slot B” of a dual slot PCMCIA/CF interface.

7	6	5	4	
-	-	IREQ_nINT	IO_MODE	
-	-	1	0	reset
-	-	R	R/W	R/W

3	2	1	0	
IREQ_RDY_MSK	IREQ_RDY_LVL	uP_PCC_nDRV	uP_PCC_RESET	
1	0	1	1	reset
R/W	R/W	R/W	R/W	R/W

IREQ_nINT: This bit reflects the state of the IREQ interrupt latch and can be read by software to determine the cause of an interrupt. This bit always reads “1” when the IO_MODE bit is “0” (slot is not in IO_MODE).
0 = IREQ_nINT has occurred and an interrupt is being generated
1 = IREQ_nINT has not occurred or slot is not in I/O mode

IO_MODE: Controls behavior of PCC_nIREQ – PCC_RDY interrupt generation. If set to IO mode (value of 1), the interrupt will be latched from a falling-edge on the PCC_nIREQ – PCC_RDY signal. If not set to IO mode, the interrupt will be controlled by the IREQ_RDY_LVL bit and will not be latched. Note that setting this bit to “0” will clear the latched state of the interrupt and thereby set the IREQ_nINT bit to a “1”.
0 = Memory mode (RDY selectable level interrupts)
1 = IO mode (IREQ pulse falling edge latched interrupts)

IREQ_RDY_MSK: External PCMCIA/CF single slot (or dual configuration “Slot B”) PCC_nIREQ – PCC_RDY interrupt mask
0 = interrupt not masked

1 = interrupt masked

IREQ_RDY_LVL: External PCMCIA/CF single slot (or dual configuration “Slot B”) PCC_nIREQ – PCC_RDY interrupt level selection. Note that this bit has no affect if the IO_MODE bit is a 1.
0 = interrupt is generated on low level of PCC_nIREQ – PCC_RDY signal
1 = interrupt is generated on high level of PCC_nIREQ – PCC_RDY signal

uP_PCC_nDRV: External PCMCIA/CF single slot (or dual slot “B”) slot enable signal (used to control buffer enables and power to the slot)
0 = external power and buffers enabled
1 = external power and buffers disabled

uP_PCC_RESET: External PCMCIA/CF single slot (or dual slot “B”) reset signal
0 = PCMCIA/CF card is in operational state
1 = PCMCIA/CF card is in reset

2.1.17 Reserved On-Board Memory Blocks

None.

2.1.18 Reserved Off-Board Memory Blocks

Address Range: 0x1200 0000 – 0x12FF FFFF

- These sixteen memory blocks are reserved for off-board IO controller expansion.

2.1.19 Open Memory Blocks – Available for User

Address Range: 0x1300 0000 – 0x13FF FFFF

These sixteen memory blocks are open and available for the user to utilize.

2.2 Slow Peripherals Chip Select (Area 1)

Address Range	Memory Block Description	Size
0x0400 0000 – 0x041F FFFF	(Boot) EPROM Chip Select	2MB
0x0420 0000 – 0x043F FFFF	CF Chip Select	2MB
0x0440 0000 – 0x045F FFFF	ISA-like Bus Chip Select	2MB
0x0460 0000 – 0x05FF FFFF	Reserved - On-Board Expansion	2MB (X13)
0x0600 0000 – 0x06FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x0700 0000 – 0x07FF FFFF	Open – Available for User	1MB (X16)

Each memory block for area 1 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

2.2.1 (Boot) EPROM Chip Select

Address Range: 0x0400 0000 – 0x041F FFFF

- Use this area to access off-board EPROM, when flash is selected for area 0.

Note: If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of ISA and CompactFlash (area 1 will be occupied by flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low. If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3)

of the flash register is high, the ISA and CompactFlash chip selects will be available to the user. When the card engine flash is selected for boot (signal MODE 3 is high), bit (3) of the flash register is ignored, and the off-board EPROM is available to the user at address range 0x0400 0000 – 0x041F FFFF. (ISA and CompactFlash are also available.)

2.2.2 CompactFlash (CF) Chip Select

Address Range: 0x0420 0000 – 0x043F FFFF

- This area of memory is used when accessing the off-board memory mapped CompactFlash Type 1 Memory Only slot.

Note: If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of ISA and CompactFlash (area 1 will be occupied by flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low.

2.2.3 ISA-like Bus Chip Select

Address Range: 0x0440 0000 – 0x045F FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 4 for read and write timing diagrams.

Note: If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the Flash register is low, the user will lose the option of ISA and CompactFlash (area 1 will be occupied by Flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low.

2.2.4 Reserved On-Board Memory Blocks

Address Range: 0x0460 0000 – 0x05FF FFFF

- These memory blocks are reserved for future on-board expansion.

2.2.5 Reserved Off-Board Memory Blocks

Address Range: 0x0600 0000 – 0x06FF FFFF

- These memory blocks are reserved for off-board IO controller expansion.

2.2.6 Open Memory Blocks – Available for User

Address Range: 0x0700 0000 – 0x07FF FFFF

- These memory blocks are open and available for the user to utilize.

3 IO Controller Functions

This section describes in detail the different IO Controller function blocks. See Section 1.5 for the IO Controller block diagram.

3.1 Chip Select Decoder Logic

This logic decodes processor chip selects 1 and 4 into smaller segments of memory. See Section 2.1 for the Fast Peripherals Chip Select (Area 4), and Section 2.2 for the Slow Peripherals Chip Select (Area 1).

CPLD signal FAST_nMCS is output when FAST_nCS (area 4) is low and uP_MA25 is high. CPLD signal SLOW_nMCS is output when SLOW_nCS (area 1) is low and uP_MA25 is high. Signals FAST_nMCS and SLOW_nMCS are brought off the card engine through the expansion bus connectors.

Note: If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of chip select signal SLOW_nMCS (area 1 will be occupied by flash). This means SLOW_nMCS will not be allowed to go low.

3.2 Boot Chip Select Decoder Logic

Note: Mode pin 3 selects between on-board and off-board boot device.

The card engine can boot from the 32-bit on-board NOR flash device or an 8, 16, or 32-bit off-board memory device. The boot device is determined by a mode line setting (mode pin 3) on the application board. The boot device is always located in area 0 (CS0). When mode pin 3 is high, the on-board flash is selected for boot, and when mode pin 3 is low, the off-board memory device is selected for boot. This logic is presented the following table.

Note: If the off-board EPROM is selected for boot (MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of ISA and CompactFlash (area 1 will be occupied by flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low. If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is high, the ISA and CompactFlash chip selects will be available to the user. When the card engine flash is selected for boot (MODE 3 is high), bit (3) of the flash register is ignored, and the off-board EPROM is available to the user at address range 0x0400 0000 – 0x041F FFFF (area 1). (ISA and CompactFlash are also available.)

Flash (on-board)	Off-board memory	Mode Pin 3	Flash Reg (3)	Function
CS0 (area 0)	CS1 (area 1)	1	ignored	boot from flash in area 0, off-board memory device is in area 1
CS1 (area 1)	CS0 (area 0)	0	0	boot from off-board memory device in area 0, flash is in area 1
CS1 (area 1)	CS0 (area 0)	0	1	boot from off-board memory device in area 0, (flash not populated) area 1 is open

The chip selects for area 0 and 1 are routed externally to the flash and off-board memory device by signals FLASH_nCS and BOOT_nCS.

3.3 SPI Interface

3.3.1 Usage notes

The SPI interface usage flow is as follows:

SPI Read Cycle:
1) set SPST and SPRW to 1
2) poll SPLD bit until it equals 1
3) clear SPST bit to 0
4) poll SPDN bit until it equals 1
5) read the SPI data register for received data
6) repeat…

SPI Write Cycle:
1) write 8 bit data to SPI data register
2) set SPST to 1
3) poll SPLD bit until it equals 1
4) clear SPST to 0
5) poll SPDN bit until it equals 1
6) repeat…

3.3.2 Touch SPI Interface

See Texas Instruments (Burr-Brown) ADS7843 data sheet for the complete command set and registers. See sections 2.1.4 and 2.1.5 for SPI Data and SPI Control Register bit definitions.

3.4 ISA-like Bus Logic (CompactFlash and ISA peripherals in area 1)

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic outputs the ISA chip select, CompactFlash chip select, BALE, read (nIORD), and write (nIOWR) signals. It also creates two timing delays in the ISA-like bus timing: first, the delay between the falling edge of the chip select (CompactFlash or ISA) and falling edge of read (nIORD) or write (nIOWR) signal, and second, the delay between the rising edge of the read or write signal and rising edge of the chip select.

The first delay is created by shifting the falling edge of the read (nIORD) or write (nIOWR) signal to create a delay from the chip select. The rising edge of the read and write signals follow the rising edge of the processor read and write signals. See Section 4 for sample read and write ISA-like timing diagrams.

The ISA device chip select is output by the CPLD when an access to address range 0x0440 0000 – 0x045F FFFF is made, and the CompactFlash chip select is output when an access to address range 0x0420 0000 – 0x043F FFFF is made.

The ISA-like bus timing, in Section 4, is shown with the minimum number of internal wait states programmed for the processor to meet CompactFlash timing. The user can change the programmed wait state value by modifying the processor's Wait Control Register 2 (WCR2), for area 1.

The nCHRDY input signal to the CPLD is shown in the ISA-like bus timing diagrams. It can be asserted by CompactFlash or an ISA device. When pulled low, the nCHRDY signal generates a high on the uP_RDY signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. The nCHRDY low pulse width for CompactFlash is a maximum of 350ns; an example of this signal is shown in the timing diagrams. Not all CompactFlash cards or ISA devices will assert the nCHRDY signal. Therefore, the other signals in the read and write timing diagrams are shown assuming the nCHRDY signal is not pulled low.

Note: If the off-board EPROM is selected for boot (signal MODE 3 is low) and bit (3) of the flash register is low, the user will lose the option of ISA and CompactFlash (area 1 will be occupied by flash). This means the ISA and CompactFlash chip select outputs from the CPLD will not be allowed to go low.

3.5 Wired LAN Bus Logic

This logic creates read and write output signals to the wired LAN chip by shifting the falling edge of the read and write signals from the processor, to meet the required wired LAN timing. The rising edge of the wired LAN read and write signals are not shifted.

An interrupt to the processor is generated when an interrupt from the wired LAN is seen at the CPLD.

3.6 Buffer Control Logic

This logic controls the output enable and direction of the on-board buffers.

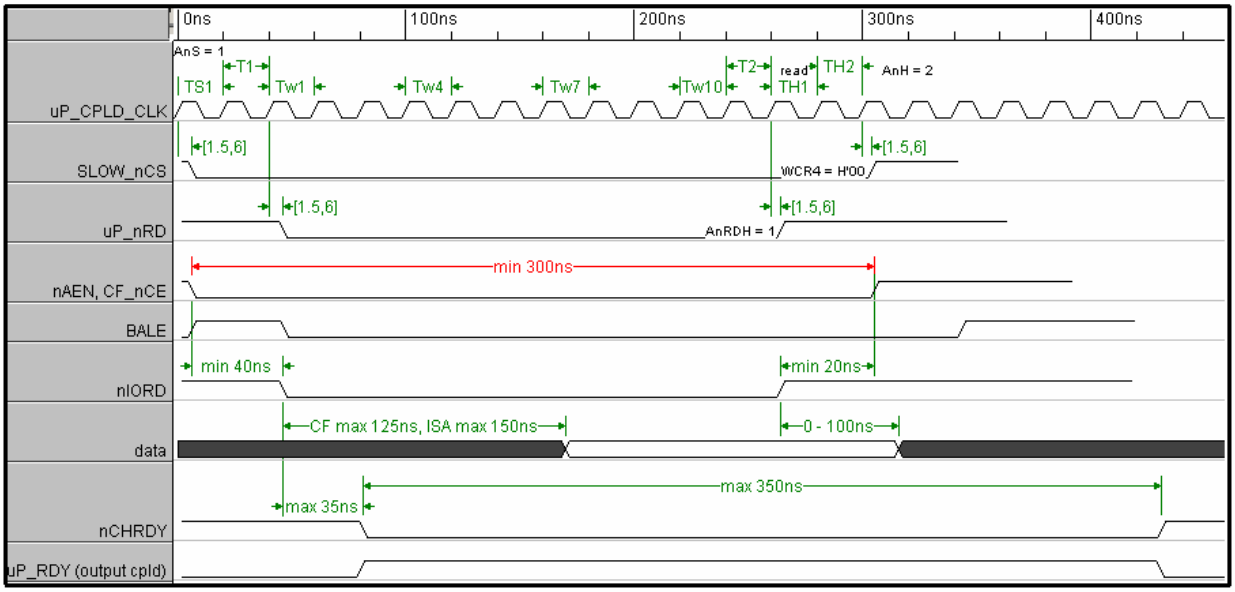
3.7 Interrupt Logic

This logic generates the processor's uP_IRQ3, from information in the Interrupt/Mask register, Section 2.1.7.

4 ISA Timing Diagrams

4.1 ISA-like Bus, Read Cycle Timing Diagram

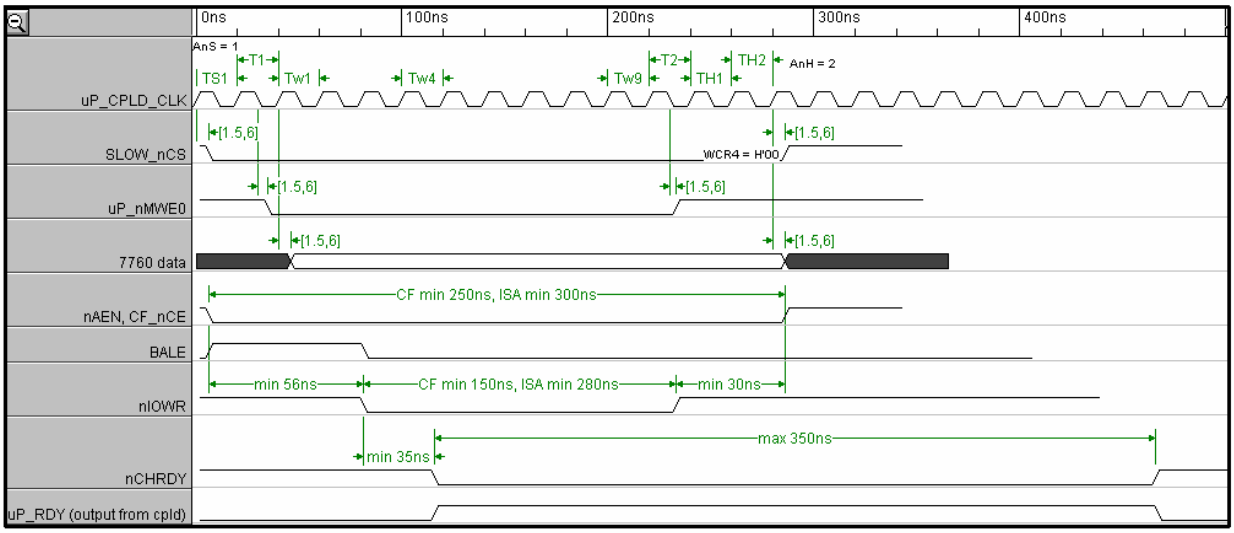
Figure 4.1: ISA-like Bus, Read Cycle Timing



Note: All timing parameters shown in nanoseconds (ns).

4.2 ISA-like Bus, Write Cycle Timing Diagram

Figure 4.2: ISA-like Bus, Write Cycle Timing



Note: All timing parameters shown in nanoseconds (ns).

5 IO Controller Pin Information

Pin	Signal Name	Input/Output
C1	uP_nCS0	Input
E7	uP_nCS3	Input
A2	SLOW_nCS	Input
B3	FAST_nCS	Input
A4	WRLAN_nCS	Output
B1	BOOT_nCS	Output
B2	FLASH_nCS	Output
K4	uP_nBACK	Input
J4	nSTANDBY	Input
F2	OSC_nSHUTDOWN1	Output
F1	OSC_nSHUTDOWN2	Output
B4	FLASH_STS1	Input
E3	FLASH_STS2	Input
C4	CPLD_nCS_TOUCH	Output
C5	CPLD_CS_EEPROM	Output
A3	uP_IRQD	Input
F4	CPLD_SCLK	Output
E2	CPLD_TX	Output
E1	CPLD_RX	Input
A5	uP_CPLD_CLK	Input

E4	UP_MA25	Input
D2	UP_MA24	Input
D1	UP_MA23	Input
D3	UP_MA22	Input
C2	UP_MA21	Input
K1	uP_MODE3	Input
J1	uP_MODE2	Input
H1	uP_MODE1 - uP_PCC_nCE2B	Input
H2	uP_MODE0 - uP_PCC_nCE2A	Input
G2	uP_nWR	Input
G1	FL_VPEN	Output
J3	uP_SW_nRESET	Input
K3	MSTR_nRST	Input
G3	WRLAN_nENABLE	Output
K5	uP_IRQ3	Output
J5	TOUCH_nINT	Input/Output
H5	WRLAN_INT	Input
E9	uP_MA2	Input
J2	PCC_nIREQ-PCC_RDY	Input
H4	nSUSPEND	Input
K6	UP_MD0	Input/Output
J6	UP_MD1	Input/Output
H6	UP_MD2	Input/Output
K7	UP_MD3	Input/Output
J7	UP_MD4	Input/Output
H7	UP_MD5	Input/Output
J8	UP_MD6	Input/Output
K8	UP_MD7	Input/Output
K2	CPLD_GPIO_1	Output
F10	CPLD_GPIO_2	Input/Output
J10	uP_PCC_nCD2	Input
H10	uP_PCC_nCD1	Input
H9	uP_PCC_VS1	Input
J9	uP_PCC_VS2	Input
G9	uP_PCC_RESET	Output
G10	uP_PCC_BVD2	Input
G8	uP_PCC_BVD1	Input
F9	uP_PCC_nDRV	Output
F7	uP_MA3	Input
D9	SLOW_nMCS	Output
D10	FAST_nMCS	Output
D8	CPLD_nWAIT-PCC_nWAIT	Input
B6	uP_nRD-nCAS	Input
A6	uP_nMWE0-DQM0-PCC_nREG	Input
C6	uP_RDY	Output
E10	uP_MA1	Input
C9	BUFF_nOE	Input/Output

C10	BUFF_DIR_ADDRESS	Input/Output
B10	BUFF_DIR_DATA	Input/Output
B9	WRLAN_nIOWR	Output
A9	WRLAN_nIORD	Output
A8	nIOWR	Output
B8	nIORD	Output
A7	BALE	Output
B7	nCHRDY	Input
C7	nAEN	Output
B5	MSTR_nRST	Input
K9	CF_nCE	Output
E8	MFP26 - PCC_nINPACK	Input
K10	RSVD_1	Input
A1	CPLD_TDI	JTAG
F3	CPLD_TMS	JTAG
F8	CPLD_TCK	JTAG
A10	CPLD_TDO	JTAG
D5,G6	VCCINT	POWER
C8,D4,E6,F5,G7,H3	VCCIO	POWER
C3,D7,E5,F6,G4,H8	GNDIO	GND
D6,G5	GNDINT	GND

6 CPLD Revision History

CPLD revision history from the VHDL source file header.

```
-------------------------------------------------------------------------------------------------------------------
-- Copyright (c) 2002-2004 Logic Product Development
--
--    Filename: sh7760_10.vhd
--    Description: Top-Level Design for the Hitachi 7760 Card Engine CPLD
--    Project: EPS
--    Language: VHDL
--    Target Part: Altera CPLD MAX7128AFC100-10
--    File Type: Product Code
--    Engineers: Colette O'Brien (CRO) - Logic Product Development
--
--
-- Rev Code:    Y.Z
--           Y = Released version (card engines update to released version "Y.0" at release time)
--           Z = Test version w/ in the above released version
--
-- Rev Code          Date       Engineer  Notes
-------------------------------------------------------------------------------------------
-- 1.B               05/21/04   HAR       + Added sw interrupt bit to Control register
--                                         + Renamed uP_NMI to nSTANDBY and moved to bit 4 of the power management
--                                         +           register to align with LH7A400 bit positions
--                                         + Moved IRQD interrupt reg bit positions to bits 6/7 instead of 5/6 to
--                                         +           align with LH7A400 bit positions
--                                         + Add sw interrupt, suspend and standby to interrupt register
--                                         + Removed capability to write to int register bit 4 (old PIRQ bit)
-- 1.A               03/09/04   MJF, KTL + Changed data bus to latch on rising edge of nMWE0
-- 1.9               02/04/04   HAR       + Added capability to make the RDY/IREQ signal edge or level detected
-- 1.8               02/04/04   HAR       + Moved PCMCIA status and control registers to on-board address location (a25=0)
--                                         + Added mask and level select for rdy/ireq interrupt
--                                         + Removed CD line interrupt source
-- 1.7               01/02/04   KTL       + Reworked PCC RDY and CD1/2 signal interrupts, defined new registered bits.
-- 1.4               10/23/03   RMH       + Changed bidirectional GPIO to default to inputs out of reset
-- 1.3               10/23/03   HAR       + re-inserted IRQD interrupt and mask bits for IRQ3 creation
--                                         + will not work on revA or earlier boards!!!!!
-- 1.2               10/23/03   HAR       + made changes for interrupts on revA boards and SPI data reg
-- 1.1               08/01/03   CRO       + made changes for 66.6mhz uP_CPLD_CLK
--                                         + current spi clk (CPLD_SCLK) = 2.08mhz, and not required < 2mhz, due to routing issues
-- 1.0               06/11/03   CRO       + initial rev of code with updates for revA hardware
--                                         + added PCMCIA interrupts and registers (slow area)
--                                         + removed sw_reset and suspend interrupts, added uP_IRQD interrupt
--                                         + added uP_nBACK, OSC_SHUTDOWN, and uP_IRQD signals to code
--                                         + added initial conditions for OSC_SHUTDOWN signals
--                                         + changed initial condition for OSC_SHUTDOWN signals to '1' (normal output, not tristated)
-- 0.1               06/10/03   CRO       + test code for spi data and control registers
-- 0.0               03/25/03   CRO       + inital rev of document for Rev 1 card engines
```

