SH7760-10
Card Engine

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REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CARD ENGINE REV	APPROVAL	DATE
1	Charles Eddleston	First Draft Version	-	CJE	8/4/03
2	James Wicks	Added mode line description note	-	JW	9/19/03
3	Kurt Larson, Hans Rempel, Erik Reynolds, James Wicks	Preliminary Release	-	HR,ER	10/09/03 10/22/03
4	James Wicks, Kurt Larson, Michael Anderson	Figure 2.2 Correction, Preliminary Release 2, USB Signal description update	C	JW	6/21/04
A	Hans Rempel	Pilot Release; Corrected Section 5.4.2 LCD signals; Added note re: wait signal usage with LCDC; Fixed pin out descriptions on J1B signals;	C	HAR	10/22/04
B	James Wicks	Pin Corrections: - JIA pin 68 uP_USB2_PWR_EN - JIB pin 45 up_UARTB_RTS JIC multiplex table, Section 5.4.1: - uP_nMRD - PCC_nOE now labeled pin 84 JIA multiplex table, Section 5.4.2: - Pin 3 LCD_CLKOUT corrected to LCD_DCLK - Removed Pins 67 and 69 - Added Pin 65 - Added Pin 68 JIB multiplex table, Section 5.4.3: - Pin 45 uP_UARTB_DSR corrected to uP_UARTB_RTS - Pin 60 MFP20 - CAN0_RX corrected to MFP20 - uP_NMCS5 - PCC_nMCE1A - Added pin 39 - Added pin 68	C	MAA	3/14/05
C	Jed Anderson	Updated Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes; Updated Intel web address is Section 2.8	-	JCA	11/08/06

Please check http://www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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SH7760 CARD ENGINE

CARD ENGINE ADVANTAGE

- Reduce TIme to Market
  → 6 to 9 month savings
- Product-Ready Hardware Platform
- Production Quality Software
- Engineering Support

PRODUCT HIGHLIGHTS

- Ready-to-Run Windows® CE BSP
- Bootloader/Monitor
- Custom Windows CE device driver development

ORDERING INFORMATION

- Zoom™ Starter Development Kit (Model # SDK-SH7760-10-6416)

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

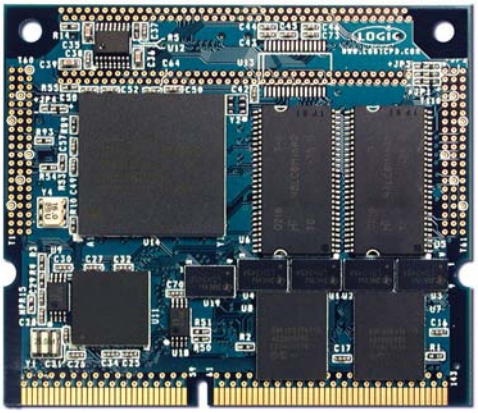
For more information on our Embedded Product Solutions, please contact Logic Sales at product.sales@logicpd.com or 612.672.9495.

RENESAS

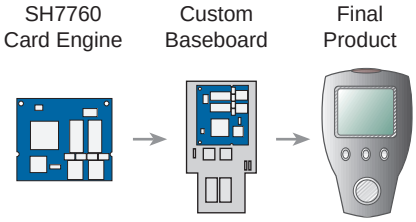
Microsoft® Windows® Embedded Partner
Gold-level Member

The SH7760 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The SH7760 Card Engine is a complete System on Module (SOM) offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. The use of custom baseboards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation microcontroller Card Engines when new funtionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Renesas SH7760 32-bit SH-4 RISC microprocessor running at 198 MHz
- **SDRAM Memory** Up to 64 Mbytes
- **Flash Memory** Up to 32 Mbytes on board
- **Display** Programmable color LCD controller
  - Built in driver supports up to 640 x 480 x 8-bit color
  - Supports STN, Color STN, TFT, DSTN
- **Touch Screen** Four wire resistive touch controller (ADS7843)
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN 91C111 (MAC & PHY)
- **Audio** Audio codec AC97 (Wolfson WM9708)
- **I2C**
- **PC Card Expansion**
  - CompactFlash Type 1 card (memory-mode only) - PCMCIA of CF (2 slots)
- **USB** One USB 1.1 Host
- **Serial Ports** Three 16C550-like, standard UARTs
- **Timers/Counters** Four Channels
- **A/D** Six Channels
- **CAN** Two Channels Ver. 2.0
- **GPIO** Programmable depending on peripheral requirements
- **SPI** Supports Motorola SPI
- **Software**
  - Windows™ CE BSP available
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37" (60.2 mm) long x 2.67" (67.8 mm) wide x 0.19" (4.9 mm) high
  - 144-pin SODIMM connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit (Model # SDK-SH7760-10-6416)

 411 WASHINGTON AVE N SUITE 101 MINNEAPOLIS MN 55401 TEL:612.672.9495 FAX: 612.672.9489 WWW.LOGICPD.COM

PN: 70000035 Rev C

1.2 Acronyms

AC'97	Audio CODEC 97
ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CF	CompactFlash
CMT	Compare Match Timer
CODEC	Coder Decoder
CPLD	Complex Programmable Logic Device
CPG	Clock Pulse Generator
DAC	Digital to Analog Converter
DC	Direct Current
DMAC	Direct Memory Access Controller
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative/Discharge
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIR	Fast Infrared
FIFO	First In First Out
GPIO	General Purpose Input Output
HAC	Hitachi Audio CODEC
HAL	Hardware Abstraction Layer
HCAN	Hitachi Controller Area Network
HSPI	Hitachi Serial Protocol Interface
HUDI	Hitachi User Device Interface (JTAG compliant)
IC	Integrated Circuit
I^2C	Inter-IC
I^2S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LOLO	LogicLoader™
MMC	Multimedia Card
NC	No Connect
NIC	Network Interface Controller
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Slow Infrared
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

- SH7760-10 Card Engine IO Controller Specification
- LogicLoader™ User's Manual
- SH7760 Hardware Manual
- Altera MAX 7000A CPLD data sheet (EPM7128)
- Altera Device Package Information data sheet
- Altera Ordering Information
- Texas Instruments (Burr-Brown) ADS7843 data sheet
- Wolfson WM9708 AC'97 Audio CODEC data sheet

1.4 SH7760-10 Card Engine Block Diagram

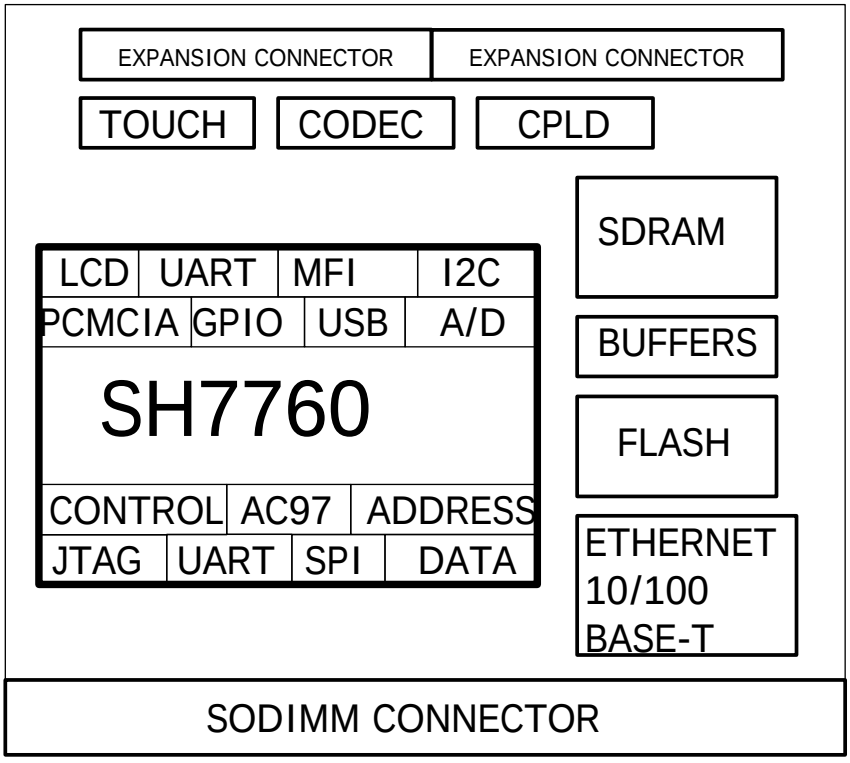


Figure 1.1: SH7760-10 Card Engine Block Diagram

1.5 Electrical, Mechanical, and Environmental Specifications

1.5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC IO, Peripheral Supply Voltage (VIO), and Analog Supply Voltage	3.3V, 3.3V_uP_SDRAM 3.3VA	-0.3 to 4.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.1	V
Positive Voltage on any pin, with respect to DC IO and Peripheral Supply Voltage		VIO + 0.3	V
Negative Voltage on any pin, with respect to DGND		-0.3	V
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstr	-55 to 125	°C

IMPORTANT NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.5.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	TBD	406	600	mA	2
DC IO Supply Standby Current	TBD	TBD	TBD	mA	2
DC IO Supply Sleep Current	TBD	TBD	TBD	mA	2
DC Core Supply Voltage	1.4	1.5	1.6	V	1
DC Core Supply Active Current	TBD	220	730	mA	2
DC Core Supply Standby Current	TBD	TBD	250	µA	2
DC Core Supply Sleep Current	TBD	90	160	mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input Signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.6		VIO	V	
Output Signal Low Voltage	GND		0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. This test was performed with the 91C111 chip power disabled.
3. Contact Logic for more information on an industrial temperature SH7760-10 Card Engine.
4. May vary depending on Card Engine configuration.

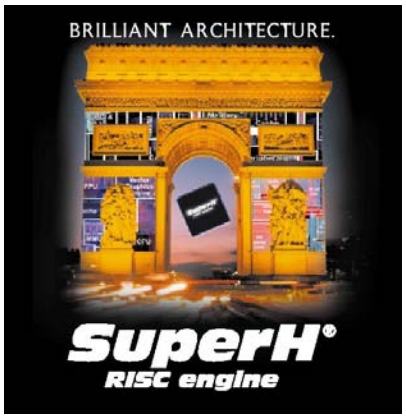
2 Electrical Specification

2.1 Microprocessor

2.1.1 SH7760 Microprocessor

The SH7760-10 Card Engine uses Renesas' highly integrated SoC SH7760 microprocessor. This specific microprocessor employs a 32-bit SH-4 RISC core to provide many integrated on-chip peripherals including:

Integrated SuperH SH-4 Core
- 32-bit RISC-type SuperH RISC Engine CPU
- 16 KB instruction cache
- 32 KB operand cache
- MMU
- 4 GB logical address space
- 5 stage pipeline



Integrated LCD Controller
- Up to 640 x 480 Resolution (8-bit)
- Supports STN, DSTN, TFT
- Up to 64,000 colors

Three UART's (SCIF)
- 128-byte Tx/Rx FIFO
- RTS/CTS hardware flow control

USB Host
- USB Rev 1.1
- OHCI Rev 1.0

HSPI
HCAN2 Module (supports CAN)
AC'97 CODEC interface
Smart Card interface (ISO7816)
Up to 70 General Purpose I/O Signals (69 I/O, 1 O)
10 I/O ports (multiplexed)
10-bit ADC (4-Channel)
8 DMA Channels
4 Counter/Timers
Low Power Modes

See Renesas's SH7760 Hardware Manual for additional information.

IMPORTANT NOTE: Please see http://www.renesas.com/eng/ for any errata on the SH7760.

2.1.2 SH7760 Microcontroller Block Diagram

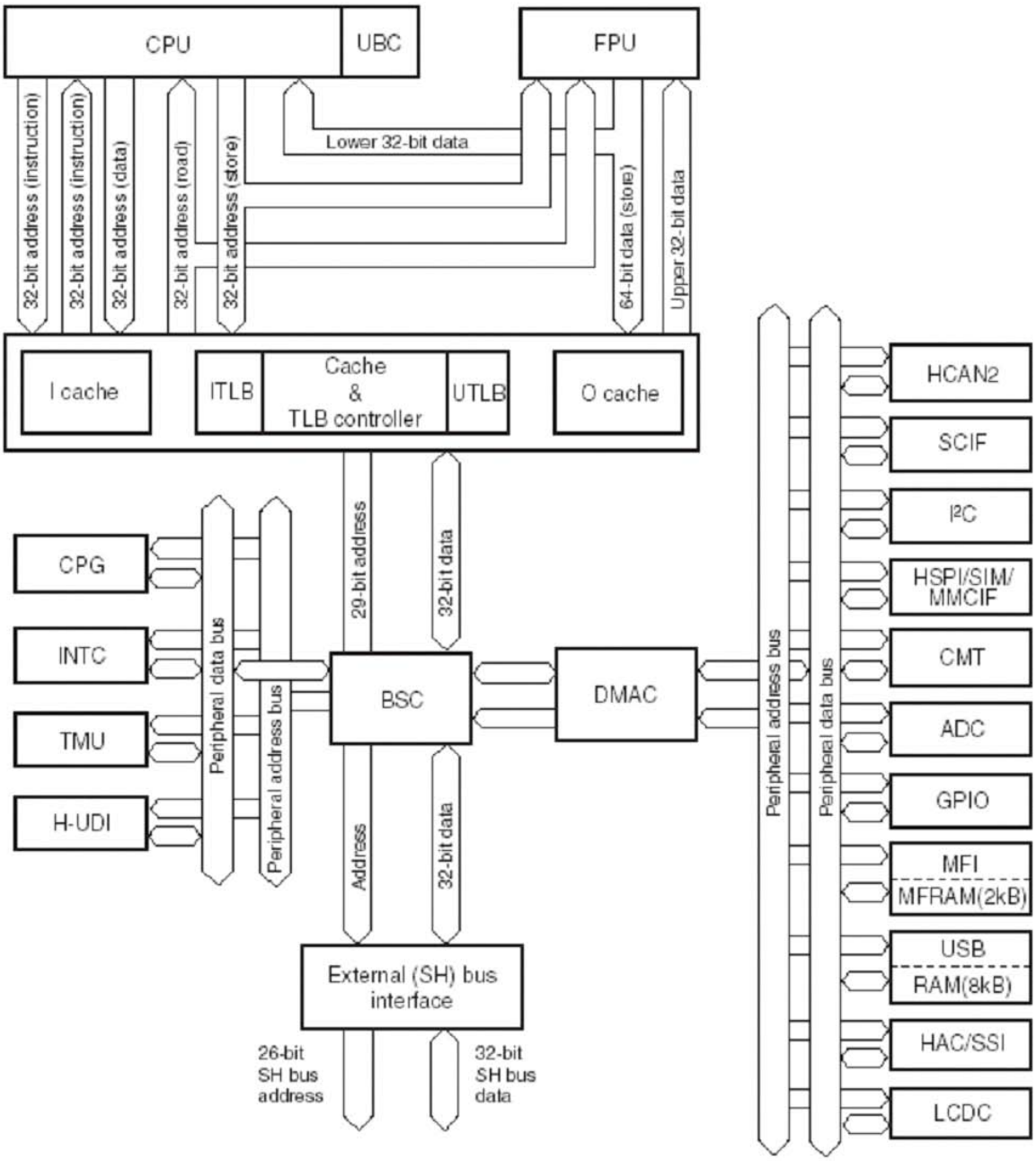


Figure 2.1: SH7760 Microcontroller Block Diagram

2.2 Clocks

The SH7760 processor can use any of 6 different clock-operating modes and generates up to 5 individual clocks from a single crystal input. Logic has initialized these clocks to specific values, though different applications may require different clocking requirements. For more details on changing the clock settings, see the SH7760 Hardware Manual.

Internally, the SH7760 processor uses three PLL circuits to step the clock frequencies up and 3 frequency dividers to step them down in order to create the 5 independent clock frequencies. There are three main clocks that are generated from the input clock: CPU clock (LCK), bus clock (BCK), and peripheral clock (PCK).

By default the SH7760-10 Card Engine puts the processor into “Clock Mode 3” and turns on the on-chip oscillator, thus setting the input crystal range at 16-22MHz. In Clock Mode 3, the internal multipliers are defined as 12:4:2 times the input clock for the CPU, Bus, and Peripheral clocks, respectively. Since a 16.6666MHz crystal is used as the input clock, this sets the CPU core speed to 200MHz, the bus speed to 66.6MHz, and the peripheral clock speed to 33.3MHz.

Besides the input clock crystal to the processor, there are oscillators on the SH7760-10 Card Engine. These are used to generate the LCD_CLK (40MHz) and UCLK (48MHz) signals for the LCD and USB components, respectively.

Other clock speeds can be supported and modified in software for specific user applications.

The SH7760-10 Card Engine provides two clock signals for external use off of the 144-pin SODIMM connector: uP_BUS_CLK and uP_AUX_CLK. Both signals are initialized to 66.6MHz. The signal uP_BUS_CLK is used on the Card Engine as the primary clock for the on-board SDRAM and CPLD. It is recommended that designs use the uP_AUX_CLK signal as a bus reference clock and only use the uP_AUX_CLK as a reference in order to minimize clock loading.

SH7760 Microcontroller Signal Name	SH7760-10 Card Engine Net Name	Default Software Value in LogicLoader™
LCK	N/A	200 MHz
DCK	uP_AUX_CLK	66.6 MHz
CKIO	uP_BUS_CLK	66.6 MHz
PCK	N/A	33.3 MHz

2.3 Comparable Match Timer

The SH7760-10 Card Engine offers an elaborate CMT that provides a 4-channel auto-reload 16/32-bit timer setup. This unit has two major modes of operation: it can be configured as a four-channel timer/counter unit that contains a 32-bit free running timer as a common time-stamp for four 32-bit capture/compare registers or as four 16-bit timer/counters with count enables. In the latter mode, this results in four independent incrementing/decrementing blocks. For information on how to setup the timer/counter modes, see the SH7760 Hardware Manual.

2.4 Memory

2.4.1 Synchronous DRAM

The SH7760-10 Card Engine’s SDRAM data bus interface is 32 bits wide. The SDRAM memory density can be configured as 16, 32 or 64MB depending on customer requirements. The default memory density for the SH7760-10 Card Engine on the SDK, IDK and custom boards is 32MB.

2.4.2 Direct Memory Access Controller

The Renesas SH7760 processor offers an eight-channel internal DMAC. Using the DMAC reduces the load on the CPU and increases the operating efficiency of the SH7760 processor. During the external request 2-channel mode, two DMAC channels are available for use on the SH7760-10 Card Engine through uP_nDREQ0 and uP_nDREQ1 pins. Refer to the SH7760 Hardware Manual for more information on using Direct Memory Access on this Card Engine.

2.4.3 NOR Flash

The SH7760-10 Card Engine uses a 32-bit memory bus (split into two 16-bit channels – one to each flash chip) to interface to Intel StrataFlash flash memory chips. The on-board Card Engine flash memory density can be configured as 8, 16, or 32 MB, depending on the user's flash requirements and cost constraints. Logic's default flash configuration for the SH7760-10 Card Engine is 16 MB on the SDK board and 32 MB on the IDK board.

Because flash is one of the most expensive components on the SH7760-10 Card Engine, it is important to select a size that will best suit the end application in order to reduce overall system cost.

It is possible to expand the system's non-volatile storage capability by adding external flash IC's, CompactFlash memory cards, or other non-volatile storage (such as NAND flash). See the SH7760-10 Application Kit for reference designs or contact Logic for other possible peripheral designs.

2.4.4 CompactFlash (Memory-Mapped Mode Only)

For applications that require additional non-volatile storage, the SH7760-10 Card Engine uses the on-board CPLD to provide the necessary signals for a memory mode only CompactFlash card interface. This interface only supports CompactFlash Type I memory-only cards, but is very useful for expanding the system's non-volatile memory in an expandable and cost effective way.

The SDK reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. Hot-swapping capability can be achieved by using additional hardware on the user's daughter board. See the SH7760-10 IO Controller Specification for further details on CompactFlash use.

IMPORTANT NOTE: The CPLD CompactFlash interface supports memory-mapped mode only. The PCMCIA/CF memory or I/O mode interface should be used if additional PCMCIA/CF card support is required.

The entire SH7760-10 Card Engine can support 2 PCMCIA and one Single I/O mode CompactFlash, or 3 CompactFlash cards with one in I/O mode only.

2.5 PCMCIA/CF

The SH7760-10 Card Engine can provide up to two slots of full memory and I/O mode PCMCIA or CompactFlash support. The full interface (control and bus) for one slot is included on the Card Engine, but an additional external latch is required to implement the second slot. The IDK reference design has example designs for the dual slot implementation.

The PCMCIA/CF interfaces are memory mapped to the PCC capable areas of the SH7760-10 Card Engine. The single fully supported slot is mapped to memory area 6, and the second external slot is mapped to memory area 5. Please see the SH7760 Processor Hardware Manual for additional information.

2.6 MultiMediaCard

The SH7760-10 Card Engine supports a MMC interface that complies with MMC System Specification v2.11. This interface supports MMC mode and allows for 20Mbit/s (maximum) transfers for the card interface at a peripheral operating clock of 20MHz. For more detailed information see the MultiMediaCard Association System Specification, available at www.mmca.org.

2.7 10/100 Ethernet Controller

The SH7760-10 Card Engine uses the SMSC 91C111 10/100 single chip Ethernet Controller to provide a full duplex, 10/100 BaseT, auto negotiation capable, network interface. Six signals from the 91C111 NIC are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LED's. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. The Zoom IDK and SDK reference designs include the impedance matching circuit.

IMPORTANT NOTE: The ENEEP signal on the SMSC 91C111 is connected to a zero ohm resistor that is not populated. This is because the ENEEP signal has a weak internal pull-up in the SMSC 91C111 and if the signal is tied low it low will disable the serial EEPROM interface.

2.8 Audio

The SH7760 processor contains two audio interfaces: the Hitachi Audio CODEC (HAC) and the Serial Sound Interface (SSI). The SH7760-10 Card Engine interfaces the HAC port to a Wolfson WM9708 CODEC. The WM9708 provides full duplex 18-bit CODEC functions and supports variable sample rates from 8 to 48 kHz. The Wolfson chip uses an on-board 24.576MHz crystal to generate the AC'97 master clock frequency.

If a different CODEC option is needed, Logic has interfaced different high performance audio CODEC's with our Card Engine products. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

IMPORTANT NOTE: See Intel's specifications for more information on the AC'97 standard (available on the Internet at http://www.intel.com/design/chipsets/audio/).

2.8.1 HAC

The SH7760 processor's HAC interface (AC'97 v2.1 compliant) is used to communicate with the Wolfson WM97808 CODEC. There are three outputs from the WM9708 CODEC exported to the Card Engine's external connectors: CODEC_OUTL, CODEC_OUTR, and MFP34 - MONO_OUT. These signals are available from the J1A and J1B 80-pin expansion connectors.
IMPORTANT NOTE: The SH7760 processor is equipped with a second HAC channel that is used to implement other functions on the Card Engine. If a second HAC channel is needed, it may be possible to reconfigure the system to use this channel; please contact Logic for any assistance in this matter.

2.8.2 SSI

The Serial Sound Interface on the SH7760-10 is a 2-channel module that is capable of bi-directional transfer in order to communicate with various audio devices. This module is compatible with a variety of devices that use the Phillips SSI format. SSI is not implemented on the SH7760-10 Card Engine; please contact Logic for any assistance on using the built-in SSI function.

2.9 Video Interface

The SH7760 processor has a built in LCD controller supporting STN, dual-STN, and TFT panels at up to 640 x 480 x 8-bit or 640 x 240 x 16-bit color resolution. See the SH7760 Hardware Manual for further information on the integrated LCD controller. The signals from the SH7760's LCD controller are organized by bit and color and are exported to the J1A expansion connectors. Logic has written software to interface to numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller may affect processor performance on the SH7760-10 Card Engine. Selecting different display resolutions and color bits per pixel will vary processor bus load.

IMPORTANT NOTE: External memory devices that assert the asynchronous nWAIT signal or the nCHRDY signal may create a bus bandwidth bottleneck which can portray itself in LCD screen flicker when using the internal LCD controller on the SH7760 processor. This is most commonly seen in resolutions over 320 x 240 @ 16bpp when using the PCMCIA/CF interface.

2.10 Serial Interfaces

The SH7760-10 Card Engine comes with the following synchronous and asynchronous serial channels: UARTA, UARTB, UARTC, I2S, HSPI, and HCAN. If additional serial channels are required, please contact Logic for reference designs.

2.10.1 UARTA

The UARTA interface on the SH7760-10 Card Engine uses one of the SH7760 microprocessor's SCIF ports (Serial Communications with FIFO). This is a high-speed full duplex serial interface with 128-byte FIFO's (asynchronous or synchronous). UARTA is the main UART serial channel on the SH7760-10 Card Engine and offers SCIF0_RTS and SCIF0_CTS as modem control signals. UARTA is available on the J1C 144-pin SODIMM connector. For more information and details on how to set the UART baud rate, please see the SH7760 Hardware Manual.

2.10.2 UARTB

The UARTB interface on the SH7760-10 Card Engine uses one of the SH7760 microprocessor's SCIF ports (Serial Communications with FIFO). This is a high-speed full duplex serial interface with 128-byte FIFO's (asynchronous or synchronous). UARTB is the secondary UART serial channel on the SH7760-10 Card Engine and offers SCIF1_RTS and SCIF1_CTS as modem control signals. UARTB is available on the J1B 80-pin expansion connector. For more information and details on how to set the UARTB baud rate, please see the SH7760 Hardware Manual.

2.10.3 UARTC

The UARTC interface on the SH7760-10 Card Engine uses one of the SH7760 microprocessor's SCIF ports (Serial Communications with FIFO). This is a high-speed full duplex serial interface with 128-byte FIFO's (asynchronous or synchronous). UARTC is the third UART serial channel on the SH7760-10 Card Engine. UARTC is available on the J1B 80-pin expansion connector. For more information and details on how to set the UARTC baud rate, please see the SH7760 Hardware Manual.

IMPORTANT NOTE ON ALL UART CHANNELS: The signals from the Card Engine are TTL level signals, not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the SDK and IDK kits. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

2.10.4 Inter-IC Interface (I2C)

The SH7760-10 Card Engine provides an on-chip 2-Channel I2C interface that is compatible with the Phillips I2C interface. This I2C bus allows the SH7760 to communicate directly with other I2C-compatible devices. The I2C bus allows device communication over two lines – a data and a clock line. For more information on how to use the I2C bus, see both the SH7760 Hardware Manual and the Phillip's I2C Interface Specification.

IMPORTANT NOTE: Though the SH7760 is compatible with the Phillips I2C interface, it does use a different register structure to control the IC than found in the Phillips implementation.

2.10.5 HSPI

Synchronous serial communications on the SH7760-10 Card Engine may be accomplished through the Hitachi Serial Protocol Interface (HSPI). The HSPI interface supports both master and slave mode. The bit rate is selectable via register-controlled baud-rate generator. The HSPI signals are available off the J1C 144-pin SODIMM connector. Please see the SH7760 Hardware Manual for further information.

2.10.6 HCAN

The SH7760-10 offers a dual channel Hitachi Controller Area Network 2 (HCAN2) module that conforms to both CAN v2.0A/2.0B and ISO-11898 specification guidelines. This module serves to control the Controller Area Network provided for real-time communication in automobiles and industrial equipment. CAN transfer rates are selectable up to a rate of 1Mbit/s. For more information on using HCAN, refer to the SH7760 Hardware Manual or CAN specification 2.0B.

2.11 USB Interface

The SH7760-10 Card Engine provides a USB Host Controller module that is fully compliant with the USB v1.1 and Open HCI v1.0 specifications. The module supports 1 USB port with up to 127 endpoint communications and both full-speed (12Mbits/sec) and low-speed (1.5Mbits/sec) USB transfers. The USB interface on the SH7760 is available for external use off the J1A 80-pin connector. Please see the SH7760 Hardware Manual for further information on how to properly use these features.

IMPORTANT NOTE: In order for USB to be correctly implemented on the SH7760-10 Card Engine, additional impedance matching circuitry needs to be added onto the USBP and USBM signals. USB 1.1 requirements specify that the impedance on each driver must be between 28-44Ω. For reference, see the impedance matching circuit on the Logic SDK or IDK board.

IMPORTANT NOTE ON USB FULL-SPEED MODE: There is a known issue with USB host under full-speed mode on the SH7760 processor in which a device may be improperly disconnected (SE0 will occur if >28 bits=0 in a received data packet). Please reference technical notices for the HD6417760BP200QS for further information.

2.12 Touch Interface

The SH7760-10 Card Engine implements the popular TI ADS7843 12-bit sampling ADC touch controller, supporting standard 4-wire resistive touch panels. The touch controller is communicated to via the on-board CPLD that provides a parallel to SPI interface to the SH7760 microcontroller.

Please see the SH7760-10 IO Controller Specification and the TI ADS7843 specification for more information.

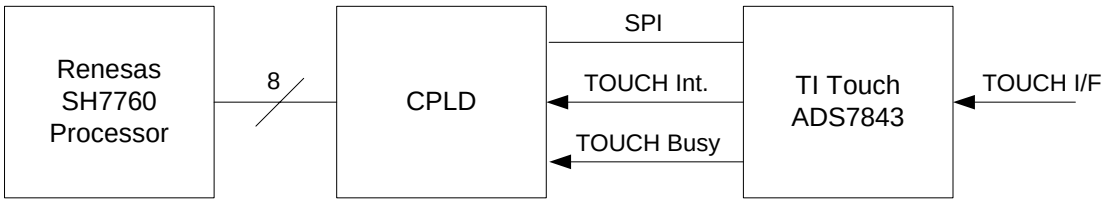


Figure 2.2: Touch Controller Block Diagram

2.13 General Purpose Analog & Digital I/O

Logic designed the SH7760-10 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins provided on the Card Engine's external connectors that interface to the SH7760 processor and the CPLD. Some of these GPIO pins are interrupt capable while other signals are input or output only. Please see the Pin Descriptions in Section 5 for details.

The SH7760-20 Card Engine provides 6 ADC (Analog to Digital Converter) channels – four directly from the SH7760 processor and 2 from the ADS7843 Touch Chip. These signals are available on the J1A expansion connector.

If certain peripherals are not needed (e.g., the LCD controller, chip selects, IRQs, UARTS, AC97, PCMCIA and CompactFlash, Smart Card Interface, or BMI interface) then it is possible to reconfigure the peripheral pins as GPIO pins to gain extra GPIO. Please see the tables in Section 5.4 for a list of the available GPIO trade-offs.

2.14 CPLD

Please see the SH7760-10 IO Controller Specification for CPLD information.

2.15 Serial EEPROM Interface

The SH7760-10 Card Engine contains a 1kb serial EEPROM for non-volatile configuration or state storage. The serial EEPROM is connected to the SH7760 processor via the CPLD through the same SPI interface as is used for the touch controller. See Figure 2.3, below. For more information please view the SH7760-10 Card Engine IO Controller Specification.

Figure 2.3: Serial EEPROM Block Diagram

2.16 Expansion Options

The SH7760-10 Card Engine was designed to be easily expandable. The entire local bus of the processor as well as serial "chainable" buses are provided on the external connectors to allow for easy peripheral additions. Some of these signals are buffered and brought out to the 144-pin SODIMM connector and two 80-pin expansion connectors. See the SH7760-10 Card Engine schematics for more detail. A user may expand the Card Engine's functionality by adding PCI or ISA devices. Logic has used other Audio CODECs, Ethernet IC's, co-processors, and components on reference designs and other Card Engine boards. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The SH7760-10 Card Engine was designed to be a highly integrated, high performance, horizontal platform that could meet the peripheral, performance and budgetary needs of for a wide variety of products. This Card Engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64 MB SDRAM
- Flexible flash footprint: 8, 16, or 32 MB StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional Wolfson WM9708 Audio CODEC
- Optional TI ADS7843 Touch Controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all Card Engine peripheral hardware reset pins are connected to either the MSTR_nRST net or to the RESET_HIGH net as shown in the figure below. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the SH7760-10 Card Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems.

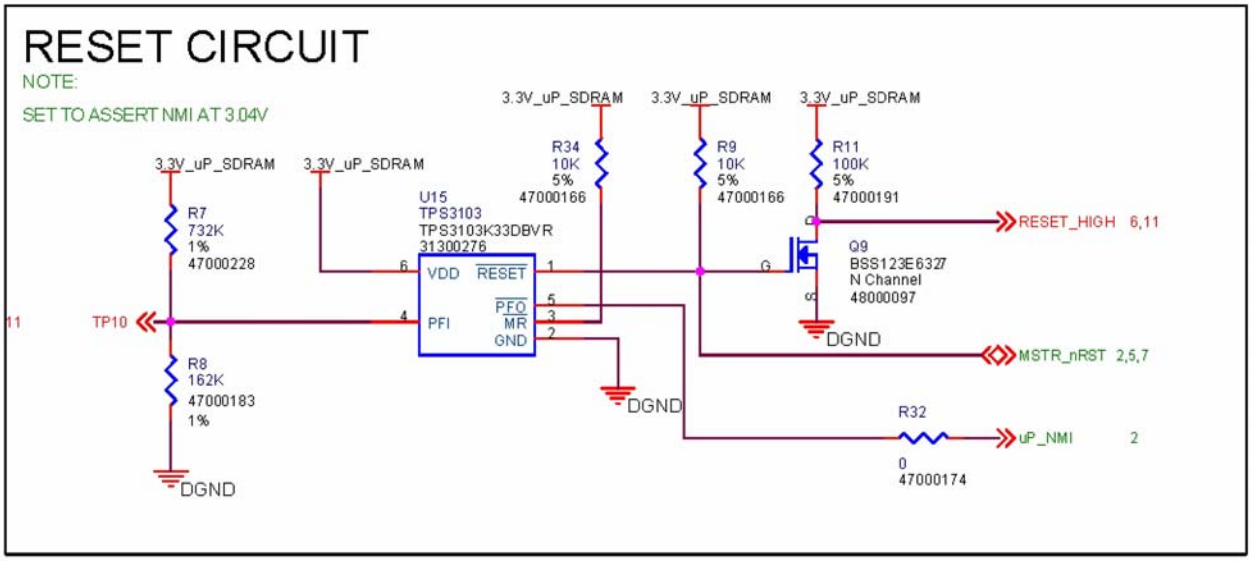


Figure 3.1: Reset Circuit

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user cannot be certain to retain information stored in SDRAM. The data loss may occur because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal. The RESET_HIGH signal, on the other hand, is the active high output of the reset circuit and is not provided as part of the Card Engine connector interface.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See the section entitled "Power Management" for further details.

There are two conditions that will cause a system-wide reset: power-on or a low pulse on the MSTR_nRST signal.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 2.941V. Once the 3.3V_uP_SDRAM supply surpasses 2.941V, the reset chip will trigger a rising edge of MSTR_nRST after a 65-195ms delay (130ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that any external assertion source that triggers the MSTR_nRST signal, analog, or digital de-bouncing be used to generate a clean one shot reset signal.

Power Fail:
The power fail comparator input pin (PFI pin) is implemented to trigger the processor's NMI pin to initiate a hardware low power mode. Please see the TI TPS3103 data sheet at http://www.ti.com/ for additional details on reset timing and thresholds.

3.2.2 Soft Reset

Logic has created a soft reset (also called "manual reset") signal, uP_SW_nRESET, to be used as a reset for the SH7760's internal registers without affecting the peripherals on the rest of the board or the data stored in SDRAM. In the case of a uP_SW_nRESET low pulse, the operation of the external clocks are not interrupted, allowing the processor to reset while maintaining the SDRAM contents.

The Bus State Controller is not initialized in the manual reset process, allowing for refreshing operations to continue. Following the assertion of uP_SW_nRESET, the SH7760 transitions to the Exception-Handling state and starts executing the user-coded exception-handling program. Upon completion of the exception program, the processor transitions to the Program Execution State and is ready to execute program instructions. The uP_SW_nRESET signal is an input to the SH7760 processor's manual reset input pin.

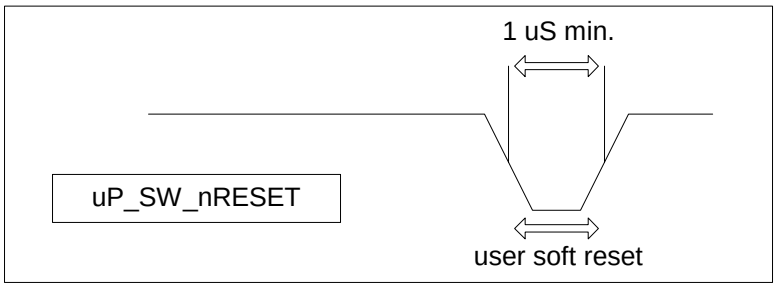


Figure 3.2: Soft Reset

See the SH7760 Hardware Manual for additional information on register conditions after a soft (manual) reset.

3.3 Interrupts

There are five interrupt signals from the SH7760-10 Card Engine that are reserved for external interrupt sources: uP_IRQA, uP_IRQB, uP_IRQC, uP_IRQD, and uP_NMI. By default, the SH7760-10 Card Engine interrupts are set to trigger on a LOW level and are pulled up to 3.3V_uP_SDRAM by 10k resistors. In terms of priority, NMI has the highest, followed by interrupts A-D, which are in order of most dedicated/highest priority to least dedicated/lowest priority. The uP_NMI interrupt should only be used in time critical applications. In Logic's software BSP's, the uP_NMI signal is used for power management intervention.

IRQD is routed through the CPLD in order to allow other interrupt requests from the wired LAN chip, touch chip, and application board to access the processor. For specifics on how this interrupt sharing and masking is used, see the SH7760-10 Card Engine IO Controller Specification.

The SH7760-10 Card Engine also has other GPIO pins that can be used as external interrupts. Please review the Pin Multiplexing and Initialization tables in this manual for more information. Contact Logic for more information in implementing additional interrupts in your design.

See the SH7760 Hardware Manual for more information on interrupt sources.

3.4 H-UDI JTAG Debugger Interface

The SH7760 microprocessor has a Hitachi User Debugging Interface (H-UDI) implemented through a JTAG-compatible interface. Renesas provides an E10A for SH7760 PCI or PCMCIA emulator that connects to this interface for debugging purposes. The following signals make up the JTAG interface to the SH7760, for connection to an E10A emulator card: uP_nTRST, uP_TMS, uP_TDO, uP_TDI, and uP_TEST2.

These signals should interface directly to a 14-pin 0.1" through-hole connector as demonstrated in Logic's circuit schematics in the SDK, IDK or other reference designs. The emulator cards are available from Renesas in either PCI or PCMCIA format, and function under supported operating systems (please see http://www.renesas.com/eng/ for a list of available drivers).

This H-UDI JTAG connection is very useful when:

- Debugging new hardware
- Debugging low level software
- Recovering a board that has a corrupted boot-block

Renesas also provides eXDI plug-in drivers to support Microsoft WindowsCE Platform Builder as a hardware-debugging tool. By using the eXDI functionality, it is possible to debug your low level WindowsCE code using the Platform Builder interface with very little else functioning on the system.

IMPORTANT NOTE: When laying the 14-pin connector out, realize the Renesas pin numbering does not conform to a standard 14-pin 0.1" through-hole connector pin numbering scheme. See Logic's reference designs for further details. Contact Renesas http://www.renesas.com/eng/ for ordering information for E10A emulators.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the SH7760-10 Card Engine was designed to have the following five power rails, 3.3V_uP_SDRAM, 3.3V, 3.3VA, 3.3V_WRLAN, and VCORE. All power areas are inputs to the Card Engine with the exception of 3.3V_WRLAN, which is an output from the Card Engine.

3.5.1.1 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins must be connected to a 3.3V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in this section below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the SH7760-10 Card Engine. This supply must stay within the acceptable levels specified in Section 1.5.1 of this manual, unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane power all analog peripheral supply pins. The 3.3VA supply must stay within the acceptable levels specified in Section 1.5.1.1 of this manual, except during power-off and critical power conditions. The analog power pins on the SH7760 are connected to the VCORE voltage with low-pass filtering.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This “power” supply net is an output from the Card Engine and is controlled through a registered bit in the on-board CPLD. For more details on this specific control bit, see the SH7760-10 Card Engine IO Controller Specification manual for specific details. Logic’s software BSP asserts this signal in order to properly manage power in the LAN91C111 Ethernet chip. Software power management does not put the part in a low enough power state for many applications.

The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the Card Engine will try to power itself through the impedance matching resistors. Please see Logic’s schematics for the SDK or IDK reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the Card Engine is to power the 91C111 chip separately and allow for complete, but independent shut down. Furthermore, the 3.3V_WRLAN output from the Card Engine is required to completely isolate the LAN circuit so that it is not back powered through the impedance matching resistors.

3.5.1.5 VCORE

The VCORE input pins are connected to a 1.5V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Section 1.5.1.1). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please see the description of Standby mode later in this section.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The SH7760-10 Card Engine was designed with these aspects in mind and provides maximum flexibility in software and system integration.

On the SH7760 there are many different software configurations that drastically effect power consumption: processor core clock frequency, processor bus clock frequency, processor peripheral clocks, processor power management states (Normal, Reset, Power-Down), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the LogicLoader™ User's Manual or appropriate BSP manual.

IMPORTANT NOTE: Most of the SH7760-10 Card Engine hardware architecture was designed for low power battery operated applications. The Altera CPLD, however, was chosen to optimize cost over power savings. If power-optimization is the primary goal of the design; please contact Logic for other design configurations in this area.

3.5.3 Peripherals

Most peripherals provide software programmable power states. Sometimes, however, these programmable power states may not be the best solution. The SMSC 91C111 controller, for example, has software programmable power states which may not be sufficient for some applications. In order to solve this problem, Logic has provided hardware to cut power to the 91C111 IC. Please see the appropriate data sheets and the SH7760-10 Card Engine IO Controller Interface Specification for more information.

The SH7760-10 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3V_WRLAN, 3.3VA, and VCORE for a flexible hardware design. See Figure 3.3, below.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_ SDRAM	3.3VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to refresh.
3.3V	3.3VDC	Connects to the digital peripherals on the Card Engine.
3.3VA	3.3VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
VCORE	1.5V	Connects to the processor core voltage. See information on each specific processor for the VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperatures, etc.
3.3V_WRLAN	3.3V (This Pin is an output, see section 3.5.1.4)	Provides power to the SMSC 91C111 processor from the 3.3V area. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the IO Controller Specification for controlling this signal.

IMPORTANT NOTE: Because the power management on the SMSC 91C111 is not suitable for many applications, the PMOS FET was added to control power input into the wired LAN.

Figure 3.3: Power Plane Diagram

3.5.4 System Power States

The SH7760-10 Card Engine power management's scheme was designed to be easy to use. Logic has provided hardware signals to activate three different power states (Normal, Reset, and Power-Down) on the SH7760-10 Card Engine that take advantage of the SH7760 microprocessor's power management features. The installed software BSP must support these power management states in order to function correctly. See the BSP documentation for more information.

The SH7760 microprocessor provides for five power management modes in the power-down state: NORMAL, STANDBY, SLEEP, DEEP SLEEP, and Module STANDBY. A very useful software and hardware development feature are the microprocessor status lines that are exported as the nets

Status2	Status1	Operating Status
High	High	Reset
High	Low	Power-Down (Sleep)
Low	High	Power-Down (Standby)
Low	Low	Normal

Note: These signals are inverted off the Card Engine on the application board

The status lines uP_STATUS1 and uP_STATUS_2 are hardware-controlled signals that signify the current operating mode of the microprocessor. See table with status information, above.

IMPORTANT NOTE: The BSPs available from Logic for the different operating systems supported on the SH7760-10 Card Engine may not support all power management states. Please see the appropriate BSP documentation for power management modes for more information.

3.5.4.1 Normal Mode

The SH7760-10 Card Engine's normal operating mode is aptly named 'Normal Mode' and contains three different processing states: the program execution state, bus-released state, and exception-handling state. All states transition to the bus-released state on a bus request and return to the same state when the bus is cleared. The exception-handling state is entered on an exception interrupt in the program execution state and returns after the exception is processed. The SH7760 can enter Normal mode from either the power-down mode or the reset state. From reset, Normal is accessed if either the RESET signal or both the RESET and MRESET signals go high (exception-handling state entered). A transition from Power-down mode to Normal occurs either on a bus request (bus-released state entered) or an interrupt (exception-handling state entered).

3.5.4.2 Reset Mode

Reset mode on SH7760-10 Card Engine encompasses two reset states: power-on and manual. In the power-on reset state, the internal state of the CPU and the on-chip peripheral module registers are initialized. In the manual reset state, the internal state of the CPU and registers of on-chip peripheral modules other than the BSC are initialized. Since the BSC is not initialized in the manual reset state, refreshing operations continue. The power-on state is entered when the active-low RESET pin goes low. The manual reset is entered when the active-low RESET pin is high and the active-low MRESET pin is low. To allow a user to access the manual reset state, Logic has provided the uP_SW_nRESET signal (as described in section 3.2.2).

3.5.4.3 Power-Down Mode

There are five power-down modes on the SH7760: sleep, deep sleep, software standby, hardware standby, and module standby. A SLEEP instruction in normal mode will cause a transition to power-down mode. Depending on the status of the STBY bit, the system will then enter sleep mode or standby mode. If it enters sleep mode, the status of the DSLP bit will put the processor into either sleep or deep sleep. In either sleep or deep sleep mode, the clock pulse generator operates, CPU use is halted (registers retained) and the memory contents are retained. Sleep mode is exited on an interrupt or system reset.

Software standby mode stops the clock pulse generator and can also be exited on an interrupt or system reset. Module standby mode is used to halt specific module operations while leaving the system core running; this is the least power effective solution and can be exited on a register clear or reset.

Before asserting the MSTR_nRST signal to re-initialize the system from software standby, the custom application board should be certain that good power has been re-applied to the system or a partial boot condition may result, corrupting SDRAM and causing the system to lose state information.

The different processor power states are shown in Figure 3.4 below.

Power-Down Mode	Entering Conditions	Status						Exiting Method
		CPG	CPU	On-Chip Memory	Peripheral Modules	Pins	External Memory	
Sleep mode	SLEEP instruction executed while STBY bit is 0 in STBCR	Operating	Halted (registers retained)	Retained	Operating	Retained	Refresh-ing	• Interrupt • Reset
Deep sleep mode	SLEEP instruction executed while STBY bit is 0 in STBCR, and DSLP bit is 1 in STBCR2	Operating	Halted (registers retained)	Retained	Operating (DMA halted)	Retained	Self-refreshing	• Interrupt • Reset
Software standby mode	SLEEP instruction executed while STBY bit is 1 in STBCR	Halted	Halted (registers retained)	Retained	Halted	Retained	Self-refreshing	• Interrupt • Reset
Hardware standby mode	Setting CA pin to low level	Halted	Halted	Undefined	Halted	High-impe-dance state	Undefined	• Power-on reset
Module standby function	• Setting MSTP bit to 1 in STBCR • Setting CSTP bit to 1 in CLKSTP00	Operating	Operating	Retained	Specified modules halted	Retained	Refresh-ing	• Clearing MSTP and CSTP bits to 0 • Reset

Figure 3.4: Status in Power-Down Mode

3.6 ESD Considerations

The SH7760-10 Card Engine does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in. The SH7760-10 Card Engine was designed to be low cost and adaptable to many different applications. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SH7760 Memory Map

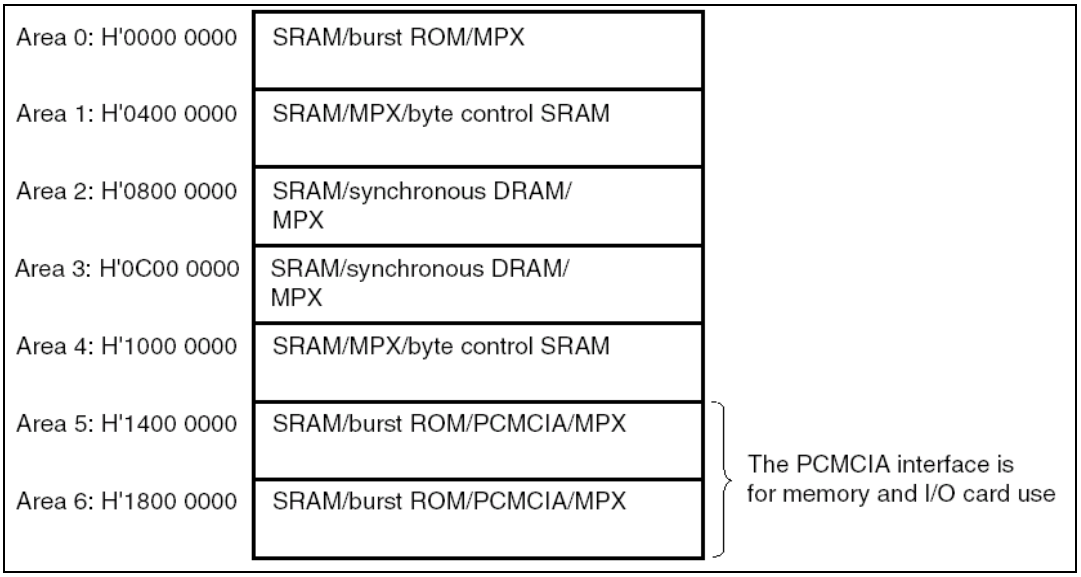


Figure 4.1: SH7760-10 Card Engine General Memory Map

IMPORTANT NOTE: Figure 4.1 shows the general addressing scheme for the memory areas on the SH7760 Processor. Please note that the addresses specified do not include the logical memory mapping offsets. The correspondence between the virtual address and off-chip memory space is shown below in Figure 4.2.

4.1.1 Card Engine Memory Map Description

The table below specifies the intended use for each area of the off-chip memory space, which is allocated above in Figure 4.1.

Chip Select	Bank	Start Address	Memory Description	Bus Width
nCS6	6	0x1800 0000	PC Card Interface/User Area	16/8
nCS5	5	0x1400 0000	PC Card Interface/User Area	16/8
nCS4	4	0x1000 0000	IO Controller Peripherals (fast[1])	16
nCS3	3	0x0C00 0000	SDRAM	32
nCS2	2	0x0800 0000	Video/SDRAM expansion	32
nCS1	1	0x0400 0000	IO Controller Peripherals (slow[1])	16
nCS0	0	0x0000 0000	Boot Device (flash or Off-Board)	32

Note:
1. CPLD peripherals are components that get a decoded chip select from the CPLD (e.g., CPLD memory mapped registers, onboard SMSC 91C111 Ethernet controller. Please see the SH7760-10 IO Controller Specification document for details). These peripherals are separated into two different chip select banks, due to difference in timing: slow and fast.

4.1.2 Virtual/Off-Chip Memory Map

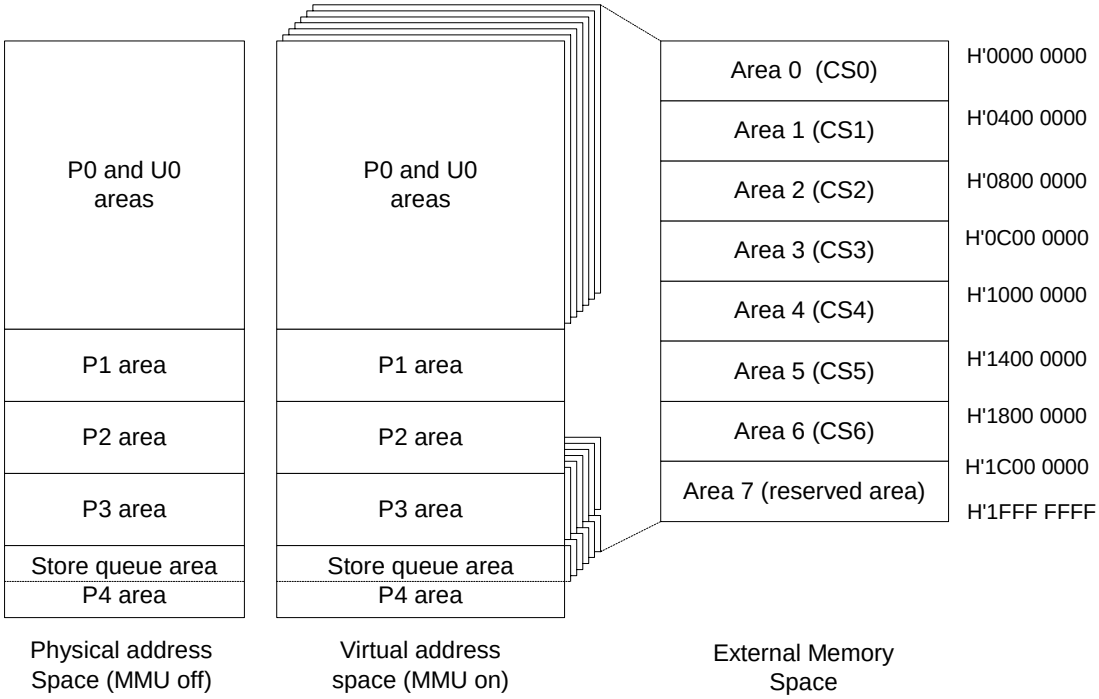


Figure 4.2: Correspondence between Virtual Address and Off-Chip Memory Spaces

4.1.3 Chip Select 1 (CS1) – CPLD Peripherals (slow timing)

The table below indicates how the CPLD decodes chip select 1. For more detailed information see the SH7760-10 IO Controller Specification.

Address Range	Memory Block Description	Size
0x0400 0000 – 0x041F FFFF	(Boot) EPROM Chip Select	2MB
0x0420 0000 – 0x043F FFFF	CF Chip Select	2MB
0x0440 0000 – 0x045F FFFF	ISA-like Bus Chip Select	2MB
0x0460 0000 – 0x05FF FFFF	Reserved - On-Board Expansion	2MB (X13)
0x0600 0000 – 0x06FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x0700 0000 – 0x07FF FFFF	Open – Available for User	1MB (X16)

4.1.4 Chip Select 4 (CS4) – CPLD Peripherals (fast timing)

The table below indicates how the CPLD decodes chip select 4. For more detailed information see the SH7760-10 IO Controller Specification.

Address Range*	Memory Block Description	Size
0x1000 0000 – 0x101F FFFF	Wired LAN Chip Select	2MB
0x1020 0000 – 0x103F FFFF	Card Engine Control Reg	2MB
0x1040 0000 – 0x105F FFFF	Reserved	2MB
0x1060 0000 – 0x107F FFFF	SPI Data Reg	2MB
0x1080 0000 – 0x109F FFFF	SPI Control Reg	2MB
0x10A0 0000 – 0x10BF FFFF	EEPROM SPI Reg	2MB
0x10C0 0000 – 0x10DF FFFF	Interrupt/Mask Reg	2MB
0x10E0 0000 – 0x10FF FFFF	Mode Reg	2MB
0x1100 0000 – 0x111F FFFF	Flash Reg	2MB
0x1120 0000 – 0x113F FFFF	Power Management Reg	2MB
0x1140 0000 – 0x115F FFFF	IO Controller Code Revision Reg	2MB
0x1160 0000 – 0x117F FFFF	Extended GPIO Data Reg	2MB
0x1180 0000 – 0x119F FFFF	GPIO Data Reg	2MB
0x11A0 0000 – 0x11BF FFFF	GPIO Direction Reg	2MB
0x11C0 0000 – 0x11DF FFFF	PCMCIA Status Reg	2MB
0x11E0 0000 – 0x11FF FFFF	PCMCIA Control Reg	2MB
0x1200 0000 – 0x12FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x1300 0000 – 0x13FF FFFF	Open – Available for User	1MB (X16)

For further information on the use of the CPLD peripherals and their control and data registers, please see the SH7760-10 IO Controller Specification document.

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify that the necessary configurations exist (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the Card Engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O	Active Low. This signal initiates a hard reset (power on) – external memory contents are lost during reset. Every peripheral on the Card Engine with a reset line is reset with the assertion of this signal. Refer to SH7760 processor datasheet for register states during or after power on reset. This signal is asserted by an open drain component on the Card Engine and has a 10K pullup to 3.3V_uP_SDRAM.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	uP_SW_nRESET	I	Active Low. This signal initiates a software reset (manual reset) – external memory contents are retained during reset. This pin is connected to the CPLD; please see SH7760-10 Card Engine IO Controller Specification for detailed information on the use of the CPLD based reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nMCS	O	Active Low. Buffered chip select for area 4 of SH7760 memory. This is the "fast" peripheral chip select area. This is set to a 16-bit wide area and should not be changed. See memory map for details.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8	SLOW_nMCS	O	Active Low. Buffered chip select for area 1 of SH7760 memory. This is the "slow" peripheral chip select area. This is set to a 16- bit wide area and should not be changed unless the slow peripherals are not needed. Note: the SLOW_nMCS signal is asserted only when accessing slow areas in the CPLD that are listed as "Open - Available to User." See memory map for details.
9	DGND	I	Digital Ground (0V)

Pin #	Signal Name	I/O	Description
10	MFP31 - VIDEO_nMCS	O	Active Low. Buffered chip select for area 2 of SH7760 memory. This is the "video" chip select area. This chip select is also capable of controlling additional external SDRAM. This is set to a 32-bit wide area and can be changed based on the user's needs. See memory map for details.
11	ETHER_nACT_LED	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nCS	O	This signal is the chip select for boot ROM and is connected to area 0 of SH7760 memory. When uP_MODE3 is low, the off-board EPROM selected for boot and the chip select 0 area width is set by uP_MODE 0 and 1. When uP_MODE3 is high, flash is selected for boot and chip select 0 is set to a 32-bit wide area. In cases where uP_MODE3 is high, the off-board EPROM is available to the user at address range 0x0400 0000 – 0x041F FFFF. See memory map for details.
13	ETHER_nLNK_LED	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in. There is a delay between the falling edge of the chip select (flash or ISA) and falling edge of nIOWR; see the SH7760-10 IO Controller Specification for further details on how this is implemented.
15	nSTANDBY	I	Active Low. CPU power mode signal. A low nSTANDBY signal effects a transition to hardware standby mode. In this mode, all modules stop – interrupts and manual resets are not available. The only way to exit hardware standby mode is by means of asserting a power-on reset via MSTR_nRST. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the SH7760-10 IO Controller Specification for further details.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) output from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid. This signal is generated inside the ISA-like logic in the CPLD; see the SH7760-10 IO Controller Specification for further details.
21	uP_NMI	I	Active Low. The non-maskable interrupt – highest priority - for the CPU. Used to exit power-down mode or as a highest priority interrupt. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.

Pin #	Signal Name	I/O	Description
22	nCHRDY	O	Active Low. When pulled low, the nCHRDY signal generates a high on the uP_RDY signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. Peripherals using this signal must make their outputs open drain, as it shares a bus with the CPLD_nWAIT - PCC_nWAIT signal. See the SH7760-10 IO Controller Specification for further details. This signal is pulled up to 3.3V through a 10K resistor.
23	uP_IRQD	I	Active low external interrupt signal. When an interrupt is asserted on this line, uP_IRQ3 is asserted (IRL Interrupt Request 3 on SH7760-10). uP_IRQ3, in conjuncture with uP_IRQA, uP_IRQB, and uP_IRQC, is used to specify the IRL interrupt level: 0 (‘0000’ - highest-level interrupt request) to 15 (‘1111’ - no interrupt request). uP_IRQD is different from the other interrupts as it is used to pass maskable interrupts from the LAN and touch chips. See the SH7760-10 IO Controller Specification for further details.
24		NC	No internal connection (not implemented on the SH7760-10)
25	uP_IRQC	I	Active Low. IRL Interrupt Request 2 on SH7760-10. This signal, in conjuncture with uP_IRQA, uP_IRQB, and uP_IRQ3, is used to specify the IRL interrupt level: 0 (‘0000’ - highest-level interrupt request) to 15 (‘1111’ - no interrupt request). This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
26	uP_TEST2	I	This signal is used to implement the H-UDI emulator on the SH7760 processor. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor to put the processor in normal operation mode.
27	uP_IRQB	I	Active Low. IRL Interrupt Request 1 on SH7760-10. This signal, in conjuncture with uP_IRQA, uP_IRQC, and uP_IRQ3, is used to specify the IRL interrupt level: 0 (‘0000’ - highest-level interrupt request) to 15 (‘1111’ - no interrupt request). This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
28	uP_nTRST	I	Active Low H-UDI (JTAG) reset. This signal is pulled down to digital ground through a 10K resistor.
29	uP_IRQA	I	Active Low. IRL Interrupt Request 0 on SH7760-10. This signal, in conjuncture with uP_IRQB, uP_IRQC, and uP_IRQ3, is used to specify the IRL interrupt level: 0 (‘0000’ - highest-level interrupt request) to 15 (‘1111’ - no interrupt request). This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
30	uP_TMS	I	H-UDI (JTAG) Mode Select Input. May leave unconnected if not using H-UDI.
31	uP_nBS	O	Active Low. This signal used to indicate the start of a bus cycle. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. Refer to SH7760 processor datasheet for more information on specific Bus Sequences.
32	uP_TDO	O	H-UDI (JTAG) Test Data Serial Output. Leave unconnected when H-UDI port is not in use.
33	uP_nBACK	O	Active Low. This is the Bus Request Acknowledge signal. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. Refer to SH7760 processor datasheet for more information on specific Bus Sequences.
34	uP_TDI	I	H-UDI (JTAG) Test Serial Data Input. May leave unconnected if not using the H-UDI port.

Pin #	Signal Name	I/O	Description
35	uP_nBREQ	I	Active Low. This is the Bus Release Request signal. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. Refer to SH7760 processor datasheet for more information on specific Bus Sequences.
36	uP_TCK	I	H-UDI (JTAG) Test Clock Input. May leave unconnected if not using the H-UDI port.
37	CPLD_nWAIT – PCC_nWAIT	I	This is the asynchronous bus wait signal that is combined with nCHRDY in the on-board CPLD to control the SH7760 processor's nRDY line. If more than one device needs to insert wait states on the bus by asserting this pin low, the devices must implement an open-drain style control. This signal has a 1k ohm pull-up on the Card Engine. For more information, please see the SH7760-10 IO Controller Specification.
38	uP_MODE3	I	Boot select signal (0 = external boot device, 1 = on-board flash). This defaults to high (on-board flash) if left unconnected (pulled to 3.3V through a 10K resistor).
39	uP_UARTA_RTS	O	Active low. Request to send for SCIF port 2 (UARTA).
40	uP_MODE2	I	Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left unconnected (pulled to 3.3V through a 10K resistor).
41	uP_UARTA_CTS	I	Active low. Clear to send for SCIF port 2 (UARTA).
42	uP_MODE1 - uP_PCC_nCE2B	I	Area 0 Bus width setting (uP_MODE1/uP_MODE0): 0/0 = reserved, 0/1 = 8-bit, 1/0 = 16-bit, 1/1 = 32-bit. This defaults to 32-bits when unconnected (pulled to 3.3V_uP_SDRAM through a 10K resistor). When using PCMCIA, this is a PC Card enable signal.
43	uP_UARTA_TX	O	SCIF port 2 (UARTA) data output.
44	uP_MODE0 - uP_PCC_nCE2A	I	Area 0 Bus width setting (uP_MODE1/uP_MODE0): 0/0 = reserved, 0/1 = 8-bit, 1/0 = 16-bit, 1/1 = 32-bit. This defaults to 32-bits when unconnected (pulled to 3.3V_uP_SDRAM through a 10K resistor). When using PCMCIA, this is a PC Card enable signal.
45	uP_UARTA_RX	I	SCIF port 2 (UARTA) data input.
46	uP_nDREQ1	I	Active low. DMA transfer request input from external device. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. Refer to SH7760 processor datasheet for more information on DMA Transfers.
47		NC	No internal connection (not implemented on the SH7760-10)
48	uP_nDREQ0	I	Active low. DMA transfer request input from external device. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. Refer to SH7760 processor datasheet for more information on DMA Transfers.
49		NC	No internal connection (not implemented on the SH7760-10)
50	uP_DRAK1	O	DMA acceptance confirmation that notifies acceptance of DMA transfer request and start of execution to external device that has active low output DREQ 1. Refer to SH7760 processor datasheet for more information on DMA Transfers.
51	nSUSPEND	I	Active low. This signal is one of the CPLD interrupts and is used to suspend SH7760 operations. This pin is connected directly to the CPLD and it is pulled up to 3.3V_uP_SDRAM by a 10k resistor. Software is required for proper suspend operation.
52	uP_DRAK0	O	DMA acceptance confirmation that notifies acceptance of DMA transfer request and start of execution to external device that has active low output DREQ 0. Refer to SH7760 processor datasheet for more information on DMA Transfers.

Pin #	Signal Name	I/O	Description
53	uP_AUX_CLK	O	This signal is a programmable auxiliary clock that is set to 66.6664MHz (max) by the default MD0-MD2 settings.
54	uP_DACK1	O	DMA transfer end notification. Refer to SH7760 processor datasheet for more information on DMA Transfers.
55	DGND	I	Digital Ground (0V)
56	uP_DACK0	O	DMA transfer end notification. Refer to SH7760 processor datasheet for more information on DMA Transfers.
57	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.5V.
58	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.5V.
59	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.5V.
60	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.5V.
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_nReset). Recommend leaving this supply as the only powered supply during Standby power down mode.
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_nReset). Recommend leaving this supply as the only powered supply during Standby power down mode.
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_nReset). Recommend leaving this supply as the only powered supply during Standby power down mode.
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_nReset). Recommend leaving this supply as the only powered supply during Standby power down mode.
65	uP_SPI_FRM	I/O	HSPI (Hitachi SPI) chip select. This signal may be used by application software to frame SPI data transmission or reception.
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 66.6664MHz (max) and is connected to the SDRAM as well as the CPLD. This signal is, by default, unavailable in an effort to reduce on board EMI noise. It can be made available upon request, please contact Logic for more information.
67	uP_SPI_MOSI_TX	O	HSPI (Hitachi SPI) transmit data output.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_MISO_RX	I	HSPI (Hitachi SPI) receive data input. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
70	uP_nRAS	O	Active low Synchronous Memory Row Address Strobe Signal. uP_nRAS is used in synchronizing all SDRAM into row addressing mode. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
71	uP_SPI_SCK	O	HSPI (Hitachi SPI) serial clock. HSPI transmit/receive data is valid on the rising edge of this clock after the uP_SPI_FRM pin goes low. Refer to the SH7760 datasheet for more information on using HSPI.
72	uP_nRD - nCAS	O	Active low signal that indicates a read signal. This is also the Synchronous Memory Row Address Strobe Signal, which is used to synchronize all SDRAM into column addressing mode. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
73	uP_MD0	I/O	Buffered Data Bus bit 0.

Pin #	Signal Name	I/O	Description
74	uP_nMWE3 - DQM3 - PCC_nIOWR	O	Active low. Buffered write enable for buffered data bus bits 31->24. This is also the DQM3 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2 - DQM2 - PCC_nIORD	O	Active low. Buffered write enable for buffered data bus bits 23->16. This is also the DQM2 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMWE1 - DQM1 - PCC_nWE	O	Active low. Buffered write enable for buffered data bus bits 15->8. This is also the DQM1 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0 - DQM0 - PCC_nREG	O	Active low. Buffered write enable for buffered data bus bits 7->0. This is also the DQM0 - PCC_nREG SDRAM signal from the SH7760. Both functions are valid (functionality changes based on memory area accessed).
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active low. When low, this buffered signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal can be used for buffer direction control.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD - PCC_nOE	O	Active low. This buffered signal (connected to the un-buffered uP_nRD – nCAS) is the read strobe that latches data output from external peripherals. It is also the PCMCIA OE signal when areas 5 or 6 are accessed in PCMCIA mode.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the SH7760-10)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection (not implemented on the SH7760-10)
89	DGND	I	Digital Ground (0V)
90	uP_MA0	O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	O	Buffered Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)

Pin #	Signal Name	I/O	Description
108	uP_MA9	O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.
116	uP_MA13	O	Buffered Address Bus bit 13.
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	O	Buffered Address Bus bit 16.
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.
136	uP_MA23	O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	O	Buffered Address Bus bit 24.
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC	O	LCD VSYNC (TFT Signal)
2	LCD_HSYNC	O	LCD HSYNC (TFT Signal).
3	LCD_DCLK	O	LCD Panel Data Clock
4	LCD_DON	O	Active high. LCD display-on signal.
5	LCD_MDISP	O	LCD enable signal (TFT signal).
6	LCD_VEEEN	O	Active high. This signal is the LCD panel VEE enable.
7	LCD_VDDEN	O	Active high. This signal is the LCD panel VCC enable.
8		NC	No internal connection (not implemented on the SH7760-10).
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the SH7760-10).
11		NC	No internal connection (not implemented on the SH7760-10).
12		NC	No internal connection (not implemented on the SH7760-10).
13		NC	No internal connection (not implemented on the SH7760-10).
14		NC	No internal connection (not implemented on the SH7760-10).
15		NC	No internal connection (not implemented on the SH7760-10).
16		NC	No internal connection (not implemented on the SH7760-10).
17	uP_STATUS_1	O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Normal Operation, 0/1 = Standby, 1/0 = Sleep, 1/1 = Reset.
18	uP_STATUS_2	O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Normal Operation, 0/1 = Standby, 1/0 = Sleep, 1/1 = Reset.
19	uP_AC97_BITCLK1	O	Clock input from an AC97 compliant audio CODEC.
20	uP_AC97_RESET	O	Reset line to an AC97 compliant audio CODEC.
21	uP_AC97_SYNC1	O	This signal is the sync output to an AC97 compliant audio CODEC. The CODEC Frequency is set on CODEC to be 48Khz, while the default frequency for the sync is set up to be 2.9491Mhz (14.7456MHz / 5) on the processor.
22	uP_AC97_SD_IN1	I	This signal is the serial data output from the AC97 compliant audio CODEC to the processor.
23	uP_AC97_SD_OUT1	O	This signal is the serial data input to the AC97 compliant audio CODEC from the processor.
24	DGND	I	Digital Ground (0V)
25	uP_A/D1	I	This signal is analog input 1 on the 4-channel, 10-bit resolution ADC on the SH7760.
26	uP_A/D2	I	This signal is analog input 2 on the 4-channel, 10-bit resolution ADC on the SH7760.
27	AGND	I	Analog Ground (0V)
28	uP_A/D3	I	This signal is analog input 3 on the 4-channel, 10-bit resolution ADC on the SH7760.
29	uP_A/D4	I	This signal is analog input 4 on the 4-channel, 10-bit resolution ADC on the SH7760.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio CODEC.
32	CODEC_INR	I	Right channel stereo line input of the audio CODEC.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
35	AGND	I	Analog Ground (0V)

Pin #	Signal Name	I/O	Description
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch panel controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch panel controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch panel controller.
39	TOUCH_TOP	I	This is the X- position input to the four-wire resistive touch panel controller.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. R0 is not connected to the processor itself and therefore is tied to R5.
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1 is connected to LCD_DATA11.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2 is connected to LCD_DATA12.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3 is connected to LCD_DATA13.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4 is connected to LCD_DATA14.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5 is connected to LCD_DATA15.
48	G0	O	The LCD data bus used to transmit data to the LCD module. GREEN 0 is connected to LCD_DATA5.
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1 is connected to LCD_DATA6.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2 is connected to LCD_DATA7.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3 is connected to LCD_DATA8.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4 is connected to LCD_DATA9.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5 is connected to LCD_DATA10.
54	B0	O	The LCD data bus used to transmit data to the LCD module. B0 is not connected to the processor itself and therefore is tied to B5.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1 is connected to LCD_DATA0.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2 is connected to LCD_DATA1.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3 is connected to LCD_DATA2.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4 is connected to LCD_DATA3.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5 is connected to LCD_DATA4.
61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. See the SH7760-10 IO Controller Specification for further details.
62	RSVD_1	O	This signal is routed to the onboard CPLD and is reserved for future use. See the SH7760-10 IO Controller Specification for further details. This signal is pulled up to 3.3V through a 10K resistor.

Pin #	Signal Name	I/O	Description
63	CPLD_GPIO_1	O	This signal is a general purpose I/O, which in this case, is used to drive the GPIO LED on the application board (such as the SDK). For more information on how this signal is driven, see the SH7760-10 IO Controller Specification .
64	CPLD_GPIO_2	IO	This signal is a general purpose I/O. It is controlled by a memory-mapped address in the CPLD. See the SH7760-10 IO Controller Specification for further details.
65	uP_USB2_nOVR_CRNT	I	Active high. This is a data carrier detect signal used to determine whether or not the USB interface is currently in use.
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection (not implemented on the SH7760-10).
68	uP_USB2_PWR_EN	O	Active high. Enables power supply for USB.
69		NC	No internal connection (not implemented on the SH7760-10).
70	uP_USB2_M	IO	USB Host data I/O plus. Route as a differential pair with uP_USB1_M.
71	uP_USB2_P	IO	USB Host data I/O minus. Route as a differential pair with uP_USB1_P.
72*		NC	No internal connection (not implemented on the SH7760-10).
73*		NC	No internal connection (not implemented on the SH7760-10).
74	BUFF_nOE	I/O	Active low. Controls the outputs of the buffers on the Card Engine. When low, the buffers are active and when high, the buffers will be tri-stated. This signal is an input while the signal "uP_nBACK" is low. This signal is pulled up to 3.3V through a 10K resistor.
75	BUFF_DIR_ADDRESS	I/O	Controls the direction of the address lines through the buffers. When low, the address lines are driven B->A, or out from the processor (normal condition). When high, the address lines are driven A->B, or into the processor (bus mastering). See the SH7760-10 IO Controller Specification for further details.
76	BUFF_DIR_DATA	I/O	Active high. Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven B->A, or out from the processor (write cycle). When high, the data lines are driven A->B, or into the processor (read cycle). See the SH7760-10 IO Controller Specification for further details.
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the AC97 compliant audio CODEC. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different Card Engines.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different Card Engines.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled down to ground through a 10K resistor.
2	CPLD_TDO	O	This input transmits data out of the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
3	CPLD_TMS	I	This input indicates the mode of CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
4	CPLD_TDI	I	This input receives data on the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
5	uP_nMRD - PCC_nOE	O	Active low. This buffered signal (connected to the un-buffered uP_nRD – nCAS) is the read strobe that latches data output from external peripherals. It is also the PCMCIA OE signal when areas 5 or 6 are accessed in PCMCIA mode.
6	uP_nMWE1 - DQM1 - PCC_nWE	O	Active low. Buffered write enable for buffered data bus bits 15->8. This is also the DQM1 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
7	uP_nMWE2 - DQM2 - PCC_nIORD	O	Active low. Buffered write enable for buffered data bus bits 23->16. This is also the DQM2 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
8	uP_nMWE3 - DQM3 - PCC_nIOWR	O	Active low. Buffered write enable for buffered data bus bits 31->24. This is also the DQM3 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
9	DGND	I	Digital Ground (0V)
10	uP_PCC_RESET	O	This signal is the active low reset for the off-board PCMCIA interface.
11	uP_nMCS6 - PCC_nMCE1B	O	Active low. Buffered chip select for area 6 of SH7760-10 memory. This is the "offboard/PCMCIA1" peripheral chip select area. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
12	uP_PCC_nMCE2B	O	Active low. This is the buffered PCMCIA PC card enable signal for Card Slot B data lines 8 – 15. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor on the processor side of the buffers. Its un-buffered form is also present on J1C pin 42 as uP_MODE1.
13	uP_IOIS16 - WP	I	This signal is used to determine the SRAM mode in conjuncture with uP_MODE1 and uP_MODE2. When uP_IOIS16 is high SRAM bus-width is specified as, (uP_MODE1/uP_MODE0): 0/1 = 8-bit, 1/0 = 16-bit, 1/1 = 32-bit. This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
14	PCC_nIREQ - PCC_RDY	I	This is the PC Card ready signal that comes from the CPLD. For more information, please see the SH7760-10 IO Controller Specification.

Pin #	Signal Name	I/O	Description
15	CPLD_nWAIT - PCC_nWAIT	I	This signal is used to write to the PC Card Status register and is tied to the asynchronous ready signal on the Wired LAN chip. See the SH7760-10 IO Controller Specification for further details. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
16	uP_PCC_BVD2	I	PCMCIA BVD2 signal for the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
17	uP_PCC_BVD1	I	PCMCIA BVD1 signal for the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
18	uP_PCC_nCD2	I	Active low. PCMCIA CD2 signal for the off-board PCMCIA interface. Signals that one side of the PCMCIA card is connected. See the SH7760-10 IO Controller Specification for further details.
19	uP_PCC_nCD1	I	Active low. PCMCIA CD1 signal for the off-board PCMCIA interface. Signals that one side of the PCMCIA card is connected. See the SH7760-10 IO Controller Specification for further details.
20	uP_nMWE0 - DQM0 - PCC_nREG	O	Active low. Buffered write enable for buffered data bus bits 7->0. This is also the DQM0 - PCC_nREG SDRAM signal from the SH7760. Both functions are valid (functionality changes based on memory area accessed). This signal is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
21	DGND	I	Digital Ground (0V)
22	uP_PCC_VS1	I	PCMCIA VS1 signal for the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
23	uP_PCC_VS2	I	PCMCIA VS2 signal for the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
24	uP_PCC_nDRV	O	This is the PCMCIA drive-enable for the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
25		NC	No internal connection (not implemented on the SH7760-10).
26	uP_nMWE3 - DQM3 - PCC_nIOWR	O	Active low. Buffered write enable for buffered data bus bits 31->24. This is also the DQM3 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
27	uP_nMWE2 - DQM2 - PCC_nIORD	O	Active low. Buffered write enable for buffered data bus bits 23->16. This is also the DQM2 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
28	uP_nMWE1 - DQM1 - PCC_nWE	O	Active low. Buffered write enable for buffered data bus bits 15->8. This is also the DQM1 - PCC_nIOWR SDRAM signal from the SH7760. All functions are valid (functionality changes based on memory area accessed).
29	uP_nMWE0 - DQM0 - PCC_nREG	O	Active low. Buffered write enable for buffered data bus bits 7->0. This is also the DQM0 - PCC_nREG SDRAM signal from the SH7760. Both functions are valid (functionality changes based on memory area accessed).
30		NC	No internal connection (not implemented on the SH7760-10).
31		NC	No internal connection (not implemented on the SH7760-10).
32	DGND	I	Digital Ground (0V)
33		NC	No internal connection (not implemented on the SH7760-10).
34	MFP2 - NF_WE	I/O	This signal is the flash Write Enable. It is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
35	MFP3 - NF_OE	I/O	This signal is the flash Output Enable.
36	MFP4 - NF_SC	I/O	This signal is the flash Set Command.

Pin #	Signal Name	I/O	Description
37	MFP5 - NF_CDE	I/O	This signal is the flash Chip Detect Enable. It is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
38	MFP6 - NF_CE	I/O	This signal is the flash Chip Enable. It is pulled up to 3.3V_uP_SDRAM by a 10k resistor.
39	MFP7 – ADTRG#	I/O	This is the SH7760 processor's ADTRG# signal which can be used to start an ADC acquisition cycle which generates an interrupt when the sample is complete.
40		NC	No internal connection (not implemented on the SH7760-10).
41	uP_UARTB_TX	O	SCIF port 3 (UARTB) transmit output signal on the SH7760-10.
42	uP_UARTB_RX	I	SCIF port 3 (UARTB) receive input signal on the SH7760-10.
43	uP_UARTB_CTS	O	SCIF port 3 (UARTB) clear to send on the SH7760-10.
44	DGND	I	Digital Ground (0V)
45	uP_UARTB_RTS	O	SCIF port 3 (UARTB) request to send on the SH7760-10.
46	uP_UARTC_TX	O	SCIF port 1 (UARTC transmit output signal on the SH7760-10.
47	uP_UARTC_RX	I	SCIF port 1 (UARTC) receive input signal on the SH7760-10.
48	MFP9 - uP_UARTC_CLK	I/O	SCIF port 1 (UARTC) serial clock.
49	MFP10 - TIMER/COUNTER0 - PTB4	I/O	This signal is one of four 16-bit timer/counters with count enable. When the counter is not being used this signal can also be used as GPIO PTB4.
50	MFP11 - TIMER/COUNTER1 - PTB3	I/O	This signal is one of four 16-bit timer/counters with count enable. When the counter is not being used this signal can also be used as GPIO PTB3.
51	MFP12 - TIMER/COUNTER2 - PTB2	I/O	This signal is one of four 16-bit timer/counters with count enable. When the counter is not being used this signal can also be used as GPIO PTB2.
52	MFP13 - TIMER/COUNTER3 - PTB1	I/O	This signal is one of four 16-bit timer/counters with count enable. When the counter is not being used this signal can also be used as GPIO PTB1.
53	MFP14 - uP_UARTB_BAUDCLKOUT	I/O	SCIF port 3 (UARTB) serial clock.
54	MFP15 - uP_UARTA_CLK	I/O	SCIF port 2 (UARTA) serial clock.
55	DGND	I	Digital Ground (0V)
56	MFP16 - CAN1_TX	I/O	CAN (Controller Area Network) bus transmit signal of channel 1.
57	MFP17 - CAN1_RX	I/O	CAN (Controller Area Network) bus receive signal of channel 1.
58	MFP18 - CAN1_NERR	I/O	CAN (Controller Area Network) bus error of channel 0.
59	MFP19 - CAN0_TX	I/O	CAN (Controller Area Network) bus transmit signal of channel 0.
60	MFP20 – uP_nMCS5 – PCC_nMCE1A	I/O	Active low. This is the buffered PCMCIA slot A card enable signal for data lines 0 – 7, or the Area 5 chip select signal – depending on how the processor is configured.
61	MFP21 - CAN0_NERR	I/O	CAN (Controller Area Network) bus error of channel 0.
62	MFP22 - uP_PCC_nMCE2A	I/O	Active low. This is the buffered PCMCIA slot A card enable signal for data lines 8 – 15. This signal has a 10k pull-up resistor on the processor side of the bus and signal buffers.
63	MFP23 - uP_I2C0_SDA	I/O	This is the I2C channel 0 serial data signal.
64	MFP24 - uP_I2C1_SCL	I/O	This signal is the I2C channel 1 serial clock.
65	MFP25 - uP_I2C1_SDA	I/O	This is the I2C channel 0 serial data signal.
66	DGND	I	Digital Ground (0V)
67	MFP26 - PCC_nINPACK	I/O	This signal is used in the CPLD to register the PCC_nINPACK signal of the off-board PCMCIA interface. See the SH7760-10 IO Controller Specification for further details.
68	MFP27 - uP_CANO_RX	I/O	CAN (Controller Area Network) bus receive signal of channel 0.

Pin #	Signal Name	I/O	Description
69	MFP28 - uP_I2CO_SCL	I/O	This signal is the I2C channel 0 serial clock.
70	MFP29 – uP_CKE	I/O	This signal is the clock enable signal for use in controlling the state of external SDRAM expansion memory.
71	MFP30 - SSIO_SCK - AC97_SD_IN0 - nBS2	I/O	This signal can be used as the Serial Sound Interface word selection or sync output for the Hitachi Audio CODEC channel 0.
72	MFP31 – VIDEO_nMCS	O	Active low. This is the buffered chip select signal for Area 2 of memory. Area 2 of memory is capable of controlling SDRAM memory.
73	MFP32 - A/D5	I/O	Analog input into touch screen controller: 0 to 3.3V swing possible. This signal has a 10000 pF bypass capacitor installed on the Card Engine.
74	MFP33 - A/D6	I/O	Analog input into touch screen controller: 0 to 3.3V swing possible. This signal has a 10000 pF bypass capacitor installed on the Card Engine.
75	MFP34 - MONO_OUT	I/O	The signal is the main mono output from the AC97 CODEC.
76	MFP35 - PC_BEEP	I/O	This is an analog input to the AC97 CODEC, typically used for PCBEEP signal.
77	DGND	I	Digital Ground (0V)
78	MFP36 - CD_IN_L	I/O	This is an analog input to the AC97 CODEC, typically used for CD line-in left signal.
79	MFP37 - CD_IN_R	I/O	This is an analog input to the AC97 CODEC, typically used for CD line-in right signal.
80	MFP38 - CD_GND	I/O	This signal is the CD input common mode reference (ground) to the AC97 CODEC.

5.4 Multiplexed Signal Trade-Offs

5.4.1 144-Pin SODIMM (J1C) Connector Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 144-pin SODIMM connector (J1C) on the SH7760-10 Card Engine (if any).

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
39	uP_UARTA_RTS	SCIF1_RTS	UARTA RTS	PTG2	Port G bit 2 I/O
41	uP_UARTA_CTS	SCIF1_CTS	UARTA CTS	PTG3	Port G bit 3 I/O
42	uP_MODE1 – uP_PCC_nCE2B	MD4	Mode 4	CE2B	PC Card Enable
43	uP_UARTA_TX	SCIF1_TXD	UARTA Transmit	PTG0	Port G bit 0 I/O
44	uP_MODE0 - uP_PCC_nCE2A	MD3	Mode 3	CE2A	PC Card Enable
45	uP_UARTA_RX	SCIF1_RXD	UARTA Receive	PTG1	Port G bit 1 I/O
65	uP_SPI_FRM	HSPI_CS	SPI Chip Select	PTF0	Port F bit 0 I/O
67	uP_SPI_MOSI_TX	HSPI_TX	SPI Transmit	PTF3	Port F bit 3 I/O
69	uP_SPI_MOSI_RX	HSPI_RX	SPI Receive	PTF2	Port F bit 2 I/O
71	uP_SPI_SCK	HSPI_CLK	SPI Clock	PTF1	Port F bit 1 I/O
72	uP_nRD - nCAS	nRD	Read	nCAS	Column Addressing Strobe
74	uP_nMWE3 - DQM3 - PCC_nIOWR	nWE3	Buffered write enable for data bus 31->24	DQM3 or PCC_nIOWR	DRAM selection signal or PCMCIA interface signal
76	uP_nMWE2 - DQM2 - PCC_nIORD	nWE2	Buffered write enable for data bus 23->16	DQM2 or PCC_nIORD	DRAM selection signal or PCMCIA interface signal
78	uP_nMWE1 - DQM1 - PCC_nWE	nWE1	Buffered write enable for data bus 15->8	DQM1 or PCC_nWE	DRAM selection signal or PCMCIA interface signal
80	uP_nMWE0 - DQM0 - PCC_nREG	nWE0	Buffered write enable for data bus 7->0	DQM0 or PCC_nREG	DRAM selection signal or PCMCIA interface signal
84	uP_nMRD - PCC_nOE	nMRD	Buffered read signal	PCC_nOE	PCMCIA Output Enable

5.4.2 80-Pin Expansion Connector A (J1A) Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 80-pin expansion connector A (J1A) on the SH7760-10 Card Engine.

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1	LCD_VSYNC	LCD_FLM	First line marker	MFI-RW or PTE2	MFI-read/write or Port E bit 2 I/O
2	LCD_HSYNC	LCD_CL1	LCDC Shift Clock 1	MFI-E or PTE5	MFI enable or Port E bit 5 I/O
3	LCD_DCLK	LCD_CL2	LCDC Shift Clock 2	MFI-MD or PTE4	MFI mode or Port E bit 4 I/O
4	LCD_DON	LCD_DON	LCDC display-on	MFI-CS or PTE6	MFI chip select or Port E bit 6 I/O
5	LCD_MDISP	LCD_MDISP	DISP Signal	MFI-RS or PTE3	MFI register select or Port E bit 3 I/O
6	LCD_VEEEN	VEPWC	LCD power (VEE)	IRQ5 or PTE0	Interrupt Request 5 or Port E bit 0 I/O

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
7	LCD_VDDEN	VCPWC	LCD power (VCC)	IRQ4 or PTE1	Interrupt Request 4 or Port E bit 1 I/O
19	uP_AC97_BITCLK1	HAC_BIT_CLK1	AC97 Bit Clock	PTJ2	Port J bit 2 I/O
20	uP_AC97_RESET	HAC_RES	AC97 Reset	PTJ6	Port J bit 6 I/O
21	uP_AC97_SYNC1	HAC_SYNC1	Sync output	PTJ5	Port J bit 5 I/O
22	uP_AC97_SD_IN1	HAC_SD_IN1	AC97 output	PTJ4	Port J bit 4 I/O
23	uP_AC97_SD_OUT1	HAC_SD_OUT1	AC97 input	PTJ3	Port J bit 3 I/O
42	R1	LCD_DATA11	LCD DATA 11 I/O	MFI-D11 or PTD4	MFI Data or Port D bit 4 I/O
43	R2	LCD_DATA12	LCD DATA 12 I/O	MFI-D12 or PTD3	MFI Data or Port D bit 3 I/O
45	R3	LCD_DATA13	LCD DATA 13 I/O	MFI-D13 or PTD2	MFI Data or Port D bit 2 I/O
46	R4	LCD_DATA14	LCD DATA 14 I/O	MFI-D14 or PTD1	MFI Data or Port D bit 1 I/O
47	R5	LCD_DATA15	LCD DATA 15 I/O	MFI-D15 or PTD0	MFI Data or Port D bit 0 I/O
48	G0	LCD_DATA5	LCD DATA 5 I/O	MFI-D5 or PTC2	MFI Data or Port C bit 2 I/O
49	G1	LCD_DATA6	LCD DATA 6 I/O	MFI-D6 or PTC1	MFI Data or Port C bit 1 I/O
50	G2	LCD_DATA7	LCD DATA 7 I/O	MFI-D7 or PTC0	MFI Data or Port C bit 0 I/O
51	G3	LCD_DATA8	LCD DATA 8 I/O	MFI-D8 or PTD7	MFI Data or Port D bit 7 I/O
52	G4	LCD_DATA9	LCD DATA 9 I/O	MFI-D9 or PTD6	MFI Data or Port D bit 6 I/O
53	G5	LCD_DATA10	LCD DATA 10 I/O	MFI-D10 or PTD5	MFI Data or Port D bit 5 I/O
56	B1	LCD_DATA0	LCD DATA 0 I/O	MFI-D0 or PTC7	MFI Data or Port C bit 7 I/O
57	B2	LCD_DATA1	LCD DATA 1 I/O	MFI-D1 or PTC6	MFI Data or Port C bit 6 I/O
58	B3	LCD_DATA2	LCD DATA 2 I/O	MFI-D2 or PTC5	MFI Data or Port C bit 5 I/O
59	B4	LCD_DATA3	LCD DATA 3 I/O	MFI-D3 or PTC4	MFI Data or Port C bit 4 I/O
60	B5	LCD_DATA4	LCD DATA 4 I/O	MFI-D4 or PTC3	MFI Data or Port C bit 3 I/O
65	uP_USB2_nOVR_CRNT	USB_OVC#	USB Over Current	PTH0	Port H bit 0 I/O
68	uP_USB2_PWR_EN	USB_PENC	USB Power Enable	PTH1	Port H bit 1 I/O

5.4.3 80-Pin Expansion Connector B (J1B) Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 80-pin expansion connector B (J1B) on the SH7760-10 Card Engine.

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
5	uP_nMRD – PCC_nOE	nMRD	Buffered read signal	PCC_nOE	flash output enable
6	uP_nMWE1 – DQM1 – PCC_nWE	nWE1	Buffered write enable for data bus 15->8	DQM1 or PCC_nWE	DRAM selection signal or PCMCIA interface signal
7	uP_nMWE2 – DQM2 – PCC_nIORD	nWE2	Buffered write enable for data bus 23->16	DQM2 or PCC_nIORD	DRAM selection signal or PCMCIA interface signal
8	uP_nMWE3 – DQM3 – PCC_nIOWR	nWE3	Buffered write enable for data bus 31->24	DQM3 or PCC_nIOWR	DRAM selection signal or PCMCIA interface signal
34	MFP2 – NF_WE	NF_WE	flash Write Enable	PTK5	Port K bit 5 I/O
35	MFP3 – NF_OE	NF_OE	flash Output Enable	PTK4	Port K bit 4 I/O
36	MFP4 – NF_SC	NF_SC	flash set command	PTK3	Port K bit 3 I/O
37	MFP5 – NF_CDE	NF_CDE	flash Chip Detect Enable	PTK6	Port K bit 6 I/O
38	MFP6 – NF_CE	NF_CE	flash Chip Enable	PTK7	Port K bit 7 I/O

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
39	MFP7– ADTRG#	ADTRG#	ADTRG# signal	PTK2	Port K bit 2 I/O
41	uP_UARTB_TX	SCIF2_TXD	UARTB Transmit	PTH3	Port H bit 3 I/O
42	uP_UARTB_RX	SCIF2_RXD	UARTB Receive	PTH4	Port H bit 4 I/O
43	uP_UARTB_CTS	SCIF2_CTS	UARTB Clear To Send	PTH6	Port H bit 6 I/O
45	uP_UARTB_RTS	SCIF2_RTS	UARTB Ready To Send	PTH5	Port H bit 5 I/O
46	uP_UARTC_TX	SCIF0_TXD	UARTC Transmit	PTG5	Port G bit 5 I/O
47	uP_UARTC_RX	SCIF0_RXD	UARTC Receive	PTG6	Port G bit 6 I/O
48	MFP9 - uP_UARTC_CLK	SCIF0_CLK	UARTC Clock	PTG7	Port G bit 7 I/O
49	MFP10 - TIMER/COUNTER0 - PTB4	CMT_CTR0	Counter 0	PTB4	Port B bit 4 I/O
50	MFP11 - TIMER/COUNTER1 - PTB3	CMT_CTR1	Counter 1	PTB3	Port B bit 3 I/O
51	MFP12 - TIMER/COUNTER2 - PTB2	CMT_CTR2	Counter 2	PTB2	Port B bit 2 I/O
52	MFP13 - TIMER/COUNTER3 - PTB1	CMT_CTR3	Counter 3	PTB1	Port B bit 1 I/O
53	MFP14 - uP_UARTB_BAUDCLKOUT	SCIF2_CLK	UARTB clock	PTH7	Port H bit 7 I/O
54	MFP15 - uP_UARTA_CLK	SCIF1_CLK	UARTA clock	PTG4	Port G bit 4 I/O
56	MFP16 - CAN1_TX	CAN1_TX	CAN1 Transmit	PTA2	Port A bit 2 I/O
57	MFP17 - CAN1_RX	CAN1_RX	CAN1 Receive	PTA3	Port A bit 3 I/O
58	MFP18 - CAN1_NERR	CAN1_NERR	CAN1 Error	PTA4	Port A bit 4 I/O
59	MFP19 - CAN0_TX	CAN0_TX	CAN0 Transmit	PTA5	Port A bit 5 I/O
60	MFP20 - uP_NMCS5 - PCC_nMCE1A	PCC_nMCE1A	PCMCIA Slot A enable 1	CS 5	Chip Select 5
61	MFP21 - CAN0_NERR	CAN0_NERR	CAN0 Error	PTA7	Port A bit 7 I/O
68	MFP27 - CAN0_RX	CAN0_RX	CAN0 Receive	PTA6	Port A bit 6 I/O
71	MFP30 - SSIO_SCK - AC97_SD_IN0 - nBS2	SSI_SCK	SSI Serial Clock input	PTB7 or HAC_SD_IN0 or nBS2	Port B bit 7 I/O or Hitachi Audio CODEC serial data 0 input or bus start 2

6 Mechanical Specifications

6.1 Interface Connectors

The SH7760-10 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B). The 80-pin expansion connectors must have a 3mm board-to-board mating height, and the SODIMM must have a 3.7mm mating height (2.9mm board-to-board).

IMPORTANT NOTE: Do not place any components underneath the Card Engine on the same side of the board as the connectors. Some components on the Card Engine take advantage of the full mating height and their locations are subject to change as the board is revised. If the design requires that components be placed underneath the Card Engine, contact Logic Product Development for assistance.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

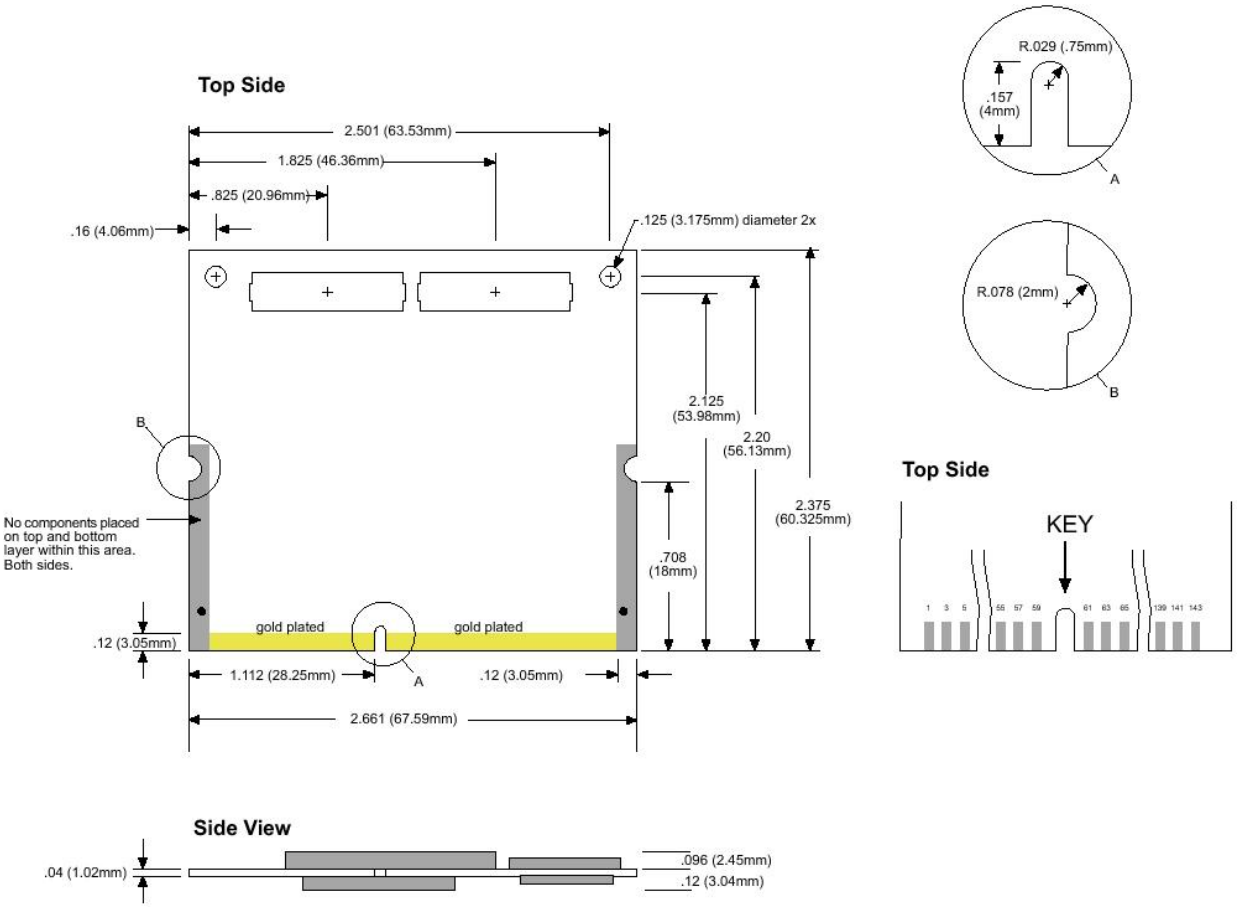


Figure 6.1: Card Engine Mechanical Drawing

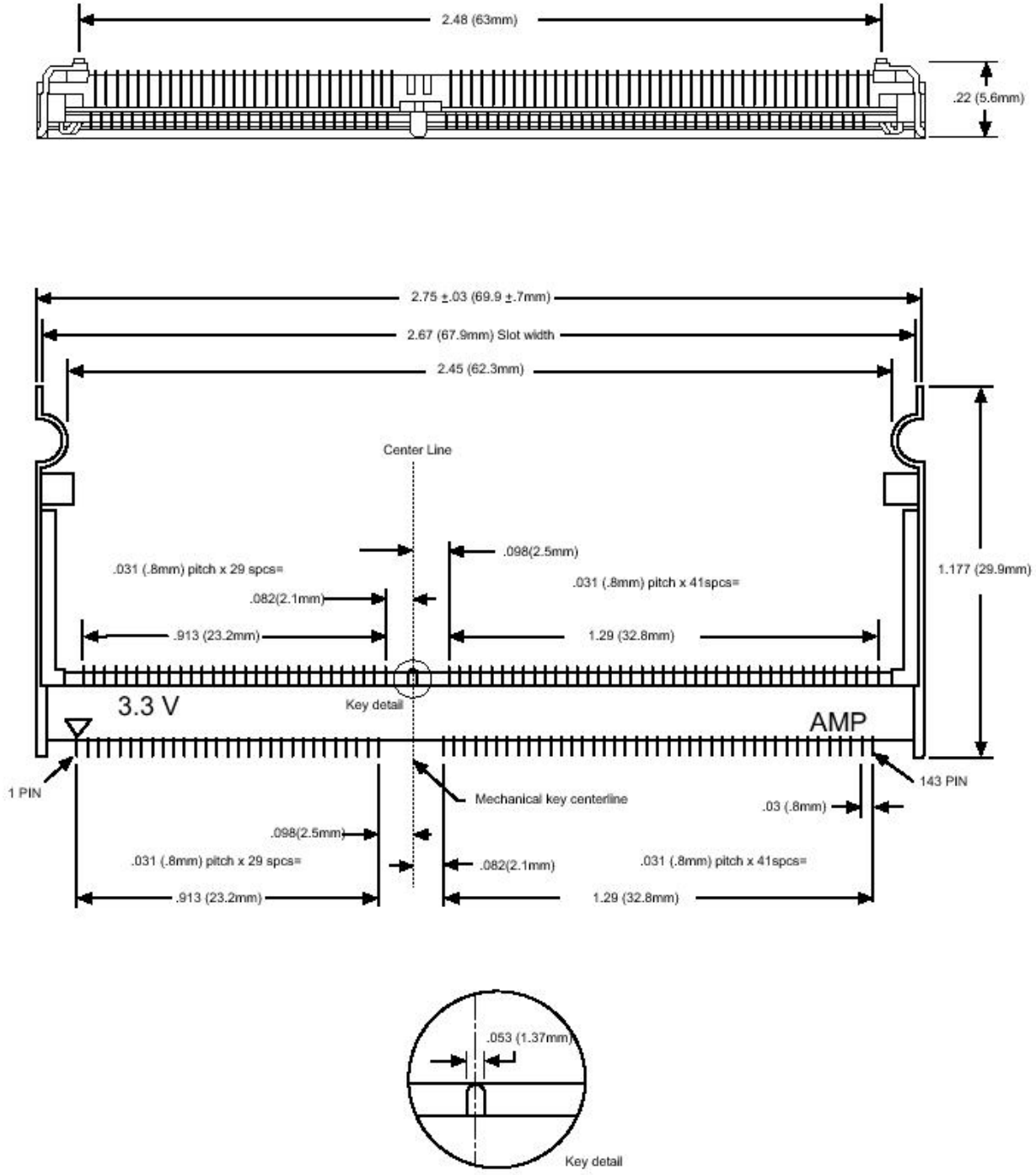


Figure 6.2: SODIMM Connector Specification

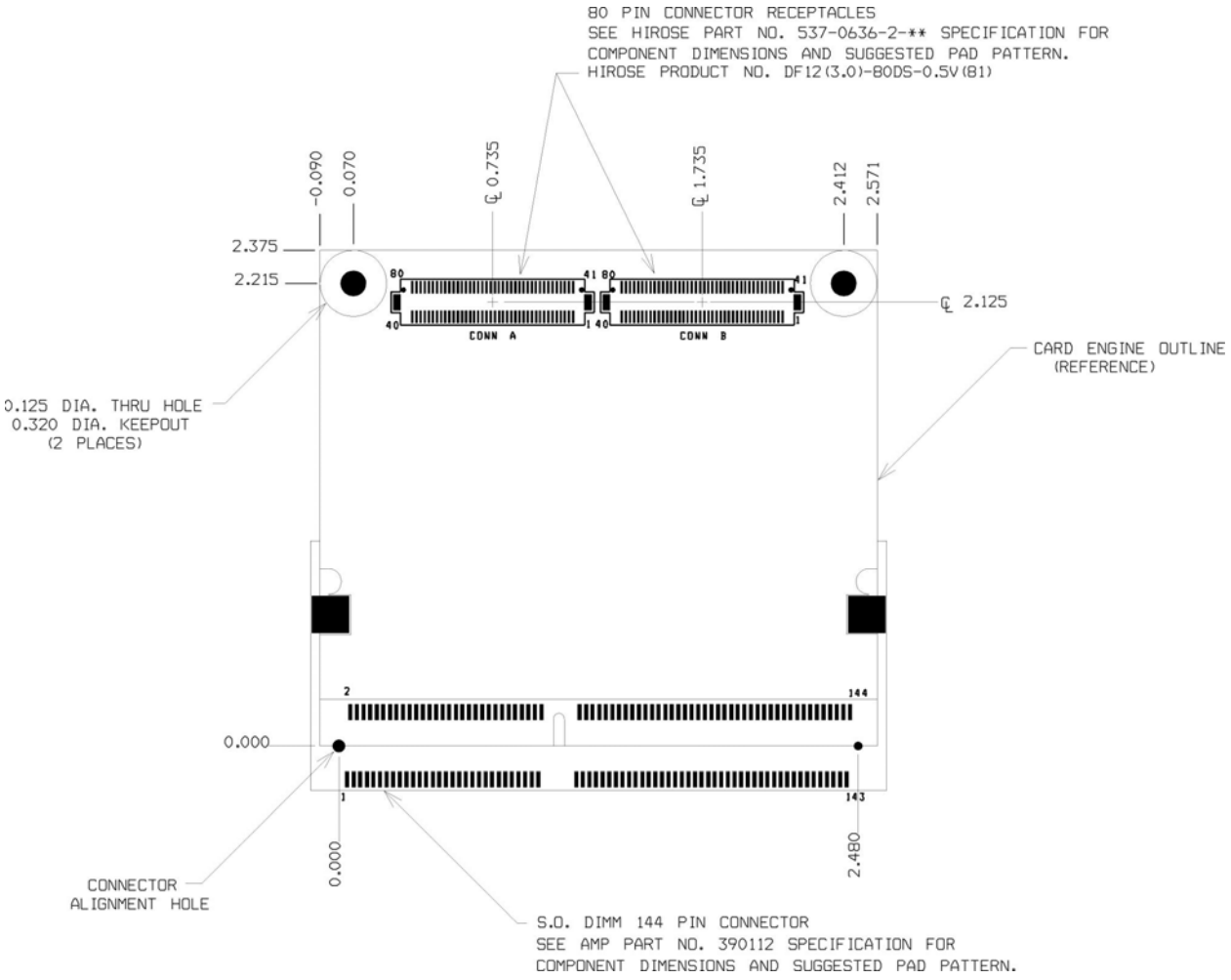


Figure 6.3: Recommended PCB Layout

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