SH7727-20
Card Engine

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Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
1	Hans Rempel	First Draft Version	HAR	02/23//03
2	Hans Rempel	Preliminary Release	HAR	03/03/03
A	Hans Rempel	Initial Release	HAR	04/01/03
B	Hans Rempel	Grammar and tech edit, SDK release	HAR	08/18/03
C	James Wicks	Editing, Updating Figures	JW	09/17/03
D	James Wicks	Added mode line description note	JW	09/19/03
E	James Wicks	J1B Pin Correction, edit	HAR	12/06/04
F	Jed Anderson	Updated Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes	JCA	11/08/06

Please check www.logicpd.com for the latest revision of this manual, errata's, and additional application notes.

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SH7727 CARD ENGINE

CARD ENGINE ADVANTAGE

- Reduce TIme to Market
  → 6 to 9 month savings
- Product-Ready Hardware Platform
- Production Quality Software
- Engineering Support

PRODUCT HIGHLIGHTS

- Ready-to-Run Windows® CE BSP
- Bootloader/Monitor
- Custom Windows CE device driver development

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

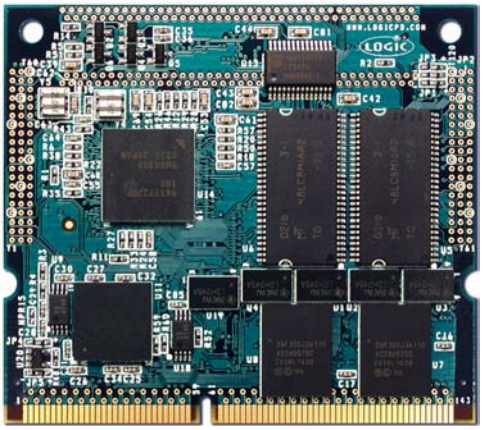
For more information on our Embedded Product Solutions, please contact Logic Sales at product.sales@logicpd.com or 612.672.9495.

RENESAS

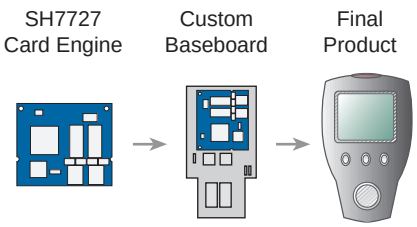
Microsoft® Windows® Embedded Partner
Gold-level Member

The SH7727 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The SH7727 Card Engine is a complete System on Module (SOM) offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. The use of custom baseboards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation microcontroller Card Engines when new funtionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Renesas SH7727 SH-3 DSP 32-bit RISC Microprocessor running at 156 MHz
- **SDRAM Memory** Up to 64 Mbytes
- **Flash Memory** Up to 32 Mbytes on board
- **Display** Programmable color LCD controller
  - Built in driver supports up to 1024 x 768 x 8-bit color or 800 x 600 x 16-bit color
  - Supports TFT, STN, Color STN, DSTN
- **Touch Screen** Four wire resistive touch controller
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN 91C111 (MAC & PHY)
- **Audio** Audio codec stereo (Phillips UDA1345TS)
- **PC Card Expansion**
  - CompactFlash Type 1 card (memory-mode only)
  - Smart Card Interface (ISO7816)
  - PCMCIA of CF (2 slots)
  - MMC*
- **USB** USB 1.1 Two Host or One Host and One Client
- **Serial Ports** 16C550-like, standard UART (supports RXD, TXD, RTS, and CTS signals only)
- **GPIO** Programmable depending on peripheral requirements
- **SPI**
- **Software**
  - Windows™ CE and Linux BSPs available
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37" (60.2 mm) long x 2.67" (67.8 mm) wide x 0.20" (5.1 mm) high
  - 144-pin SODIMM connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit

** Not supported by standard Windows CE BSP*

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PN: 70000034 Rev E

1.2 Acronyms

ADC	Analog to Digital Converter
AHB	Advanced Hardware Bus
BSP	Board Support Package
CODEC	Coder Decoder
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
ENDEC	Encoder Decoder
ESD	Electro Static Discharge
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
IO	Input Output
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LOLO	LogicLoader™
NC	No Connect
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

SH7727-20 IO Controller Specification
Renesas SuperH RISC Engine SH7727 Hardware Manual
Altera MAX 7000A CPLD data sheet (EPM7128A)
Altera Device Package Information data sheet
Altera Ordering Information
Philips UDA1345 Economy Audio CODEC Data Sheet

1.4 Card Engine Advantages

Logic's Card Engines accelerate your products time to market. In addition, the Card Engines provide the following advantages:

- **Product ready hardware & software** solutions allow immediate application development that results in embedded product development cycle with less time, less cost, less risk, with more innovation.
  - Less time – time to market solution allows software application development to begin immediately

- Less cost – significantly lowers development cost
- Less risk – complex portion of design product ready
- More Innovation – Allows you to focus on your IP

- **Common Card Engine footprint** (See Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- **Low cost hardware solution** – Custom configurations to meet your design requirements and price points.
- Complex portion of the design ready to go

1.5 Card Engine Interface

The Card Engine's common interface allows you to easily migrate to new processors and technology. Logic is in constant research and development of new technologies to improve performance, lower cost and increase feature capabilities. By using the common footprint, you can leverage Logic's work without having to re-spin your product. Contact Logic sales for more information.

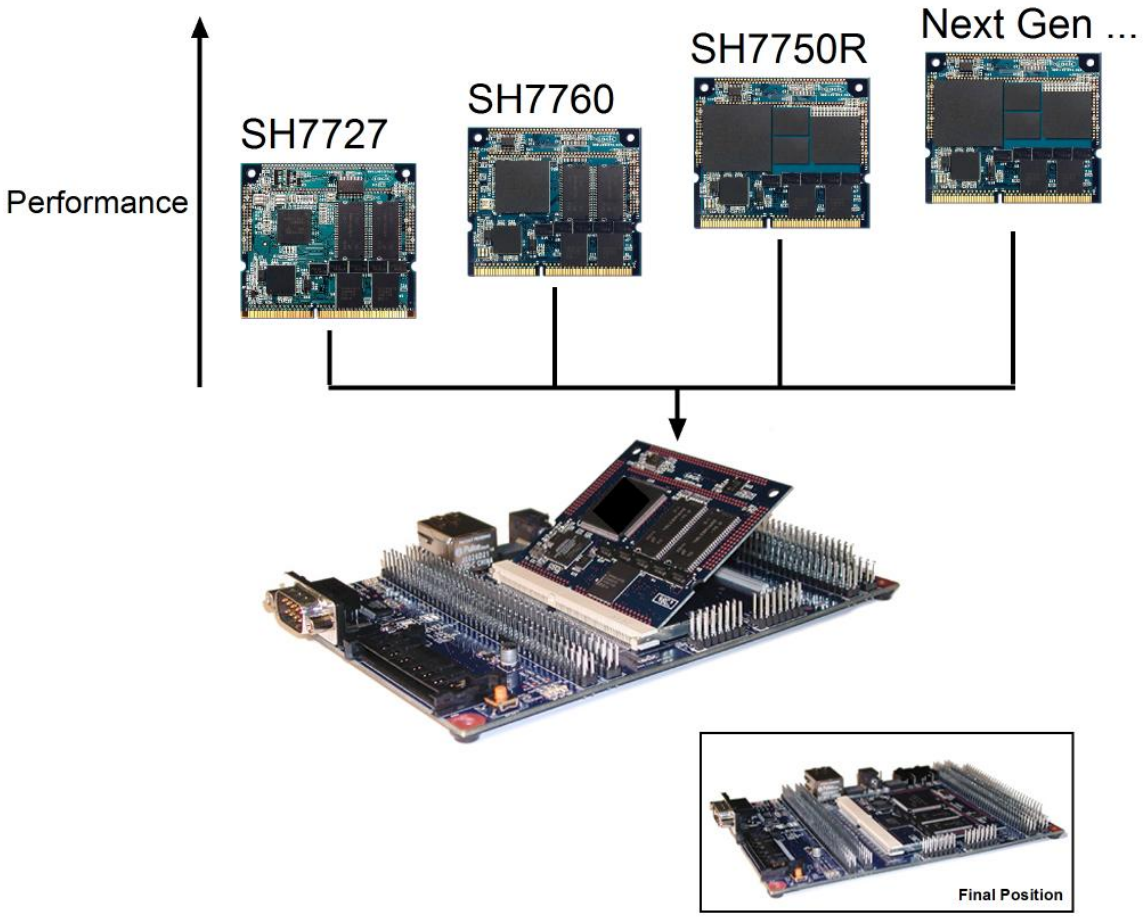


Figure 1.1: Card Engine Advantages

Encapsulating a significant amount of your design onto the Card Engine reduces risk of obsolescence issues. If a component on the Card Engine design becomes obsolete you don't have to re-spin your board, Logic will design for alternative part that is transparent to your product. Manufacturing also becomes much easier. Card Engines are delivered to you fully tested, making your manufacturing process simpler and less costly.

1.6 SH7727-20 Card Engine Block Diagram

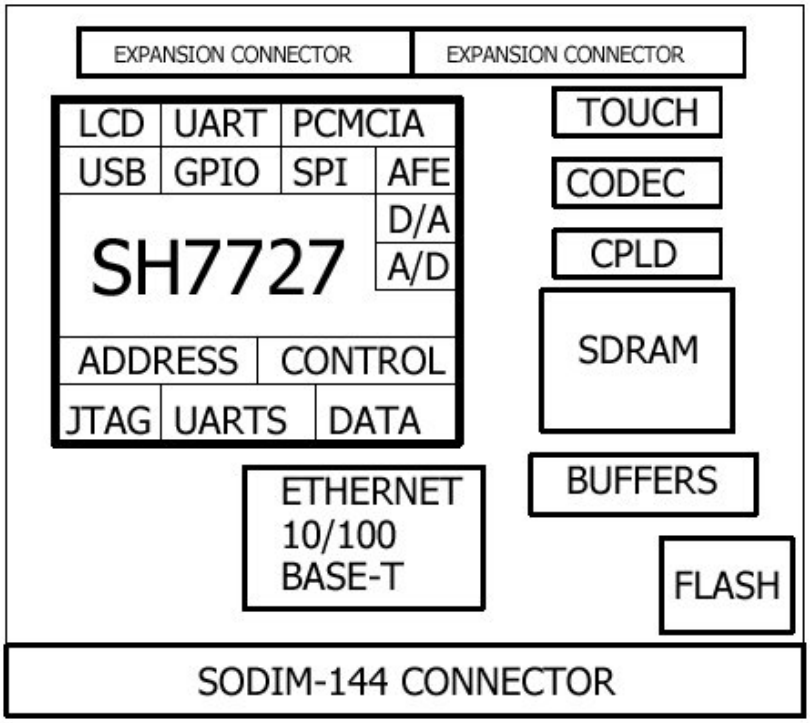


Figure 1.2: SH7727-20 Card Engine Block Diagram

1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
DC IO and Peripheral Supply Voltage (VIO)	3.3V, 3.3V_uP_SDRAM	-0.3 to 4.2	V
DC Core Supply Voltage	VCORE	-0.3 to 2.5	V
Analog Supply Voltage	3.3VA	-0.3 to 4.6	V
Positive Voltage on any pin, with respect to DC IO and Peripheral Supply Voltage		VIO + 0.3	V
Negative Voltage on any pin, with respect to DGND		-0.3	V
Operating Temperature Range[2]	Topr	0 to 75	°C
Storage Temperature Range	Tstr	-55 to 125	°C

1 - These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.
2 - Contact Logic for extended operating temperature range options

1.7.2 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	TBD	392	TBD	mA	
DC IO Supply Standby Current	TBD	TBD	TBD	mA	4
DC IO Supply Sleep Current	TBD	TBD	TBD	mA	4
DC Core Supply Voltage	1.77	1.90	2.05	V	1
DC Core Supply Active Current	TBD	330	650	mA	
DC Core Supply Standby Current	TBD	30	TBD	mA	
DC Core Supply Sleep Current	TBD	50	TBD	mA	
Commercial Operating Temperature	0	25	70	°C	
Extended Operating Temperature	-20	25	75	°C	2
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	3
Connector Insertion/removal		50		Cycles	
Input signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.4		VIO	V	
Output Signal Low Voltage	DGND		0.55	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. Contact Logic for more information on an extended temperature LSH7727-20 Card Engine
3. May vary depending on Card Engine configuration.
4. Typical operating current will vary in sleep and standby mode depending on the software configuration. The SH7727 processor hw manual specifies that it will draw no more from the IO rail (3.3V) than 50mA while in sleep and 30 micro-amps while in standby.

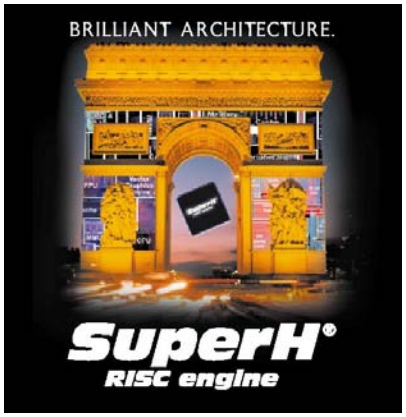
2 Electrical Specification

2.1 Microprocessor

2.1.1 SH7727 Microprocessor

The SH7727-20 Card Engine uses Renesas's highly integrated system on a chip SH7727 microprocessor. Renesas's SH7727 has a 32-bit SH-3 RISC core with a DSP core extension. Renesas's SH7727 microprocessor is a system on a chip providing many integrated on-chip peripherals including:

- Integrated SuperH SH-3 Core
  - 32 bit RISC-type SuperH RISC Engine CPU
  - DSP core extension
  - 16 KB mixed data/instruction cache
  - MMU
  - 4 GB logical address space
  - 5 stage pipeline
- 16 KB on-chip X/Y RAM
- Integrated LCD Controller
  - Up to 1024 x 768 Resolution
  - Supports STN, DSTN, TFT
  - 16 bit color
  - 2.4 KB line buffer
  - Up to QVGA hardware rotation
- UART (SCIF)
  - 16 byte tx/rx FIFO
  - RTS/CTS hardware flow control
- SSP (SCI)
- SIOF
  - I^2S audio support
- PC card controller
  - PCMCIA Rev 2.1/JEIDA v.4.2
- USB Host
  - USB Rev 1.1
  - OHCI Rev 1.0
- USB Function
  - USB Rev 1.1
- AFE Interface
  - 128 byte tx/rx FIFO
- 13 8-bit I/O ports (multiplexed)
- 10 bit ADC
- 8 bit DAC
- Four DMA Channels (1 External)
- Three Counter/Timers
- RTC
- Low Power Modes



IMPORTANT NOTE: See the Renesas website for the "Renesas SuperH RISC Engine SH7727 Hardware Manual" as well as errata at http://www.renesas.com/eng/

2.1.2 SH7727 Microprocessor Block Diagram

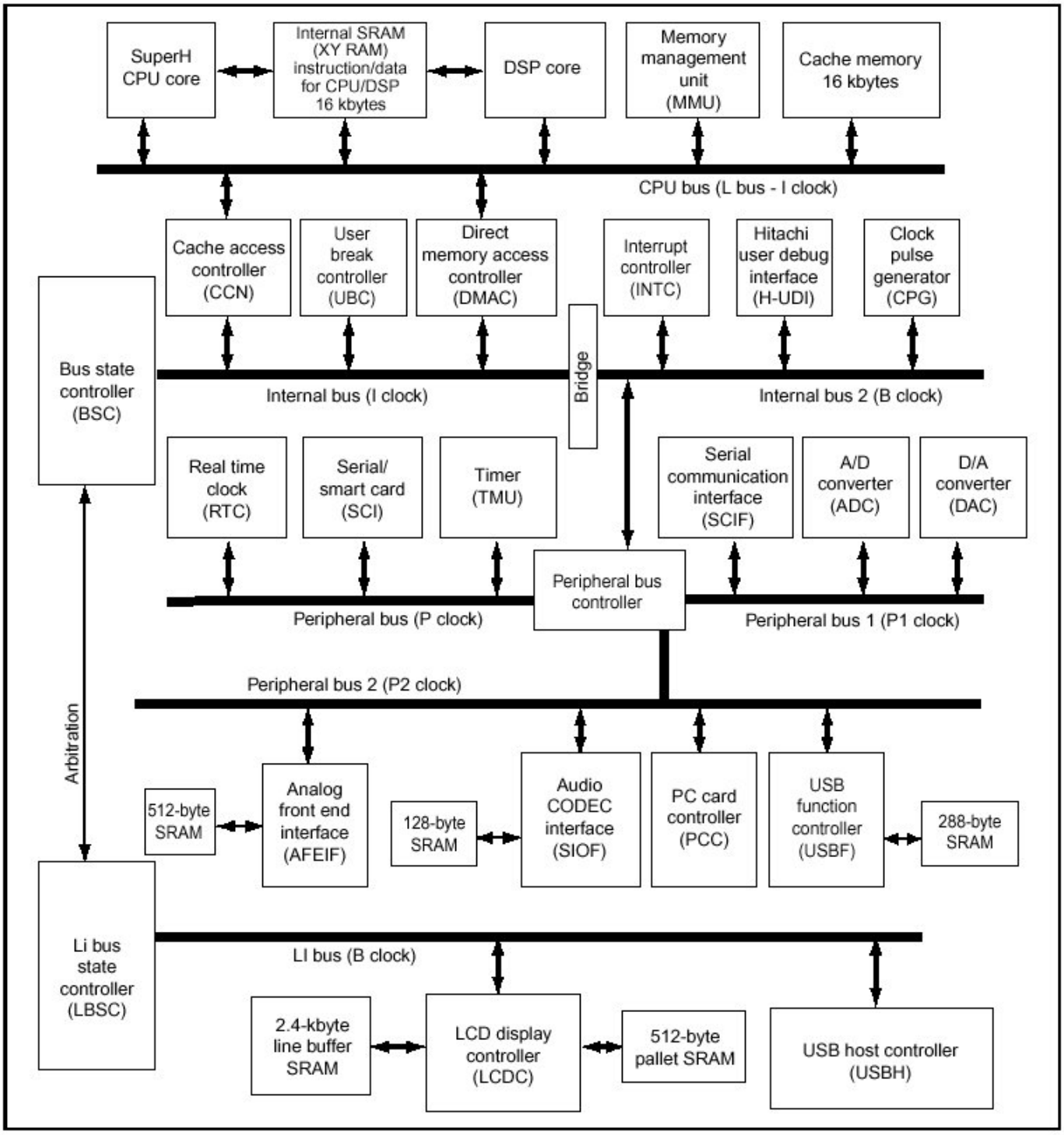


Figure 2.1: SH7727 Microprocessor Block Diagram

2.2 Clocks

The SH7727 microprocessor has a sophisticated clocking architecture and can be software programmable tailored to an application to vary the microprocessor performance, power consumption, and bus throughput. See the “Renesas SuperH RISC Engine SH7727 Hardware Manual “ for more details.

The SH7727-20 Card Engine puts the SH7727 into its “Clock Mode 2”, which turns on the on-chip oscillator and has an input crystal range of 6 to 16.67 MHz. The Card Engine uses a 12.9 MHz crystal as the input clock. Internally, the SH7727 processor uses two PLL circuits to multiply the clock frequency to the desired level as well as to phase align all clocks with CKIO. There are three main clocks that are generated from the input clock: CPU clock, bus clock and peripheral clock.

The 32.768 kHz crystal is used for the RTC interface.

The bootloader and standard software BSPs initialize the clock frequencies to an input crystal multiplier of 12:4:2 for CPU:BUS:PERIPHERAL clocks respectively. This sets the SH7727 microprocessor’s core clock speed to 154.8 MHz (12 x 12.9 MHz), the bus speed to 51.6 MHz (4 x 12.9 MHz) and the peripheral clock speed to 25.8 MHz (2 x 12.9 MHz). Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate. The specific 12:4:2 clocking ratio was chosen to optimize CPU performance with bus clock speed and common serial port baud rates.

IMPORTANT NOTE: The specific clocking scheme is dependent upon the software configuration of the FRQCR register. Depending on the software being used, the specific clock divisors may be different that the described 12:4:2 setup.

The SH7727-20 Card Engine provides two external bus clocks: uP_BUS_CLK and uP_AUX_CLK, on the 144-pin SO-DIMM connector. Both clocks are generated at a default of 51.6 MHz and are in-phase with each other. The clock signal uP_BUS_CLK is used internally to the Card Engine and should only be used externally as a temporary design reference with an oscilloscope or logic analyzer. The uP_AUX_CLK signal is not used internally to the Card Engine and may be connected to up to 50 pF of external loading before it must be buffered for extended fan-out. Logic suggests connecting no more than three external loads to uP_AUX_CLK.

SH7727 Microprocessor Signal Name	SH7727-20 Card Engine Net Name	Default Software Value in Bootloader and Software BSP’s
CPU-CLOCK	NA	154.8 MHz
P-CLOCK	NA	25.8 MHz
CKIO	uP_BUS_CLK	51.6 MHz
CKIO2	uP_AUX_CLK	51.6 MHz

2.3 Memory

2.3.1 Synchronous DRAM

The SH7727-20 Card Engine uses a 32-bit memory bus to interface to Synchronous DRAM. The memory density can be configured as 16, 32 or 64 MBytes to meet the user’s memory requirements and cost constraints. The default Card Engine memory configuration is a 32 MByte configuration.

If the user requirements exceed 64MBytes of SDRAM memory, it may be possible to add additional SDRAM. The signal VIDEO_nMCS, while typically used for an external graphics

controller, may alternatively be used as a second SDRAM memory area supporting up to an additional 64 MBytes of SDRAM memory. This can bring the total SDRAM memory density for a design up to a maximum of 128 MBytes.

IMPORTANT NOTE: The external SDRAM interface has not been tested and depends highly upon the custom daughter board design. Please contact Logic for assistance if requiring more that 64MBytes of SDRAM on your design.

The SDRAM interface signals on the external connectors are: uP_nMWE0-uP_nDQM1, uP_nMWE1-uP_PCC_nWE-uP_nDQM1, uP_nMWE2-uP_PCC_nIORD-uP_nDQM2, uP_nMWE3-uP_PCC_nIOWR-uP_nDQM3, uP_nRAS, uP_nCAS and uP_nMWR. The uP_AUX_CLK signal may be used for the SDRAM clock, and the VIDEO_nMCS signal may be used for the SDRAM chip select (if configured correctly).

Please see the Memory Map section of this manual for more information.

2.3.2 Direct Memory Access (DMA)

The Renesas SH7727 microprocessor has three internal DMA channels and 1 external DMA channel.

The SH7727 microprocessor multiplexes the external DMA control lines with the built-in PCMCIA controller functionality. Therefore, if the design utilizes the built-in PCMCIA peripheral in the full control line support mode, it is not possible to use the external DMA channel. Logic's standard BSPs currently implement the PCMCIA controller in the full control line support mode. See the PCMCIA entry in this section for a more complete description.

The standard SH7727-20 Card Engine uses the internal DMA channel 2 for audio recording and internal DMA channel 3 for audio playback. DMA channel 0 is unused and can accept requests from either internal peripherals or external sources. DMA channel 1 is unused and can accept requests only from internal peripherals.

The external DMA channel's (channel 0) interface signals on the external connectors are: uP_DREQ0, uP_DRAK0-uP_PCC_RESET and uP_DACK0-uP_PCC_nDRV.

If an external DMA channel is required, please contact Logic Product Development for assistance.

2.3.3 NOR Flash

The SH7727-20 Card Engine uses a 32-bit memory bus to interface to Intel Strataflash memory. The on-board Card Engine memory can be configured as 8, 16, or 32 MBytes to meet the user's FLASH requirements and cost constraints. A user should consult Logic when specifying flash size because it is one of the most expensive components in the SH7727-20 Card Engine.

A user can expand their non-volatile storage capability using the SH7727-20 Card Engine reference designs as a design guide. User's can expand their non-volatile storage capability by implementing additional external memory such as CompactFlash, NAND, or additional NOR flash memory. See Logic's reference designs for information (Zoom™ Starter Kit, Zoom™ Integrated Development Kit – Q4/03, LSH7727-10 Application Kit), or contact Logic for additional assistance on peripheral interfaces.

2.3.4 CompactFlash (memory-mapped mode only)

Although the SH7727-20 microprocessor has an on-chip integrated PCMCIA/CompactFlash controller, the Card Engine has also been designed to support an additional memory-only CF card. The SH7727-20 Card Engine provides the necessary signals to directly connect a CompactFlash card interface in memory-mapped mode only. The Zoom™ Starter Kit reference

design includes a CompactFlash connector for memory-mapped mode, but does not support the hot-swappable capability. See Logic's "SH7727-20 IO Controller Specification" for further details.

The memory mapped mode CompactFlash interface signal on the external connector is: CF_nCE. All other interface signals use the memory mapped address bus – please refer to a reference design for proper connections.

IMPORTANT NOTE: Additional hardware is required on the user's daughter board to provide hot-swapping capability.

IMPORTANT NOTE: The CompactFlash interface referenced here supports memory-mapped mode only.

2.4 10/100 BaseT Ethernet Controller

The SH7727-20 Card Engine uses the SMSC 91C111 10/100 Ethernet single chip solution. The Card Engine Ethernet solution provides an easy to use interface. The four analog PHY interface signals (TPO+, TPO-, TPI+, TPI-) require an external impedance matching circuit. Logic provides example circuit schematics in the Zoom™ Starter Kit for reference.

The 10/100 Ethernet Controller interface signals on the external connectors are: ETHER_RX(-), ETHER_RX(+), ETHER_TX(-), ETHER_TX(+), ETHER_nACT_LED and ETHER_nLNK_LED.

IMPORTANT NOTE: The ENEEP signal on the SMSC 91C111 is connected to a 0 ohm resistor that is not populated. The ENEEP signal has an internal weak pull up in the SMSC 91C111. If the zero ohm resistor is populated, the ENEEP signal is tied low, and will disable the serial EEPROM interface.

2.5 Audio CODEC

The SH7727-20 Card Engine uses the Philips UDA1345TS economy audio CODEC. The UDA1345 audio CODEC has a single channel stereo input and single channel stereo output. See Philips UDA1345TS data sheet for further information.

The analog I/O CODEC interface signals on the external connectors are: CODEC_OUTR, CODEC_OUTL, CODEC_INR and CODEC_INL.

The SH7727-20 Card Engine also brings out all I^2S interface signals through the SO-DIMM expansion connector for users who desire to use a different audio CODEC. Logic has interfaced other high performance audio CODECs to the SH7727 Card Engine. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

The exported I^2S interface signals may only be used with Card Engines that have the on-board CODEC (UDA1345) de-populated. These signals enable the SH7727-20 to interface to an external CODEC of the user's choice. This interface is the SIOF (Serial Input Output with FIFO) interface on the SH7727. It is capable of supporting many different synchronous serial formats, including I^2S. This interface is clock synchronized to the external clock input CODEC_CLK.

The I^2S CODEC data interface signals on the external connectors are: MFP18-uP_COTXD, MFP19-uP_CORXD, MFP20-uP_COSYNC, MFP21-uP_COSCK and MFP22-CODEC_CLK.

If an external CODEC is needed, please contact Logic Product Development for further assistance.

2.6 Analog Front End (AFE) Interface

The AFE interface is a clocked synchronous serial interface with 128-step FIFO, at 16 bits per step. The AFE I/F can be used as a soft modem interface with the proper interfacing electronics.

The AFE interface signals on the external connectors are: MFP9-uP_AFE_TX-PTM5, MFP10-uP_AFE_RX-PTM6, MFP11-uP_AFE_FSYNC-PTM7, MFP12-uP_AFE_nRDET-PTM5, MFP13-uP_AFE_SCLK, MFP14-uP_AFE_nRLYCNT-PTK1, and MFP15-uP_AFE_HC-PTK0.

See the "Renesas SuperH RISC Engine SH7727 Hardware Manual" AFEIF section for more details.

2.7 Video Interface

Renesas's SH7727 microprocessor has a built in LCD controller natively supporting panels up to 1024 x 768 at 8 bit color or 800 x 600 at 16 bit color (contact Logic for 1024x768 at 16 bit color). See the SH7727 microprocessor data sheet for further information on the integrated LCD controller. The LCD controller signals from the SH7727 are located on one of the Card Engine's 80-pin expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

The build-in LCD controller interface signals on the external connectors are: R0-5, G0-5, B0-5, LCD_VSYNC, LCD_HSYNC, LCD_CLKOUT, LCD_DON, LCD_MDISP, LCD_VEEEN and LCD_VDDEN.

Logic also has written drivers for other external graphics controllers that provide higher performance and analog outputs (CRT). Logic provides the signal "VIDEO_nMCS" for the purposes of attaching an external graphics controller to the Card Engine. If an external graphics controller is not needed, this signal may be used for other functions such as additional SDRAM or other memory-mapped peripherals.

IMPORTANT NOTE: Using the internal graphics controller may affect processor performance. Selecting display resolutions and color bits per pixel will vary processor bus-load.

2.8 Serial Interface

The SH7727-20 Card Engine comes with the following synchronous and asynchronous serial channels: UARTA (SH7727 SCIF), SPI (SH7727 SCI), and SIOF (SH7727 SIOF). If additional serial channels are required, please contact Logic for reference designs.

2.8.1 UARTA

The UARTA interface on the SH7727-20 Card Engine uses the SH7727 microprocessor's SCIF port (Serial Communications Interface with FIFO). This is a high-speed full duplex serial interface with 16 byte deep tx and rx FIFOs (asynchronous or clock synchronous). The UARTA interface is the main UART serial channel on the SH7727-20 Card Engine. See the "Renesas SuperH RISC Engine SH7727 Hardware Manual " SCIF section for more details on this port.

The UARTA interface signals on the external connectors are: uP_UARTA_TX, uP_UARTA_RX, uP_UARTA_CTS, and uP_UARTA_RTS.

UARTA is a four wire serial port and does not provide a full array of control signals. If additional hardware modem control signals are needed (such as DSR/DTR), please contact Logic for additional information.

IMPORTANT NOTE: The signals from the Card Engine are TTL level signals not RS232 level. A user must provide an external RS232 transceiver for RS232 applications. Logic provides example circuit schematics in the Zoom™ Starter Kit for reference. When choosing an RS232

transceiver, the user should keep in mind cost, availability, ESD protection, and data rates. Please contact Logic for additional support in choosing the appropriate RS232 transceiver for your application.

2.8.2 SSP/SPI

The SSP/SPI interface on the SH7727-20 Card Engine uses the SCI (Serial Communication Interface) interface on the SH7727 microprocessor. This interface can be used for additional SSP slave peripheral expansion (e.g. companion microcontroller interface).

This port can only do 8 bit transfers and requires that data be valid on the rising edge of uP_SPI_SCK for both transmit and receive. See the “Renesas SuperH RISC Engine SH7727 Hardware Manual “ SCI section for more details on this port.

The SSP interface signals on the external connectors are: uP_SPI_MOSI_TX, uP_SPI_MISO_RX, uP_SPI_SCK, and uP_SPI_FRM.

The SH7727-20 Card Engine uses the SSP bus internally to initialize the UDA1345 Audio CODEC.

Please contact Logic for additional documentation on driver software and how to implement this port in a custom design.

2.8.3 SIOF (Serial I/O with FIFO)

The SIOF (Serial Input Output with FIFO) interface on the SH7727 microprocessor is capable of supporting many different synchronous serial formats, including I^2S. See the “Renesas SuperH RISC Engine SH7727 Hardware Manual“ SIOF section for more information.

On the SH7727-20 Card Engine, the SIOF is used to interface with the on board UDA1354 audio CODEC. If the user desires to use a different audio CODEC, please see the Audio CODEC section of this data sheet.

The SIOF interface signals on the external connectors are: MFP18-uP_COTXD, MFP19-uP_CORXD, MFP20-uP_COSYNC, MFP21-uP_COSCK and MFP22-CODEC_CLK.

2.9 USB Interface

The SH7727-20 Card Engine has two USB channels available. They can be configured as two host interfaces or one host interface and one function interface. They cannot both be function interfaces. Be sure to route the D+ and the D- differential data signals as differential pairs on the custom application board.

2.9.1 USB Host

The SH7727-20 Card Engine can be configured to have 2 USB host ports. Both ports reside in the SH7727 processor’s USB peripheral and conform to USB standard 1.1 and support the OHCI version 1.0 register set. No external circuitry is required to attach the host port directly to a USB host connector and to control power for that connector (suggest using a power controller such as Micrel’s MIC2026-1).

The USB host signals on the external connectors are: uP_USB1_P, uP_USB1_M, uP_USB1_PWR_EN, uP_USB1_nOVR_CRNT, uP_USB2_P, uP_USB2_M, uP_USB2_PWR_EN and uP_USB2_nOVR_CRNT.

2.9.2 USB Function

The USB function interface on the SH7727-20 card uses the SH7727 processor's USB port1 peripheral. Correct implementation of the USB function port requires some logic gates on the custom application board to be implemented.

The USB function signals on the external connectors are: uP_USB1_P, uP_USB1_M, uP_USB1_PWR_EN and uP_USB1_nOVR_CRNT.

Designs that use USB port 1 as a function interface typically rename the signal "uP_USB1_PWR_EN" to "uP_USB1_FUNC_TXEN" and rename "uP_USB1_nOVR_CRNT" to "uP_USB1_DETECT". The logic that is required to allow the USB port 1 to function correctly is :

uP_USB1_FUNC_TXEN <= not ((not uP_USB1_PWR_EN) and uP_USB1_FUNC_CNCT);
uP_USB1_DETECT <= (not uP_USB1_PWR_EN) and uP_USB_FUNC_CNCT;

The signal "uP_USB1_FUNC_TXEN" enables a FET pull up on the D+ line as shown in the LSH7727-10 Application Kit reference schematics. The signal "uP_USB_FUNC_CNCT" is connected to the power pin of the USB function connector (typically pin 1) to sense the connection of a USB cable.

2.10 Touch Interface

A standard four-wire resistive touch panel interface is provided on the SH7727-20 Card Engine. A custom design may interface a four-wire resistive touch panel directly to this interface. The SH7727-20 Card Engine uses the SH7727 microprocessor's analog and digital I/O port interfaces in conjunction with some control logic to provide this touch panel interface.

The analog touch interface signals on the external connectors are: TOUCH_TOP, TOUCH_BOTTOM, TOUCH_RIGHT and TOUCH_LEFT.

IMPORTANT NOTE: The net names reflect the side of the touch screen that they should be attached to and do not necessarily mean X or Y axis, as the terms "X" and "Y" can be interpreted in different ways.

2.11 General Purpose Analog & Digital I/O

Logic designed the SH7727-20 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO on the Card Engine that interface to the SH7727 microprocessor and the on-board CPLD. Some of these GPIO are interrupt capable while other signals are input only.

The Card Engine also has two analog inputs: A/D1 and MFP39–uP_A/D7-uP_D/A0. If desired, the signal MFP39-uPA/D7-uP_D/A0 may be configured to be an analog output (DAC), with an 8-bit resolution.

If certain peripherals are not used, such as the AFE I/F or LCD I/F, multiple GPIO pins become available. Please see the Tabled titled "Multiplexed Signal Tradeoffs" for more information. This table lists the available GPIO that are made available when certain peripheral functions are not used.

Please see the "Pin Descriptions and Functions" section of this manual for a more detailed description of each pin.

2.12 CPLD

Please see the "SH7727-20 IO Controller Specification" for more information.

2.13 Serial EEPROM Interface

Logic designed the SH7727-20 Card Engine to have a low cost 1 Kbit serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the SH7727 microprocessor via the CPLD through a dedicated SPI-like interface. See the figure below. Please see the "SH7727-20 IO Controller Specification" for CPLD information.

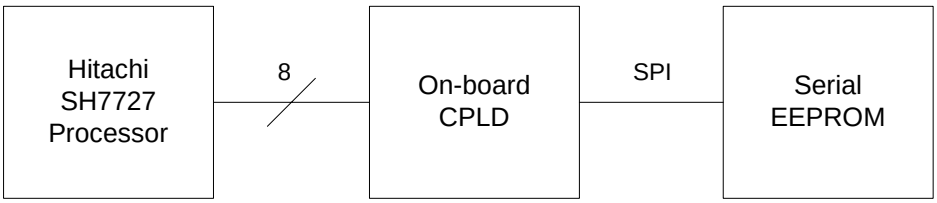


Figure 2.2: Serial EEPROM Block Diagram

2.14 Expansion Options

The SH7727-20 Card Engine was designed to be easily expandable and provides all the necessary control and bus signals to expand the user's design. Many of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. See the SH7727-20 Card Engine schematics for more detail. A user can expand the Card Engine's functionality with peripherals such as PCI, CompactFlash, PCMCIA, ISA devices, etc... Logic has used the expansion options on the Card Engine to interface to other audio CODECs, Ethernet ICs, UARTs, co-processors, graphics controllers etc... Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The SH7727-20 Card Engine was designed to be configurable to meet user's applications and budget needs. The Card Engine supports a variety of embedded operating systems and comes in the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64 MBytes Synchronous DRAM
- Flexible flash footprint: 8, 16, or 32 MBytes Intel StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional Philips UDA1345 Audio CODEC
- Optional Touch Controller

Please contact Logic for additional hardware configurations to meet your application's needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. All internal Card Engine peripheral hardware reset pins are connected to either the MSTR_nRST net or to the RESET_HIGH net as shown in the figure below. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally to the Card Engine. Logic suggests that custom designs implemented with the SH7727-20 Card Engine use the MSTR_nRST signal as the "pin hole" reset used in commercial embedded systems.

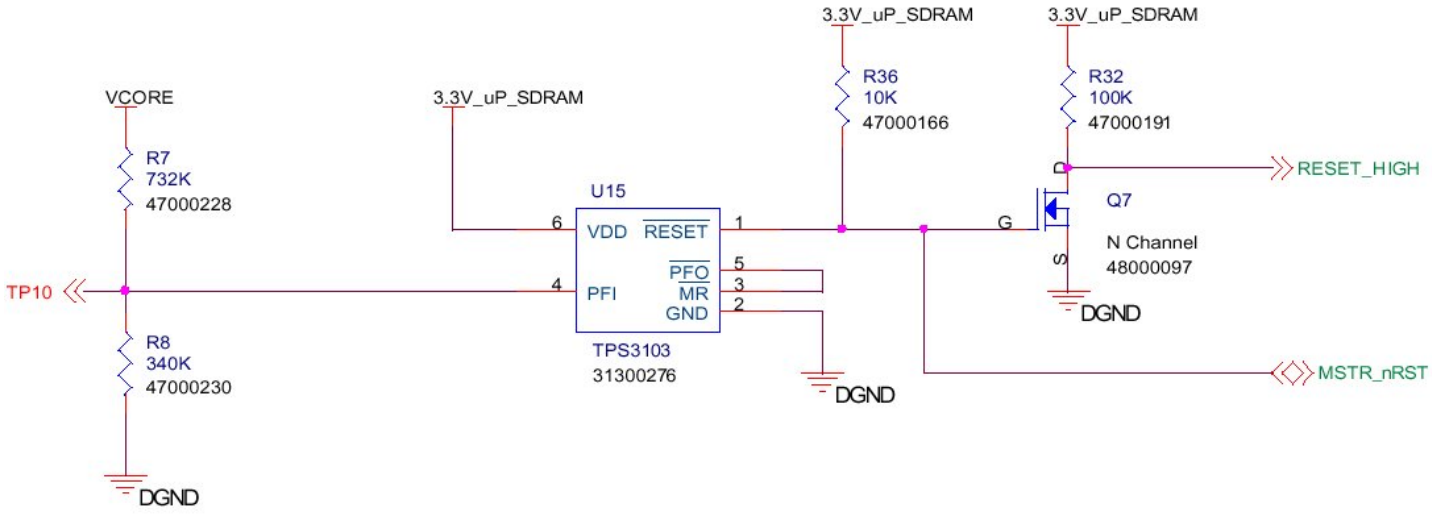


Figure 3.1: Reset Circuit

If MSTR_nRST is asserted (active low), the user can expect to lose information stored in SDRAM as the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal.

The MSTR_nRST signal is an active low output of the reset chip, located on the Card Engine. The RESET_HIGH signal is an active high output of the reset circuit and is not provided as part of the Card Engine connector interface.

IMPORTANT NOTE: The custom design should guard the assertion of the reset lines during a low power state so the microprocessor cannot be reset and powered on in a low or bad power condition (will cause data corruption and possible temporary system lockup). See section entitled "Power Management" for further details.

There are three conditions that will generate a low on the output reset pin of the reset chip (the MSTR_nRST signal): power-on condition, a low pulse on the MSTR_nRST signal, and the power fail comparator input (PFI pin) falling below the internal comparator threshold.

Power On:
At power on, MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 2.941V. Once the 3.3V_uP_SDRAM supply becomes higher than 2.941V, an internal timer will delay the rising edge of MSTR_nRST from 65 to 195 mS (130 mS typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (custom design application board) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic also suggests analog or digital de-bouncing of an external assertion source of the MSTR_nRST signal.

Power Fail:
If the power fail comparator input pin (PFI pin) falls below the internal comparator threshold of 0.551V, it will create a low pulse on the MR input pin of the reset chip. The low assertion of the MR pin will assert the MSTR_nRST signal and will hold it low after the MR pin is deasserted (PFI is above the comparator level – power is restored) for 65 to 195 mS (130 mS typical).

Please see the TI TPS3103 data sheet at http://www.ti.com for additional details on reset timing and thresholds.

3.2.2 Soft Reset

Logic has created a soft reset signal named uP_SW_nRESET that can be used to reset the SH7727 microprocessor's internal registers without affecting the peripherals on the rest of the board and without losing data stored in SDRAM or other volatile storage. The uP_SW_nRESET signal is an input to the SH7727's manual reset input pin.

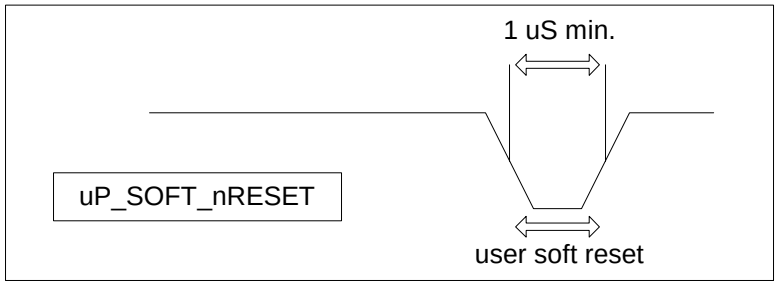


Figure 3.2: Soft Reset

See the "Renesas SuperH RISC Engine SH7727 Hardware Manual " for specific details on register conditions after a soft (manual) reset.

3.3 Interrupts

There are five interrupt signals from the SH7727-20 Card Engine that are reserved for external interrupt sources: uP_IRQA, uP_IRQB, uP_IRQC, uP_IRQD, and uP_NMI. All of these signals default to interrupt on low level. The interrupts uP_IRQA, uP_IRQB, uP_IRQC can be changed in software to enable them to be edge or level triggered, while uP_IRQD and uP_NMI are low level active-only. Interrupts A-D are in order of most dedicated/highest priority to least dedicated/lowest priority. In other words, uP_IRQA is a dedicated IRQ line with the highest priority, where as uP_IRQD is a port interrupt with the lowest priority (see Pin Description section for details).

The uP_NMI interrupt should only be used in time critical applications. In Logic's software BSPs, the uP_NMI signal is typically used for power management intervention.

The SH7727-20 Card Engine also has other GPIO pins that can be used as external interrupts. Please review the Pin Multiplexing and Initialization tables in this manual for information. Contact Logic for more information in implementing additional interrupts in your design.

See the "Renesas SuperH RISC Engine SH7727 Hardware Manual " for more information on interrupt sources.

3.4 H-UDI JTAG Debugger Interface

The SH7727 microprocessor has a Renesas User Debugging Interface (H-UDI) implemented through a JTAG-compatible interface. Renesas provides an E10A for SH7727 PCI or PCMCIA emulator that connects to this interface for debugging purposes. The following signals make up the JTAG interface to the SH7727, for connection to an E10A emulator card: uP_TRST, uP_TMS, uP_TDO, uP_TDI, uP_TEST1, and uP_TEST2.

These signals should interface directly to a 14-pin 0.1" through hole connector as demonstrated in Logic's circuit schematics in the Zoom™ Starter Kit or other reference designs. The connector used can also be a 36 pin Renesas UDI port connector as demonstrated in the "Renesas E10A for SH7727" documentation. The emulator cards are available from Renesas in either PCI or PCMCIA format, and function under supported operating systems (please see http://www.renesas.com/ for a list of available drivers).

This H-UDI JTAG connection is very useful when:

- debugging new hardware
- debugging low level software
- recovering a board that has a corrupted boot-block

Renesas also provides eXDI plug-in drivers to support Microsoft Windows CE Platform Builder as a hardware debugging tool. By using the eXDI functionality, it is possible to debug your low level Windows CE code using the Platform Builder interface with very little else functioning on the system.

IMPORTANT NOTE: When laying the 14 pin connector out, realize the Renesas pin numbering does not conform to a standard 14 pin 0.1" through hole connector pin numbering scheme. See Logic's reference designs for further details. Contact Renesas (http://www.renesas.com/) for ordering information for E10A emulators.

3.5 Power Requirements

3.5.1 System Power Supplies

The SH7727-20 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, 3.3V_WRLAN and VCORE for a flexible hardware design. All

power areas are inputs to the Card Engine with the exception of 3.3V_WRLAN, which is an output from the Card Engine.

3.5.1.1 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins are meant to be connected to a 3.3V power supply with optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using STANDBY mode with its software BSPs to prepare the system for the critical power condition. In order to do this, STANDBY mode puts the SDRAM into self-refresh mode and processor into the standby state. Please see the description of STANDBY mode later in this section.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane power the majority of the peripheral's digital supply pins on the SH7727-20 Card Engine. This supply must stay within the acceptable levels as specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a STANDBY sequence and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane power all analog power supply pins of both the SH7727 microprocessor and applicable peripherals on the SH7727-20 Card Engine. This supply must stay within the acceptable levels as specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a STANDBY sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This "power" supply net is an output from the Card Engine. It is controlled through a registered bit in the on-board CPLD. See the "SH7727-20 IO Controller Specification" manual for specific details on this control bit. Logic's software BSPs assert this signal as appropriate. This is done because the software power management in the 91C111 does not put the part in a low enough power state for many applications.

The custom application board should use this power supply output pin to supply the Ethernet impedance matching resistors with power. They should not be connected to 3.3V directly or the entire Ethernet controller circuit on the Card Engine will try to power itself through the impedance matching resistors. Please see Logic's schematics for the Zoom™ Starter Kit or other reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the Card Engine is to power the 91c111 separately and give the ability to shut it off completely but independently. The 3.3V_WRLAN output from the Card Engine is required to completely isolate the LAN circuit such that it is not back powered through the impedance matching resistors.

3.5.1.5 VCORE

The VCORE input pins are meant to be connected to a 1.9V power supply with optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using STANDBY mode with its software BSPs to prepare the system for the critical power condition. In order to do this,

STANDBY mode puts the SDRAM into self-refresh mode and processor into the standby state. Please see the description of STANDBY mode later in this section.

3.5.2 Power On/Off Sequence

The SH7727 microprocessor requires power supply sequencing for the system to comply with certain time requirements. When powering on the system, the core voltage supply (VCORE) must be at an acceptable level (see Electrical Specifications section) within 1 mS maximum of the DC I/O supply voltages (3.3V, 3.3V_uP_SDRAM). The power-off sequence should be in the reverse order of the power-on sequence.

Please see the "Renesas SuperH RISC Engine SH7727 Hardware Manual" for additional information and diagrams.

3.5.3 System Power Management

Good power management design happens in the hardware and software of any system. Typically, the power management design of any embedded system can be one of the most complicated parts and has a dramatic effect on the overall product cost, performance, usability, and customer satisfaction. Many factors effect good power management design in the hardware including: power supply selection (efficiency), clocking design, IC and component selection, etc. The SH7727-20 Card Engine electronics were designed to provide maximum flexibility to the software and system integrator.

There are many different software configurations which drastically effect the power consumption of the SH7727-20 Card Engine including: microprocessor core clock frequency, microprocessor bus clock frequency, microprocessor peripheral clocks, microprocessor bus utilization, microprocessor power management states (normal, sleep, standby, module-standby), peripheral power states and modes, product user scenarios, interrupt handling, display settings (resolution, backlight, refresh, bits per pixel, etc..) These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. These items are covered in the appropriate documents such as the Bootloader User's Manual or appropriate BSP manual.

IMPORTANT NOTE: The SH7727-20 Card Engine hardware architecture was designed for low power battery operated applications. However, the Altera CPLD on the SH7727-20 Card Engine is not an ideal part for low power battery operated designs. This specific component was chosen for cost. If one is using the SH7727-20 Card Engine as a low power reference design, one can consider other programmable logic devices that are optimized for power, not cost.

3.5.4 Peripherals

Most peripherals provide software programmable power states. Please see the appropriate data sheet for more information and the "SH7727-20 IO Controller Specification" for details. The SMSC 91C111 controller has software programmable power states but may not be sufficient for some applications. Logic has provided hardware to cut power to the 91C111 IC.

3.5.5 System Power States

The SH7727-20 Card Engine power management's scheme was designed to be easy to use. Logic has provided hardware signals to activate three power management states on the SH7727-20 Card Engine that take advantage of the SH7727 microprocessor's power management features. These power management states must be supported by the installed software BSP in order to function correctly. See the BSP documentation for more information.

The System Power States provided for are: Normal Operating Mode, Suspend Mode and Standby Mode. Each of these modes are described below.

The SH7727 microprocessor provides for four power management modes: NORMAL, STANDBY, SLEEP, and Module STANDBY. A very useful software and hardware development feature are the microprocessor status lines that are exported as the nets : uP_STATUS1 and uP_STATUS_2. These status lines are hardware-controlled signals that signify the current operating mode of the microprocessor. Please see the Pin Descriptions table of this document and the "Renesas SuperH RISC Engine SH7727 Hardware Manual" for more details.

IMPORTANT NOTE: The BSPs available from Logic for the different operating systems supported on the SH7727-20 Card Engine may not support all power management states. Please see the appropriate BSP documentation for power management modes for more detail.

3.5.5.1 Normal Operating Mode

The SH7727-20 Card Engine's normal operating state is Normal Operating Mode. This is the mode that the Card Engine is in during most of its active operation. Normal Operating Mode may also contain scenarios in which the processor is actually in its "sleep" mode while waiting for a task to be activated, as is the case with the Windows CE implementation.

The SH7727 microprocessor enters its normal operating state on reset and returns to this state when any unmasked-enabled interrupt is received, even if operating in another power mode. The SH7727 cannot transition directly between the other power states; it will always return to its normal operating state before entering any other power state.

3.5.5.2 Suspend Mode

The Suspend Mode is the SH7727-20 Card Engine's software power down mode and must be supported in the installed BSP to realize functionality. BSP support of Suspend Mode will enable the system to shutdown every on-board peripheral through its software interface and will put the SH7727 microprocessor into its standby state. The only on-board peripheral that is shutdown in hardware in Suspend Mode is the 91C111 Ethernet controller.

In Suspend Mode, all registers are maintained and the system may be resumed at the same point as it left off.

The sequence to enter Suspend Mode is shown in the figure below. Please refer to the specific BSP or software documentation for system behavior as dictated by the installed software.

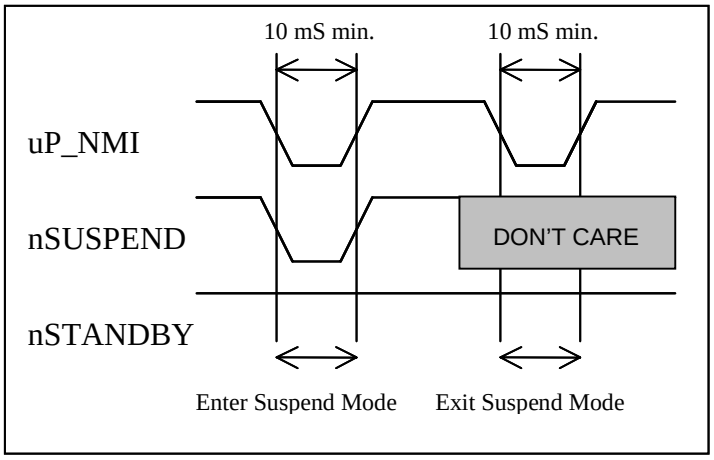


Figure 3.3: Enter/Exit Suspend Mode

3.5.5.3 Standby Mode

The Suspend Mode is the SH7727-20 Card Engine's hardware power down mode and must be supported in the installed BSP to realize functionality. BSP support of Standby Mode will enable the system to put the SDRAM in self-refresh mode and put the processor in its standby state. The nSTANDBY signal is connected to every peripheral's hardware shutdown pin on the Card Engine and should be connected in the same manner on the custom application board. The assertion of the nSTANDBY signal should only be done in critical power conditions or in conditions in which the current state of the processor is of less importance than retaining SDRAM contents.

In Standby Mode, register contents are not maintained and the system may be resumed only through the assertion of the MSTR_nRST signal. The custom application board may also disconnect power from the 3.3V and 3.3VA nets after asserting the nSTANDBY signal for at least 10mS. Before asserting the MSTR_nRST signal to re-initialize the system, the custom application board should be certain that good power has been re-applied to the system or a partial boot condition may result, corrupting SDRAM and causing the system to lose state information.

The sequence to enter Standby Mode is shown in the figure below. Please refer to the specific BSP or software documentation for system behavior as dictated by the installed software.

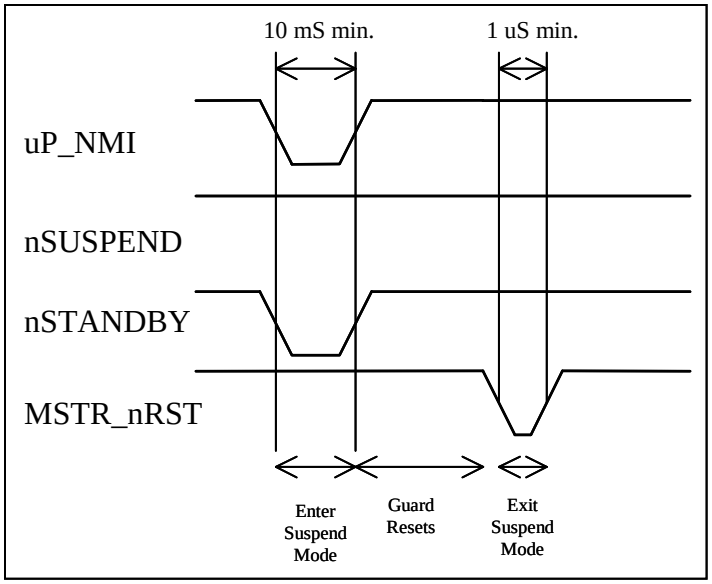


Figure 3.4: Enter/Exit Standby Mode

3.6 ESD Considerations

The SH7727-20 Card Engine was designed to interface to a customer's peripheral board and was designed to be low cost and adaptable to many different applications. Therefore the SH7727-20 Card Engine does not provide any ESD protection circuitry on the card. ESD protection circuitry must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory and I/O Mapping

4.1 SH7727 Memory Map

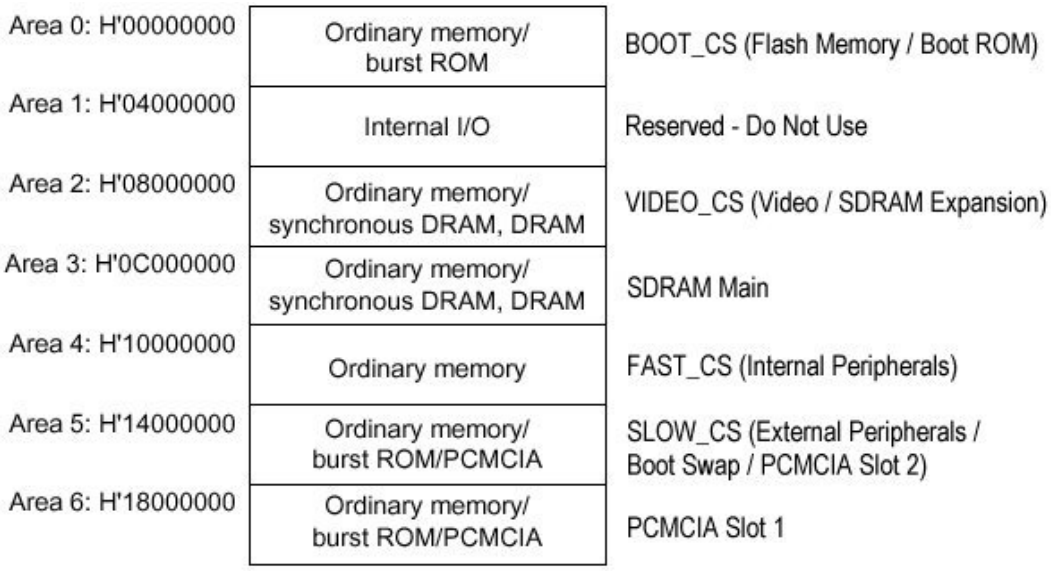


Figure 4.1: SH7727 Card Engine General Memory Map

Figure 4.1.1 shows the general addressing scheme for the memory areas on the SH7727 Card Engine. Please note that the addresses specified do not include the logical memory mapping offsets. Figure 4.1.2 shows these offsets.

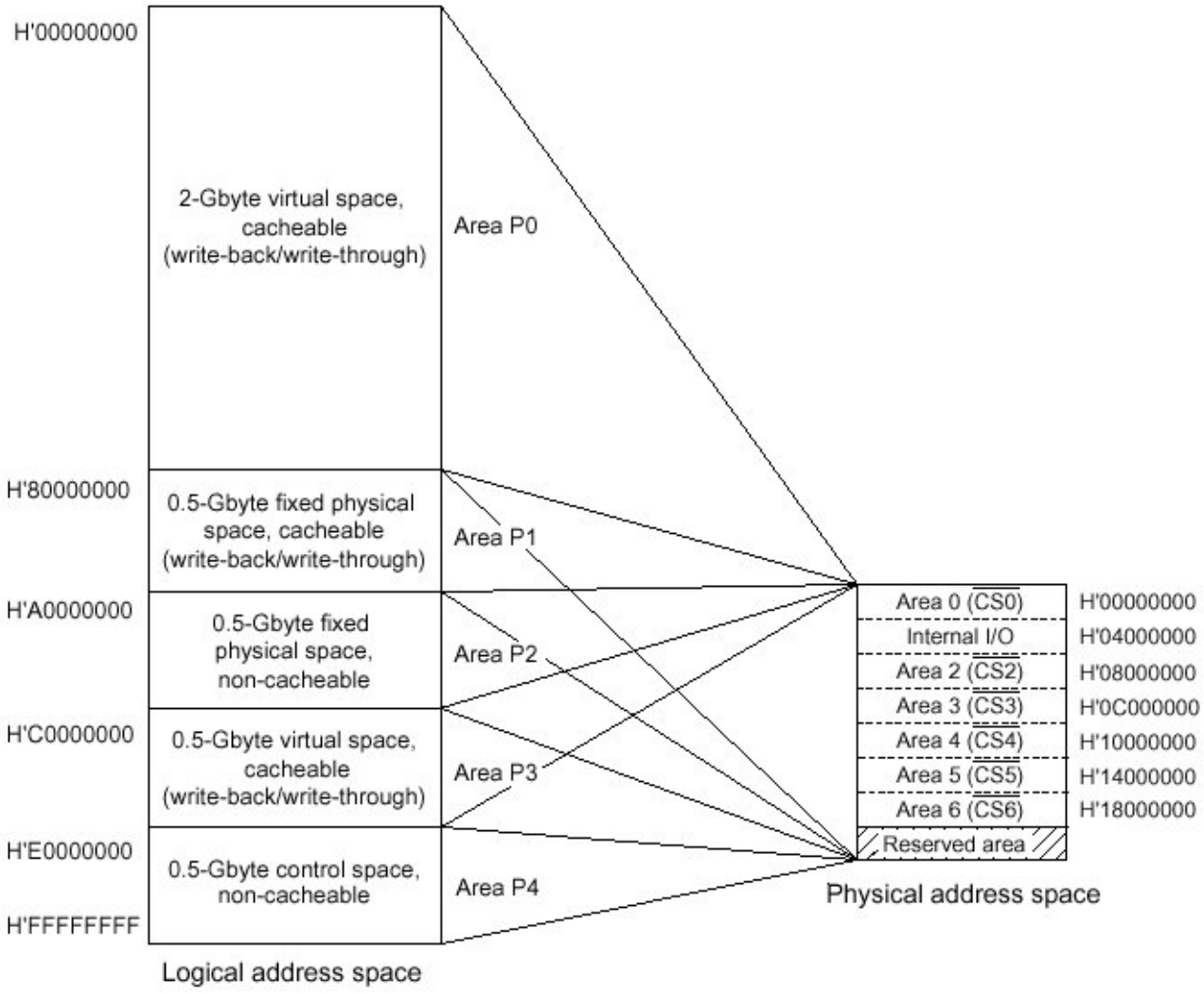


Figure 4.2: SH7727 Logical Memory Mapping in Privileged Mode

Figure 4.1.2 shows the logical memory mapping for the SH7727 in privileged mode. To access hardware peripherals that may be changing depending upon outside sources, the user should always use Area P2 as the access space (uncached physical). Program memory, such as SDRAM or flash, may be accessed through Area P1 even when the MMU is not initialized. When the MMU is properly initialized and maintained, the user can access main memory through Area P0.

For example, to access a hardware-peripheral in physical area 5 of memory (CPLD Slow Peripherals), use Logical Area P2 to access it. The actual access address would be 0xB4000000 (0xA0000000 logical offset + 0x14000000 physical offset).

4.1.1 Boot Chip Select (BOOT_nMCS) – Card Engine External Boot Memory

Use the BOOT_nMCS signal to select an external boot device, such as an EPROM, a flash device or even non-volatile SRAM. BOOT_nMCS will only be asserted if uP_MODE3 is low, otherwise, the Card Engine will assume it should boot from on-board flash and BOOT_nMCS will never be asserted. When uP_MODE3 is low, BOOT_nMCS is a direct pass through for Area 0 of physical memory.

Use uP_MODE0 and uP_MODE1 to specify the bus width of the device attached to BOOT_nMCS. Be aware that these signals must be tied directly to either ground or 3.3V if the user wants to set a specific width. This must be done because the internal Card Engine circuitry uses 10K resistor pull ups/downs to make Area 0 default to 32 bits wide.

When uP_MODE3 is low, the internal flash memory is disabled by default. It may be remapped to area 5, thereby disabling the SLOW_nMCS signal, if the bit 3 in the flash reg is cleared (see the CPLD Interface Specification for details). If the LSBit of this register is written with a "1" (default value), the internal flash memory is disabled, allowing the assertion of the SLOW_nMCS signal. If the LSBit of this register is a "0", the internal flash is remapped to Area 5, which disables the CPLD Slow Peripherals (SLOW_nCS is not asserted). See the CPLD Interface Specification for details.

When uP_MODE3 is high (default setting), devices attached to BOOT_nMCS may be accessed at an offset into Area 5. The access width in Area5, while uP_MODE3 is high, is 16 bits. So the device attached to BOOT_nMCS must be attached as a 16 bit peripheral for correct memory access. See the section on SLOW_nMCS below for details.

BOOT_nMCS is a buffered signal and is typically delayed 4nS longer than the processor local bus timing.

4.1.2 Video Chip Select (VIDEO_nMCS) – Video and SDRAM Expansion Area

The VIDEO_nMCS signal is typically used to select external high-speed graphics controllers. However, it can also be used to select additional SDRAM if densities greater than 64MB (the limit of the SDRAM Main area) are needed.

IMPORTANT NOTE: Please contact Logic for details on interfacing additional SDRAM to this area. This interface, while electrically provided, depends highly on the implementation of the external SDRAM design.

VIDEO_nMCS is accessed through physical area 2 of memory and is default 32 bits wide.

VIDEO_nMCS is a buffered signal and is typically delayed 4nS longer than the processor local bus timing.

4.1.3 SDRAM Main Area

The SDRAM Main area is always used internally for the main SDRAM memory. Depending on the Card Engine's configuration, the memory size may be 16, 32 or 64 MB.

The SDRAM Main occupies physical area 3 of memory and is default 32 bits wide.

4.1.4 Fast Chip Select (FAST_nMCS) – CPLD Fast Peripherals Area

The table below indicates how the CPLD decodes the FAST_nMCS signal.

FAST_nMCS is accessed through physical area 4 of memory and is set to be 16 bits wide.

FAST_nMCS is a buffered signal and is typically delayed 4nS longer than the processor local bus timing.

For more detailed information on the partitioning of the memory blocks, see the SH7727-20 IO Controller Specification.

Chip Select	Address Range	Mem Block Description	Size
FAST_nMCS	0x1000 0000 – 0x11FF FFFF	Reserved: On-Board Use	2MB (16X)
FAST_nMCS	0x1200 0000 – 0x12FF FFFF	Reserved: Defined Off-Board Use	1MB (16X)
FAST_nMCS	0x1300 0000 – 0x13FF FFFF	Open: Off Board Use	1MB (16X)

4.1.5 Slow Chip Select (SLOW_nMCS) – CPLD Slow Peripherals / Boot Swap / PCMCIA Slot 2

The table below indicates how the CPLD decodes the SLOW_nMCS signal.

SLOW_nMCS is accessed through physical area 5 of memory and is set to be 16 bits wide.

SLOW_nMCS is a buffered signal and is typically delayed 4nS longer than the processor local bus timing.

For more detailed information on the partitioning of the memory blocks, see the SH7727-20 IO Controller Specification.

Chip Select	Address Range	Memory Description	Size
SLOW_nMCS	0x1400 0000 – 0x141F FFFF	Boot Chip Select	2MB
SLOW_nMCS	0x1420 0000 – 0x143F FFFF	CF Chip Select	2MB
SLOW_nMCS	0x1440 0000 – 0x145F FFFF	ISA-like Bus Chip Select	2MB
SLOW_nMCS	0x1460 0000 – 0x15FF FFFF	Reserved	2MB (13X)
SLOW_nMCS	0x1620 0000 – 0x16FF FFFF	Reserved: Defined Off-Board Use	1MB (16X)
SLOW_nMCS	0x1700 0000 – 0x17FF FFFF	Open : Off Board Use	1MB (16X)

If the custom design does not use peripherals in the SLOW_nMCS area, this area may also be configured to comply with PCMCIA timing for a second PCMCIA slot. PCMCIA mode for area 5 DOES NOT allow the user to also use the uP_PCC_XXX I/O control lines, but the PCMCIA bus control signals are valid (OE, WE, IORD, IOWR, CE1A, CE2A). If the PCMCIA mode is used, the design must register and supply the other PCMCIA signals externally (e.g. VS lines, BVD lines, REG signal).

If uP_MODE3 is low and the flash register has bit 3 set to 0 (default value is 1), area 5 memory accesses will be re-routed to the on-board flash memory and the SLOW_nMCS signal will not be asserted. If uP_MODE3 is low and bit three of the flash register is set to 1 (default value), accesses in area 5 of memory will assert the SLOW_nMCS signal.

4.1.6 PCMCIA Slot 1

The PCMCIA Slot 1 chip selects use physical area 6 of memory. PCMCIA cards attached to this area of memory may be accessed in memory or I/O mode.

5 Pin Descriptions and Functions

Please reference the following tables for detailed information about the signals on the SH7727-20 Card Engine interface connectors. Reference the Pin Description tables for a general description of the signal connected to the Card Engine's connectors. Reference the Pin Multiplexing table for a description of secondary functions possibly available for specified pins depending on peripheral utilization. Reference the Software Initialization Pin State table for expected pin states after Logic's Bootloader or standard BSPs have initialized the system.

IMPORTANT NOTE: Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the Card Engine do not necessarily line up with the mode line numbers on the processor.

5.1 Pin Description Tables

5.1.1 144-Pin SODIMM (J1C) Connector Pin Descriptions

The table below lists general descriptions for each signal connected to the 144-pin SODIMM connector (J1C) on the SH7727-20 Card Engine.

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O[1]	Active Low. This signal initiates a hard reset (power on) – external memory contents are lost during reset. Every peripheral on the Card Engine with a reset line is reset with the assertion of this signal. Refer to SH7727 processor datasheet for register states during or after power on reset.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	uP_SW_nRESET	I[1]	Active Low. This signal initiates a soft reset (manual reset) – external memory contents are retained during reset. Only the SH7727 processor receives this reset signal (as a manual reset).
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nMCS	O	Active Low. Buffered chip select for area 4 of SH7727-20 memory. This is the "fast" peripheral chip select area. This is set to a 16 bit wide area and should not be changed. See memory map for details.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).

Pin #	Signal Name	I/O	Description
8	SLOW_nMCS	O	Active Low. Buffered chip select for area 5 of SH7727-20 memory. This is the "slow" peripheral chip select area. When uP_MODE3 is low, memory accesses to area 2 of memory may be diverted to the on-board flash memory as dictated by the software (this signal will be inactive high in that case). This is set to a 16 bit wide area and should not be changed unless the slow peripherals are not needed. See memory map for details.
9	DGND	I	Digital Ground (0V)
10	MFP_31 – VIDEO_nMCS	O	Active Low. Buffered chip select for area 2 of SH7727-20 memory. This is the "video" chip select area. This chip select is also capable of controlling additional external SDRAM. This is set to a 32 bit wide area and can be changed based on the user's needs. See memory map for details.
11	ETHER_nACT_LED	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nMCS	O	Active Low. This signal is the buffered chip select for boot ROM and is connected to area 0 of SH7727-20 memory when uP_MODE3 is low. When uP_MODE3 is high, this signal is activated at a specific memory mapped address in the slow chip select area (16 bit wide area 2). The memory width for area 0 is selectable with uP_MODE0 and uP_MODE1. See memory map for details.
13	ETHER_nLNK_LED	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. This signal is driven by the ISA bus master or DMA controller to signal valid write data on the data bus. A peripheral may use this signal to latch the data in.
15	nSTANDBY	I[1]	Active Low. CPU power mode signal. When low during an NMI interrupt, Card Engine will enter standby mode (hardware powerdown), where SDRAM will be in self-refresh. The only way to exit standby mode is by a processor reset.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	VDD3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid.
21	uP_NMI	I[1]	Active Low. The non-maskable interrupt – highest priority - for the CPU. Used to signal power events (type of event is qualified by STANDBY and SUSPEND) or highest priority interrupt.

Pin #	Signal Name	I/O	Description
22	nCHRDY	I[1]	Active Low. The I/O channel ready signal line allows the resources to indicate to the ISA bus master that additional cycle time is required. Peripherals using this signal must make their outputs open drain, as it is a shared bus.
23	uP_IRQD	I[1]	Active Low. Port interrupt on SH7727-20 (SH7727 pin PINT11). May also be configured as a general purpose input only pin.
24	uP_TEST1	I[1]	This is connected to the SH7727's ASEMD0 pin and is tied high on the Card Engine. Connect to pin 8 of a normal dual row header which is designated pin 11 in the E10A manual. See ZOOM Starter Development Kit reference schematics for more information.
25	uP_IRQC	I[1]	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ4). May also be configured as a general purpose input only pin.
26	uP_TEST2	I	This is connected to the SH7727's ASEBRKAK pin directly with no pull up/down resistors connected. The Renesas E10A manual suggests pulling this to 3.3V with a 4.7k Ohm resistor. Connect to pin 7 of a normal dual row header which is designated pin 4 in the E10A manual. See ZOOM Starter Development Kit reference schematics for more information.
27	uP_IRQB	I[1]	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ3). May also be configured as a general purpose input only pin.
28	uP_TRST	I[1]	JTAG Test Reset Input. May leave unconnected if not using the JTAG port.
29	uP_IRQA	I[1]	Active Low. Dedicated hardware interrupt on SH7727-20 (SH7727 pin IRQ0). May also be configured as a general purpose input only pin.
30	uP_TMS	I[1]	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port.
31	uP_nMBS	O	Active Low. This buffered signal signifies the start of an external bus cycle from the processor.
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use.
33	uP_nBACK	O	Active Low. Acknowledge signal in response to uP_BREQ signifying that CPU is releasing bus control.
34	uP_TDI	I[1]	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port.
35	uP_nBREQ	I[1]	Active Low. Request for CPU to release bus control.
36	uP_TCK	I[1]	JTAG Test Clock Input. May leave unconnected if not using the JTAG port.
37	uP_nWAIT	I	Active low. The WAIT signal requests the current bus cycle be extended until this signal is de-asserted. This signal will completely halt processor operations until it is de-asserted and the bus cycle is ended. Peripherals using this signal must make their outputs open drain, as it is a shared bus. This signal has a 1K pull up resistor to 3.3V on the Card Engine.
38	uP_MODE3	I[1]	Boot select signal (0 = external boot device, 1 = onboard flash). This defaults to high (onboard flash) if left unconnected (pulled to 3.3V through a 10K pullup resistor).
39	uP_UARTA_RTS	O	Active low. Request to send for SCIF port (UARTA).

Pin #	Signal Name	I/O	Description
40	uP_MODE2	I[1]	Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left unconnected (pulled to 3.3V through a 10K pullup resistor).
41	uP_UARTA_CTS	I[2]	Active low. Clear to send for SCIF port (UARTA).
42	uP_MODE1	I[1]	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = INVALID , 0/1 = 8 bit, 1/0 = 16 bit, 1/1 = 32 bit. This defaults to high if left unconnected (pulled to 3.3V through a 10K pullup resistor).
43	uP_UARTA_TX	O	SCIF port (UARTA) transmit data output.
44	uP_MODE0	I[1]	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = INVALID , 0/1 = 8 bit, 1/0 = 16 bit, 1/1 = 32 bit. This defaults to high if left unconnected (pulled to 3.3V through a 10K pullup resistor).
45	uP_UARTA_RX	I	SCIF port (UARTA) receive data input.
46		NC	No internal connection (not implemented on the SH7727-20)
47		NC	No internal connection (not implemented on the SH7727-20)
48	uP_DREQ0	I[1]	Active low. DMA channel 0 external request (low level or falling edge selectable). This may also be configured as a general purpose input only pin PTD4.
49		NC	No internal connection (not implemented on the SH7727-20)
50		NC	No internal connection (not implemented on the SH7727-20)
51	nSUSPEND	I[1]	Active low. CPU power mode signal. When low during an NMI interrupt, Card Engine will enter suspend mode (software powerdown). Suspend mode can be exited with the assertion of a high priority interrupt or reset.
52	uP_DRAK0 - uP_PCC_RESET	O || O	DMA channel 0 external request acknowledge (active state selectable) || Active high. PCMCIA reset.
53	uP_AUX_CLK	O	This auxiliary clock is controlled in the CPU and can be used by the peripherals. It is the same frequency and phase as the bus clock, but is separately buffered. Connect only three loads or buffer for extended fan out (SH7727 manual specifies a 50pF load maximum).
54		NC	No internal connection (not implemented on the SH7727-20)
55	DGND	I	Digital Ground (0V)
56	uP_DACK0 - uP_PCC_nDRV	O || O[1]	DMA channel 0 acknowledge (active state selectable) || Active low. PCMCIA drive enable.
57	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
58	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
59	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
60	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.

Pin #	Signal Name	I/O	Description
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
65	uP_SPI_FRM	O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI data transmission or reception. This signal is attached the SH7727's PTJ1 pin.
66	uP_BUS_CLK	O	Bus clock. Operates at 51.6MHz. Do not connect to any loads unless first buffered for extended fanout. Suggest using uP_AUX_CLK instead.
67	uP_SPI_MOSI_TX	O	This output transmits synchronous SPI data.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_MISO_RX	I[1]	This input receives synchronous SPI data.
70	uP_nRAS	O[1]	Active low. This signal is sent to a random access memory to tell that an associated address is a row address.
71	uP_SPI_SCK	O	SPI clock signal. SPI transmit/receive data is valid on the rising edge of this clock (data is output from one falling edge to the next and clocked in on the rising edge).
72	uP_nCAS	O	Active low. This signal is sent to a random access memory to tell that an associated address is a column address.
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74	uP_nMWE3 - uP_PCC_nIOWR - uP_nDQM3	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2 - uP_PCC_nIORD - uP_nDQM2	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMWE1 - uP_PCC_nWE - uP_nDQM1	O	Active low. Buffered write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed).
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0 - uP_nDQM0	O	Active low. Buffered write enable for buffered data bus bits 7->0 - DQM0 SDRAM signal from the LSH7727. Both functions are valid (functionality changes based on memory area accessed)
81	uP_MD4	I/O	Buffered Data Bus bit 4.

Pin #	Signal Name	I/O	Description
82	uP_nMWR	O	Active low. When low, this bufferred signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal can be used for buffer direction control.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD - uP_PCC_nOE	O	Active low. This bufferred signal is the read strobe that latches data output from external peripherals. It is also the PCMCIA OE signal when areas 5 or 6 are accessed in PCMCIA mode.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the SH7727-20)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection (not implemented on the SH7727-20)
89	DGND	I	Digital Ground (0V)
90	uP_MA0	I/O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	I/O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	I/O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	I/O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	I/O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	I/O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	I/O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	I/O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	I/O	Buffered Address Bus bit 8.
107	VDD3.3V	I	Power Supply (3.3V)
108	uP_MA9	I/O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	I/O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	I/O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	I/O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.
116	uP_MA13	I/O	Buffered Address Bus bit 13.
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	I/O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	I/O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	I/O	Buffered Address Bus bit 16.

Pin #	Signal Name	I/O	Description
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	I/O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	I/O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	I/O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	I/O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	I/O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	I/O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.
136	uP_MA23	I/O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	I/O	Buffered Address Bus bit 24.
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	I/O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	VDD3.3V	I	Power Supply (3.3V)

5.1.2 80-Pin Expansion Connector A (J1A) Pin Descriptions

The table below lists general descriptions for each signal connected to the 80-pin expansion connector A (J1A) on the SH7727-20 Card Engine.

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC	O	LCD Vsync/ Frame line marker (active state selectable) || General purpose I/O PTE3.
2	LCD_HSYNC	O	LCD Hsync/ Line clock (active state selectable) || General purpose I/O PTD5.
3	LCD_DCLK	O	LCD data clock || General purpose I/O PTH7.
4	LCD_DON	O	Active high. LCD display on signal || General purpose I/O PTD7.
5	LCD_MDISP	O	LCD current alternating signal/LCD enable signal || General purpose I/O PTE6.
6	LCD_VEEEN	O	Active high. LCD panel Vee enable.
7	LCD_VDDEN	O	Active high. LCD panel Vcc enable.
8		NC	No internal connection (not implemented on the SH7727-20)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the SH7727-20)
11		NC	No internal connection (not implemented on the SH7727-20)
12		NC	No internal connection (not implemented on the SH7727-20)
13		NC	No internal connection (not implemented on the SH7727-20)
14		NC	No internal connection (not implemented on the SH7727-20)
15		NC	No internal connection (not implemented on the SH7727-20)
16		NC	No internal connection (not implemented on the SH7727-20)

Pin #	Signal Name	I/O	Description
17	uP_STATUS_1	O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Running, 0/1 = Standby, 1/0 = Sleep, 1/1 = Reset || General purpose I/O PTJ6.
18	uP_STATUS_2	O	Processor status pin. uP_STATUS_2/uP_STATUS_1 -> 0/0 = Running, 0/1 = Standby, 1/0 = Sleep, 1/1 = Reset || General purpose I/O PTJ7.
19		NC	No internal connection (not implemented on the SH7727-20)
20		NC	No internal connection (not implemented on the SH7727-20)
21		NC	No internal connection (not implemented on the SH7727-20)
22		NC	No internal connection (not implemented on the SH7727-20)
23		NC	No internal connection (not implemented on the SH7727-20)
24	DGND	I	Digital Ground (0V)
25	A/D1	I	Analog input (SH7727 pin AN4) : 0 to 3.3V swing possible.
26		NC	No internal connection (not implemented on the SH7727-20)
27	AGND	I	Analog Ground (0V)
28	MFP39 - uP_A/D7 - uP_D/A0	I || O	Analog input (SH7727 pin AN7) : 0 to 3.3V swing possible || Analog output (SH7727 pin DA0) : 0 to 3.3V swing possible.
29		NC	No internal connection (not implemented on the SH7727-20)
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line-in input of the audio CODEC. 1V RMS typcial, 2V RMS max (if current limited to 1mA or less).
32	CODEC_INR	I	Right channel stereo line-in input of the audio CODEC. 1V RMS typcial, 2V RMS max (if current limited to 1mA or less).
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	Four wire resistive touch panel left position connection.
37	TOUCH_RIGHT	I	Four wire resistive touch panel right position connection.
38	TOUCH_BOTTOM	I	Four wire resistive touch panel bottom position connection.
39	TOUCH_TOP	I	Four wire resistive touch panel top position connection.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. RED 0 - internally shorted to R5 due to SH7727 only supplying 5 red pins. (SH7727 pin LCD_D15)
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1. (SH7727 pin LCD_D11)
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2. (SH7727 pin LCD_D12)
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3. (SH7727 pin LCD_D13)
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4. (SH7727 pin LCD_D14)
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5. (SH7727 pin LCD_D15)
48	G0	O	The LCD data bus used to transmit data to the LCD module. GREEN 0. (SH7727 pin LCD_D5)
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1. (SH7727 pin LCD_D6)

Pin #	Signal Name	I/O	Description
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2. (SH7727 pin LCD_D7)
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3. (SH7727 pin LCD_D8)
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4. (SH7727 pin LCD_D9)
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5. (SH7727 pin LCD_D10)
54	B0	O	The LCD data bus used to transmit data to the LCD module. BLUE 0 - internally shorted to B5 due to SH7727 only supplying 5 blue pins. (SH7727 pin LCD_D4)
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1. (SH7727 pin LCD_D0)
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2. (SH7727 pin LCD_D2)
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3. (SH7727 pin LCD_D3)
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4. (SH7727 pin LCD_D4)
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5.
61	CF_nCE	O[1]	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word operation to the card.
62	RSVD_1	I	This signal is routed to the onboard CPLD and is reserved for future use.
63	CPLD_GPIO_1	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
65	uP_USB2_nOVR_CRNT	I[1]	Active low. Signals an overcurrent condition on USB host port #2.
66	DGND	I	Digital Ground (0V)
67	uP_USB1_nOVR_CRNT	I[1]	Active low. Signals an overcurrent condition when USB port #1 is configured as host. Signals cable connection when USB port #1 is configured as function.
68	uP_USB2_PWR_EN	O	Active high. Enables power supply for USB host port #2.
69	uP_USB1_PWR_EN	O	Active high. Enables power supply when USB port #1 is configured as host. Enables D+ pullup (TX enable) when USB port #1 is configured as function.
70	uP_USB2_M	I/O	USB port #2 data I/O minus. Route as differential pair with uP_USB2_P.
71	uP_USB2_P	I/O	USB port #2 data I/O plus. Route as differential pair with uP_USB2_M.
72	uP_USB1_M	I/O	USB port #1 data I/O minus. Route as differential pair with uP_USB1_P.
73	uP_USB1_P	I/O	USB port #1 data I/O plus. Route as differential pair with uP_USB1_M.
74	BUFF_nOE	I/O[1]	Active low. Controls the outputs of the buffers on the Card Engine. When low, the buffers are active, when high, the buffers will be tri-stated. This signal is an input while the signal "uP_nBACK" is low.

Pin #	Signal Name	I/O	Description
75	BUFF_DIR_ADDRESS	O	Active high/low. Controls the direction of the address lines through the buffers. When low, the address lines are driven out from the processor (normal condition). When high, the address lines are driven in to the processor (bus mastering). This signal is high while the signal "uP_nBACK" is low.
76	BUFF_DIR_DATA	I/O	Active high/low. Controls the direction of the data lines through the buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). This signal is an input while the signal "uP_nBACK" is low.
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the SH7727-20)
79	POWER_SENSE1	I	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different Card Engines.
80	POWER_SENSE2	I	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different Card Engines.

5.1.3 80-Pin Expansion Connector B (J1B) Pin Descriptions

The table below lists general descriptions for each signal connected to the 80-pin expansion connector B (J1B) on the SH7727-20 Card Engine.

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I[2]	This is the test clock input for the CPLD JTAG port.
2	CPLD_TDO	O[1]	This input transmits data out of the CPLD JTAG port.
3	CPLD_TMS	O[1]	This input indicates the mode of CPLD JTAG port.
4	CPLD_TDI	I[1]	This input receives data on the CPLD JTAB port.
5	uP_nMRD - uP_PCC_nOE	O	Active low. This bufferred signal is the read strobe that latches data output from external peripherals. It is also the PCMCIA OE signal when areas 5 or 6 are accessed in PCMCIA mode.
6	uP_nMWE1 - uP_PCC_nWE - uP_nDQM1	O	Active low. Bufferred write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed).
7	uP_nMWE2 - uP_PCC_nIORD - uP_nDQM2	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
8	uP_nMWE3 - uP_PCC_nIOWR - uP_nDQM3	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
9	DGND	I	Digital Ground (0V)
10	uP_DRAK0 - uP_PCC_RESET	O || O	DMA channel 0 external request acknowledge (active state selectable) || Active high. PCMCIA reset.
11	uP_PCC_nCE1B	O[1]	Active low. Chip/card enable signal for PCMCIA area 6 accesses signifying data bits 0..7 are valid.
12	uP_PCC_nCE2B	O[1]	Active low. Chip/card enable signal for PCMCIA area 6 accesses signifying data bits 15..8 are valid.

Pin #	Signal Name	I/O	Description
13	uP_PCC_nIOIS16	I[1]	Active low. PCMCIA IOIS16 signal. When low, specifies 16 bit IO card or write protected memory-only card.
14	uP_PCC_RDY	I[1]	Active high. PCMCIA RDY signal. PCMCIA/CF card will hold this signal low until ready to be accessed. Also used as IREQ for IO cards.
15	uP_PCC_nWAIT	I[1]	Active low. PCMCIA WAIT signal. Has same effect of holding the current bus cycle that uP_WAIT# has.
16	uP_PCC_BVD2	I[1]	PCMCIA BVD2 signal.
17	uP_PCC_BVD1	I[1]	PCMCIA BVD1 singal.
18	uP_PCC_nCD2	I[1]	Active low. PCMCIA CD2 signal. Signals that one side of the PCMCIA/CF card is connected.
19	uP_PCC_nCD1	I[1]	Active low. PCMCIA CD1 signal. Signals that one side of the PCMCIA/CF card is connected.
20	uP_PCC_nREG	O[1]	Active low. PCMCIA REG signal. When asserted, this signal specifies accesses to card attribute memory.
21	DGND	I	Digital Ground (0V)
22	uP_PCC_VS1	I[1]	PCMCIA VS1 signal. Voltage sense.
23	uP_PCC_VS2	I[1]	PCMCIA VS2 signal. Voltage sense.
24	uP_DACK0 - uP_PCC_nDRV	O || O[1]	DMA channel 0 acknowledge (active state selectable) || Active low. PCMCIA drive enable (can use for power and PMCIA buffer control).
25	uP_SH_nWR	O	Active low. When low, this un-buffered signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal can be used for PCMCIA buffer direction control.
26	uP_nMWE3 - uP_PCC_nIOWR - uP_nDQM3	O	Active low. Buffered write enable for buffered data bus bits 31->24 - PCMCIA IOWR - DQM3 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
27	uP_nMWE2 - uP_PCC_nIORD - uP_nDQM2	O	Active low. Buffered write enable for buffered data bus bits 23->16 - PCMCIA IORD - DQM2 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed)
28	uP_nMWE1 - uP_PCC_nWE - uP_nDQM1	O	Active low. Bufferred write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1 SDRAM signal from the LSH7727. All functions are valid (functionality changes based on memory area accessed).
29	uP_nMWE0 - uP_nDQM0	O	Active low. Buffered write enable for buffered data bus bits 7->0 - DQM0 SDRAM signal from the LSH7727. Both functions are valid (functionality changes based on memory area accessed)
30		NC	No internal connection (not implemented on the SH7727-20)
31		NC	No internal connection (not implemented on the SH7727-20)
32	DGND	I	Digital Ground (0V)
33		NC	No internal connection (not implemented on the SH7727-20)
34		NC	No internal connection (not implemented on the SH7727-20)
35		NC	No internal connection (not implemented on the SH7727-20)
36		NC	No internal connection (not implemented on the SH7727-20)

Pin #	Signal Name	I/O	Description
37		NC	No internal connection (not implemented on the SH7727-20)
38		NC	No internal connection (not implemented on the SH7727-20)
39		NC	No internal connection (not implemented on the SH7727-20)
40		NC	No internal connection (not implemented on the SH7727-20)
41		NC	No internal connection (not implemented on the SH7727-20)
42		NC	No internal connection (not implemented on the SH7727-20)
43		NC	No internal connection (not implemented on the SH7727-20)
44	DGND	I	Digital Ground (0V)
45		NC	No internal connection (not implemented on the SH7727-20)
46		NC	No internal connection (not implemented on the SH7727-20)
47		NC	No internal connection (not implemented on the SH7727-20)
48	MFP9 - uP_AFE_TX - PTM5	O || I	AFE serial transmit data || General purpose input only pin PTM5.
49	MFP10 - uP_AFE_RX - PTM6	I || I	AFE serial receive data || General purpose input only pin PTM6.
50	MFP11 - uP_AFE_FSYNC - PTM7	I || I	AFE frame sync. || General purpose input only pin PTM7.
51	MFP12 - uP_AFE_nRDET - PTM5	I || I	AFE ringing detection || General purpose input only pin PTM5.
52	MFP13 - uP_AFE_SCLK	I[1]	AFE input clock.
53	MFP14 - uP_AFE_nRLYCNT - PTK1	O || I/O	Active low. AFE relay control. || General purpose I/O PTK1.
54	MFP15 - uP_AFE_HC - PTK0	O || I/O	AFE hardware control signal. || General purpose I/O PTK0.
55	DGND	I	Digital Ground (0V)
56	MFP16 - uP_nADTRG	I[1]	Active low analog trigger. Interruptible signal forcing A/D capture if configured.
57		NC	No internal connection (not implemented on the SH7727-20)
58	MFP18 - uP_COTXD	I/O	SIOF serial transmit data. This signal is attached to the on-board CODEC, but may be used to communicate to an off-board CODEC if the on-board one is not populated.
59	MFP19 - uP_CORXD	I/O	SIOF serial receive data. This signal is attached to the on-board CODEC, but may be used to communicate to an off-board CODEC if the on-board one is not populated.
60	MFP20 - uP_COSYNC	I/O	SIOF serial frame sync signal. This signal is output in master mode and input in slave mode. This signal is attached to the on-board CODEC, but may be used to communicate to an off-board CODEC if the on-board one is not populated.

Pin #	Signal Name	I/O	Description
61	MFP21 - uP_COSCK	I/O	SIOF serial communications clock. This signal is output in master mode and input in slave mode. This signal is attached to the on-board CODEC, but may be used to communicate to an off-board CODEC if the on-board one is not populated.
62	MFP22 - CODEC_CLK	I/O	This signal is the master CODEC clock frequency and is typically output from the Card Engine. If the Card Engine configuration without the internal CODEC is used, this signal must be generated externally as an input to the Card Engine if an external CODEC is being used.
63	MFP23 - CODEC_OVRLD - PTG4	O || I	Active high. Signals that the output of the CODEC is within 1dB of the rails. || If the on-board CODEC is not populated, this signal may be used as a general purpose input-only pin PTG4.
64	MFP24 - CPLD_GPIO_3	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
65	MFP25 - CPLD_GPIO_4	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
66	DGND	I	Digital Ground (0V)
67	MFP26 - CPLD_GPIO_5	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
68	MFP27 – uP_nCS3	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
69	MFP28 - CPLD_GPIO_7	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
70	MFP29 – uP_CKE	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
71	MFP30 - PCC_nCE2A - PTE4	O || I/O[1]	Active low. Chip/card enable signal for PCMCIA area 5 accesses signifying data bits 15..8 are valid. || General purpose I/O PTE4
72	MFP31 – VIDEO_nMCS	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See CPLD description doc.
73	MFP32 – CPLD_GPIO_9	I/O	No internal connection (not implemented on the SH7727-20)
74	MFP33 – CPLD_GPIO_6	I/O	No internal connection (not implemented on the SH7727-20)
75	MFP34 – CPLD_GPIO_8	NC	No internal connection (not implemented on the SH7727-20)
76		NC	No internal connection (not implemented on the SH7727-20)
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the SH7727-20)
79		NC	No internal connection (not implemented on the SH7727-20)
80		NC	No internal connection (not implemented on the SH7727-20)

[1] Has 10K pull up resistor to 3.3V on the Card Engine
[2] Has 10K pull down resistor to ground on the Card Engine

5.2 Pin Multiplexing and Initialization Tables

5.2.1 144-Pin SODIMM (J1C) Connector Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 144-pin SODIMM connector (J1C) on the SH7727-20 Card Engine (if any).

Pin #	Signal Name	Alternate Uses	Alternate Use Description	Initial State
8	SLOW_nMCS	PCC_CE1A	Active low buffered chip/card enable signal for PCMCIA slot 2 (area 5 accesses) signifying data bits 7..0 are valid. Use with MFP30 uP_PCC_nCE2A - PTE4 while PC0USE bit is disabled. Must externally control all interface signals other than bus control for both slots when using this mode. Contact Logic for additional information.	Output High
10	VIDEO_nMCS	SDRAM_EXP	Active low buffered chip select for area 2 of SH7727 memory. This chip select is capable of controlling additional external SDRAM.	Output High
11	ETHER_nACT_LED	nLEDA	Active low open drain output. 24mA sink. This output may be configured to indicate a variety of network states. This signal may be connected directly to an external LED. See SMSC91C111 data sheet for details.	Open Drain
13	ETHER_nLNK_LED	nLEDB	Active low open drain output. 24mA sink. This output may be configured to indicate a variety of network states. This signal may be connected directly to an external LED. See SMSC91C111 data sheet for details.	Open Drain
23	uP_IRQD	PTF3	Digital input-only pin.	Input
25	uP_IRQC	PTH4	Digital input-only pin.	Input
26	uP_TEST2	PTG5	Digital input-only pin. Cannot be used (disabled) when E10A emulator connected.	Input
27	uP_IRQB	PTH3	Digital input-only pin.	Input
28	uP_TRST	PTF7	Digital input-only pin. Cannot be used (disabled) when E10A emulator connected.	Input
	uP_TRST	PINT15	Port interrupt pin. Cannot be used (disabled) when E10A emulator connected.	Input
29	uP_IRQA	PTH0	Digital input-only pin.	Input
30	uP_TMS	PTF6	Digital input-only pin. Cannot be used (disabled) when E10A emulator connected.	Input
	uP_TMS	PINT14	Port interrupt pin. Cannot be used (disabled) when E10A emulator connected.	Input
32	uP_TD0	PTE0	Digital input/output pin. Cannot be used (disabled) when E10A emulator connected.	Input
34	uP_TDI	PTF5	Digital input-only pin. Cannot be used (disabled) when E10A emulator connected.	Input
	uP_TDI	PINT13	Port interrupt pin. Cannot be used (disabled) when E10A emulator connected.	Input
36	uP_TCK	PTF4	Digital input-only pin. Cannot be used (disabled) when E10A emulator connected.	Input
	uP_TCK	PINT12	Port interrupt pin. Cannot be used (disabled) when E10A emulator connected.	Input
41	uP_UARTA_CTS	IRQ5	Dedicated interrupt pin.	Input
		SCPT7	Digital input-only pin.	Input
43	uP_UARTA_TX	SCPT4_OUT	SCPT bit 4 output pin (digital output-only).	Output High

Pin #	Signal Name	Alternate Uses	Alternate Use Description	Initial State
45	uP_UARTA_RX	SCPT4_IN	SCPT bit 4 input pin (digital input-only).	Input
48	uP_DREQ0	PTD4	Digital input-only pin.	Input
51	nSUSPEND	AN6	Analog input-only pin. May only be used in this manner if the installed software does not use this pin to determine the reason for an NMI interrupt.	Input
	nSUSPEND	DA1	Analog DAC signal. 8 bit resolution.	Input
	nSUSPEND	PTL6	Digital input-only pin. May only be used in this manner if the installed software does not use this pin to determine the reason for an NMI interrupt.	Input
65	uP_SPI_FRM	PTJ1	Digital input/output pin.	Output High
67	uP_SPI_MOSI_TX	SCPT0_OUT	SCPT bit 0 output pin (digital output-only)	Output High
	uP_SPI_MOSI_TX	UARTB_TX	UARTB TX (TXD0) signal - may be configured as a UART tx pin only if the on-board CODEC is not used.	Output High
69	uP_SPI_MISO_RX	SCPT0_IN	SCPT bit 0 input pin (digital input-only).	Input
	uP_SPI_MISO_RX	UARTB_RX	UARTB RX (RXD0) signal - may be configured as a UART rx pin only if the on-board CODEC is not used.	Input
71	uP_SPI_SCK	SCPT1	Digital input/output pin.	Output High

5.2.2 80-Pin Expansion Connector A (J1A) Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 80-pin expansion connector A (J1A) on the SH7727-20 Card Engine.

Pin #	Signal Name	Alternate Uses	Alternate Use Description	Initial State
1	LCD_VSYNC	PTE3	Digital input/output pin.	Output High
2	LCD_HSYNC	PTD5	Digital input/output pin.	Output High
3	LCD_DCLK	PTH7	Digital input/output pin.	Output High
4	LCD_DON	PTD7	Digital input/output pin.	Output High
5	LCD_MDISP	PTE6	Digital input/output pin.	Output High
17	uP_STATUS_1	PTJ6	Digital input/output pin.	Output High
18	uP_STATUS_2	PTJ7	Digital input/output pin.	Output High
25	A/D1	PTL4	Digital input-only pin.	Input
36	TOUCHY	AN3	Analog input pin (ADC). May only be used on Card Engines for which the touch circuit is not populated.	Input
	TOUCHY	PTL3	Digital input-only pin. May only be used on Card Engines for which the touch circuit is not populated.	Input
38	TOUCHX	AN2	Analog input pin (ADC). May only be used on Card Engines for which the touch circuit is not populated.	Input
	TOUCHX	PTL2	Digital input-only pin. May only be used on Card Engines for which the touch circuit is not populated.	Input
42	R1	PTC7	Digital input/output pin.	Output High
	R1	PINT3	Port interrupt pin.	Output High
43	R2	PTM0	Digital input-only pin.	Output High
45	R3	PTM1	Digital input-only pin.	Output High
	R3	PINT8	Port interrupt pin.	Output High
46	R4	PTM2	Digital input-only pin.	Output High
	R4	PINT9	Port interrupt pin.	Output High
47	R5	PTM3	Digital input-only pin.	Output High
	R5	PINT10	Port interrupt pin.	Output High

Pin #	Signal Name	Alternate Uses	Alternate Use Description	Initial State
48	G0	PTC3	Digital input/output pin.	Output High
49	G1	PTD2	Digital input/output pin.	Output High
50	G2	PTD3	Digital input/output pin.	Output High
51	G3	PTC4	Digital input/output pin.	Output High
	G3	PINT0	Port interrupt pin.	Output High
52	G4	PTC5	Digital input/output pin.	Output High
	G4	PINT1	Port interrupt pin.	Output High
53	G5	PTC6	Digital input/output pin.	Output High
	G5	PINT2	Port interrupt pin.	Output High
56	B1	PTD0	Digital input/output pin.	Output High
57	B2	PTD1	Digital input/output pin.	Output High
58	B3	PTC0	Digital input/output pin.	Output High
59	B4	PTC1	Digital input/output pin.	Output High
60	B5	PTC2	Digital input/output pin.	Output High
68	UP_USB2_PWR_EN	PTE1	Digital input/output pin.	Input
69	UP_USB1_PWR_EN	PTE2	Digital input/output pin.	Output High

5.2.3 80-Pin Expansion Connector B (J1B) Pin Multiplexing and Initialization Descriptions

The table below lists secondary functions and expected software initialization state for each signal connected to the 80-pin expansion connector B (J1B) on the SH7727-20 Card Engine.

Pin #	Signal Name	Alternate Uses	Alternate Use Description	Initial State
11	uP_PCC_nCE1B	uP_CS6	Active low area 6 chip select signal when not in PCMCIA mode.	Output High
12	uP_PCC_nCE2B	PTE5	Digital input/output pin.	Output High
13	uP_PCC_nIOIS16	PTG7	Digital input-only pin.	Input
14	uP_PCC_RDY	PTE7	Digital input/output pin.	Input
15	uP_PCC_nWAIT	PTH6	Digital input-only pin.	Input
16	uP_PCC_BVD2	PTG3	Digital input-only pin.	Input
17	uP_PCC_BVD1	PTG2	Digital input-only pin.	Input
18	uP_PCC_nCD2	PTG1	Digital input-only pin.	Input
19	uP_PCC_nCD1	PTG0	Digital input-only pin.	Input
20	uP_PCC_nREG	PTF2	Digital input-only pin.	Output High
22	uP_PCC_VS1	PTF1	Digital input-only pin.	Input
23	uP_PCC_VS2	PTF0	Digital input-only pin.	Input
48	MFP9 - uP_AFE_TX - PTM5	PINT5	Port interrupt pin.	Input
49	MFP10 - uP_AFE_RX - PTM6	PINT6	Port interrupt pin.	Input
50	MFP11 - uP_AFE_FSYNC - PTM7	PINT7	Port interrupt pin.	Input
51	MFP12 - uP_AFE_nRDET - PTM5	PINT4	Port interrupt pin.	Input
56	MFP16 - uP_nADTRG	PTH5	Digital input-only pin.	Input
58	MFP18 - uP_COTXD	SCPT2_OUT	SCPT bit 2 output pin (digital output-only).	Output High
59	MFP19 - uP_CORXD	SCPT2_IN	SCPT bit 2 input pin (digital input-only).	Input
60	MFP20 - uP_COSYNC	SCPT6	Digital input/output pin.	Output High
61	MFP21 - uP_COSCK	SCPT5	Digital input/output pin.	Output High

6 Mechanical Specifications

6.1 Interface Connectors

The SH7727-20 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B). The 80-pin expansion connectors must have a 3mm board-to-board mating height, and the SODIMM must have a 3.7mm mating height (2.9mm board-to-board).

IMPORTANT NOTE: Do not place any components underneath the Card Engine on the same side of the board as the connectors. Some components on the Card Engine take advantage of the full mating height and their locations are subject to change as the board is revised. If the design requires that components be placed underneath the Card Engine, contact Logic Product Development for assistance.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

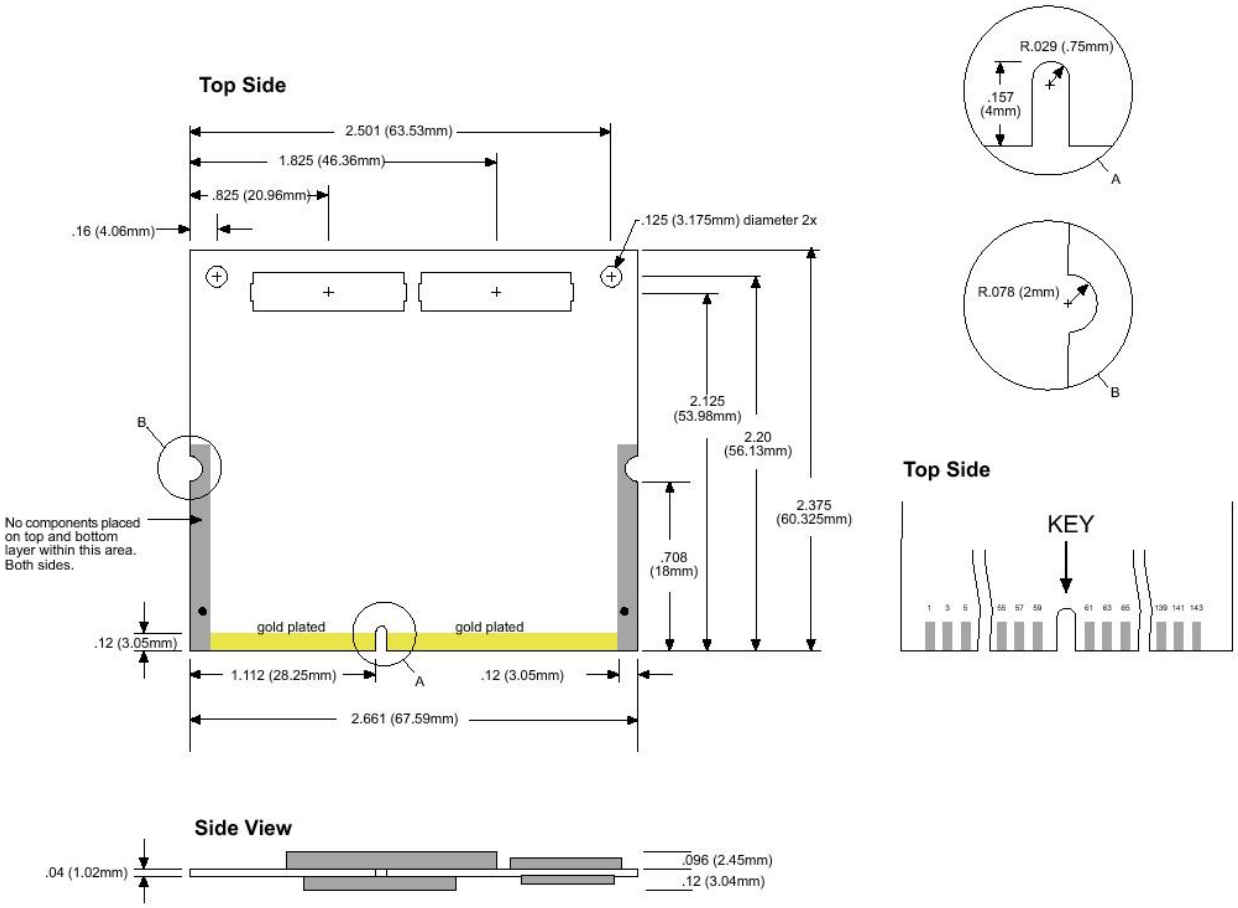


Figure 6.1: Card Engine Mechanical Drawing

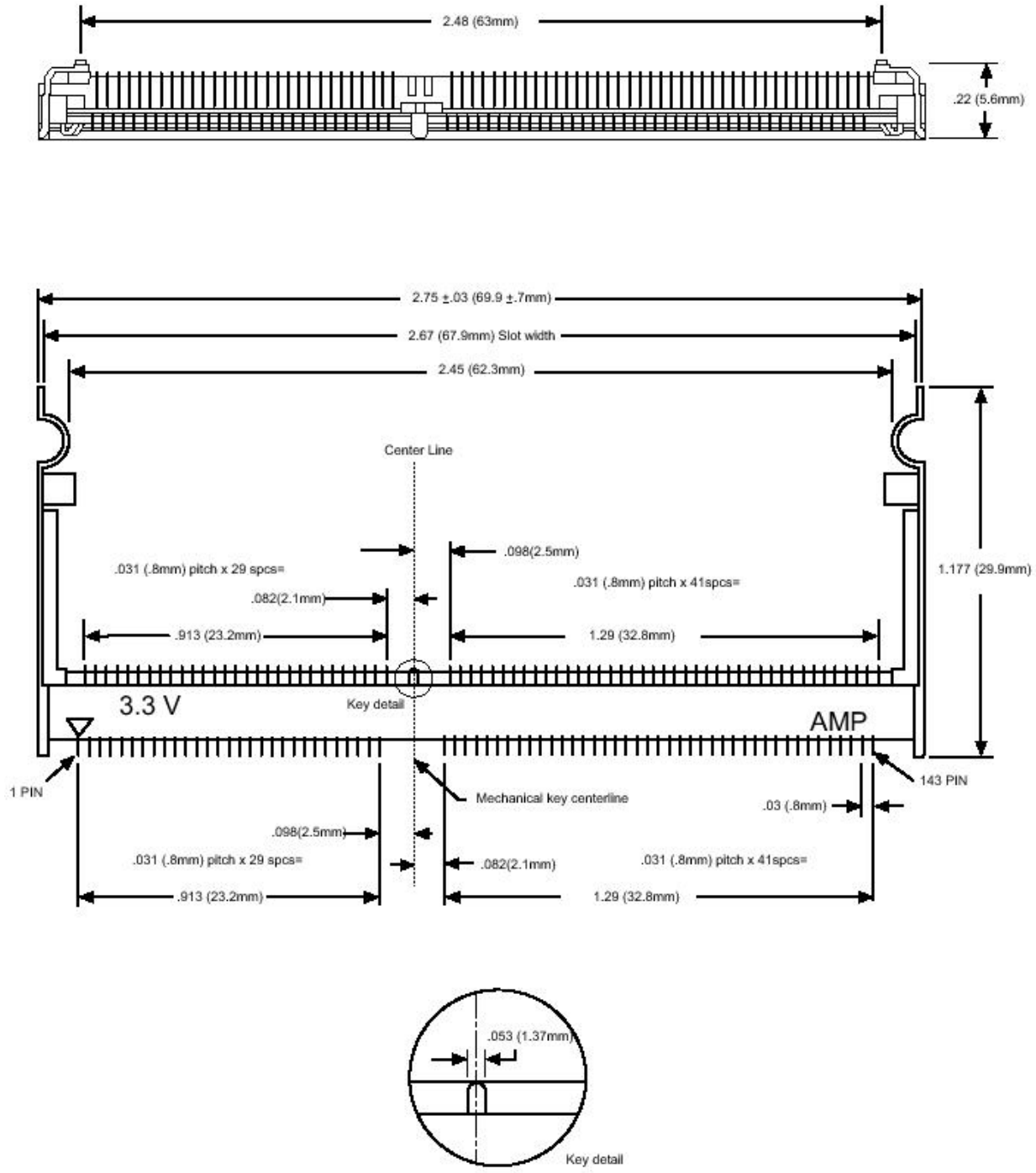


Figure 6.2: SODIMM Connector Specification

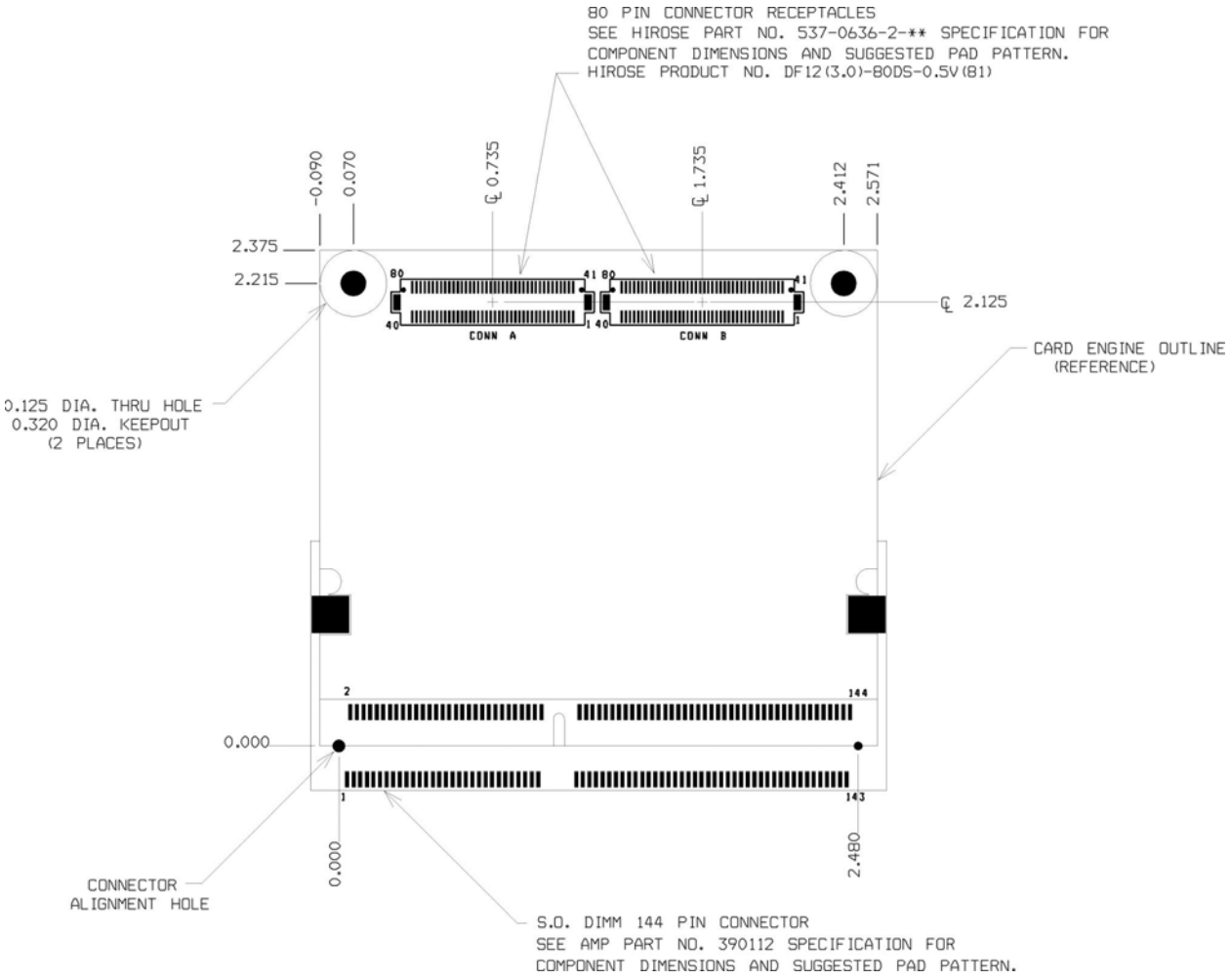


Figure 6.3: Recommended PCB Layout

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