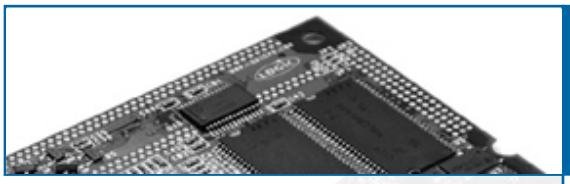
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Zoom™

Card Engine

LH75401-10/11 Card Engine
IO Controller Specification

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REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CPLD	APPROVAL	DATE
A	Matthew Tilstra	Release	--	MT	4-28-03
B	James Wicks	Section 3.1.10 correction; edit	--	JW	10/28/03
C	Erik Reynolds, Michael Anderson, James Wicks	Section 3.1.11; Edit to be compatible with the LH75401-11 Release	--	ECR	01/14/04
D	James Wicks, Jed Anderson	Section 4.6 Created into an Application Note; Format, Pin Description Update; Added note to reference App Note 303 in Section 4.	REV 1.4	ECR	01/16/06

Please check www.logicpd.com for the latest revision of this manual, errata's, and additional application notes.

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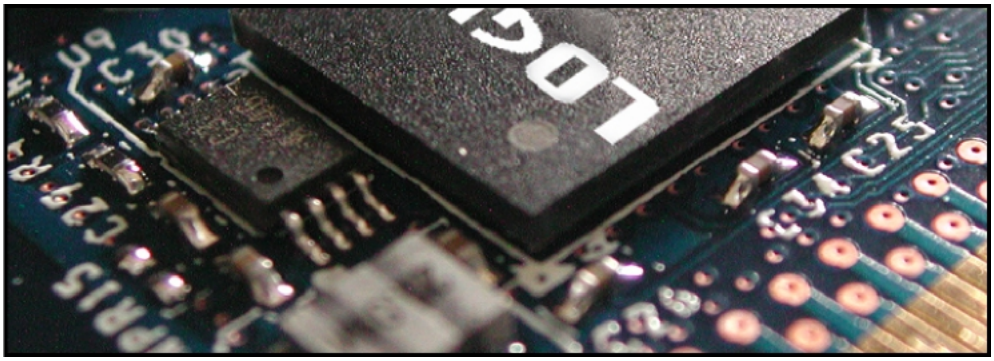
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1 Introduction

1.1 Product Brief

Logic offers production-ready I/O controller devices and design packages for customers creating custom Card Engine designs and CPLD code for the LH75401 Card Engine. Logic has optimized the VHDL code to fit in the smallest possible programmable logic device. This results in an embedded product development cycle with **less time, less cost, less risk ... more innovation.**



- **I/O Controller was written in VHDL and contains the following:**
  - I2S (8-bit stereo audio interface, includes DMA)
  - SPI (parallel to SPI interface)
  - ISA-like bus interface
  - SMSC LAN91C111 wired LAN bus interface and power control logic
  - Buffer control logic
  - Chip select decoder logic
  - Interrupt encoder logic
  - Flash program control logic
  - Processor mode control logic
  - IC code revision register
  - I2S interface to the CODEC 8-bit audio
- **Source Code**
  - Includes all VHDL code (licensable .vhd source code files)
- **Support**
  - VHDL IP Core Source Code Design Package includes the Bronze level support package

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2 Acronyms

CS	Chip Select
IRQ	Interrupt Request
MB	Megabyte (2^20 bytes)
ISA	Industry Standard Architecture

2.1 Technical Specifications

Please refer to the following component specifications and data sheets.

Altera MAX 7000A PLD data sheet (EPM7128A)
Altera Device Package Information data sheet
Texas Instruments TLV320DAC23 data manual

2.2 IO Controller Advantages

Some of the key features in the IO Controller include:

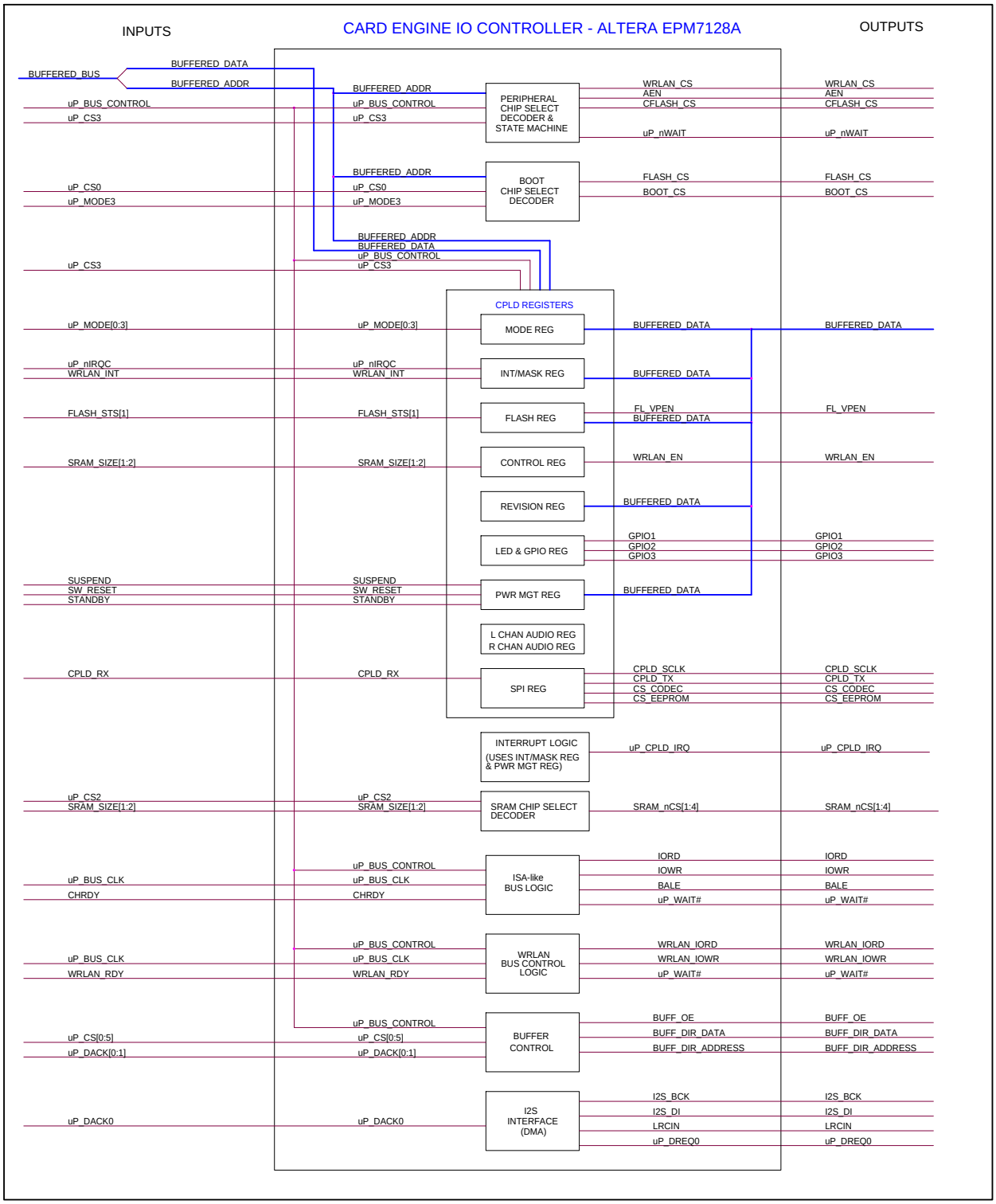
- Parallel to I2S Audio Interface with DMA
- Parallel to SPI Interface
- Chip Select Decoder
- Interrupt Decoder
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player

The IO Controller VHDL source code is available for purchase. Contact Logic for more information.

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2.3 IO Controller Block Diagram

Figure 2.1: IO Controller Block Diagram



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3 IO Controller Address and Register Definitions

Address Range	Mem Block Description	Size
0x4C00 0000 – 0x4CFF FFFF	Processor Chip Select 3 (CS3)	16MB

3.1 Processor Chip Select 3 (CS3)

Address Range	Mem Block Description	Size
0x4C00 0000 – 0x4C07 FFFF	Wired LAN Chip Select	512KB
0x4C08 0000 – 0x4C0F FFFF	Card Engine Control Reg	512KB
0x4C10 0000 – 0x4C17 FFFF	CODEC I2S Audio	512KB
0x4C18 0000 – 0x4C1F FFFF	Reserved	512KB
0x4C20 0000 – 0x4C27 FFFF	Reserved	512KB
0x4C28 0000 – 0x4C2F FFFF	SPI Reg	512KB
0x4C30 0000 – 0x4C37 FFFF	Interrupt/Mask Reg	512KB
0x4C38 0000 – 0x4C3F FFFF	Mode Reg	512KB
0x4C40 0000 – 0x4C47 FFFF	Flash Reg	512KB
0x4C48 0000 – 0x4C4F FFFF	Power Management Reg	512KB
0x4C50 0000 – 0x4C57 FFFF	IO Controller Code Revision Reg	512KB
0x4C58 0000 – 0x4C5F FFFF	GPIO Reg	512KB
0x4C60 0000 – 0x4C67 FFFF	Reserved	512KB
0x4C68 0000 – 0x4C6F FFFF	Reserved	512KB
0x4C70 0000 – 0x4C77 FFFF	CF Chip Select	512KB
0x4C78 0000 – 0x4C7F FFFF	ISA-like Bus Chip Select	512KB

Each memory block for chip select 3 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

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3.1.1 Wired LAN Chip Select

Address Range: 0x4C000000 – 0x4C07FFFF

- This area of memory is used when accessing the wired LAN chip (internal registers/memory).

3.1.2 Card Engine Control Register

Address: 0x4C080000

- This register is used for enabling/disabling power to the on-board wired LAN chip and for software to determine the amount of external SRAM available.

7	6	5	4	3	2	1	0	
S1	S2	-	-	-	-	-	WLPE	
-	-	-	-	-	-	-	0	Reset
R	R	-	-	-	-	-	R/W	R/W

S1:S2: SRAM Size bits
00 = 256 KB
01 = 512 KB
10 = 1 MB
11 = 2 MB

WLPE: wired LAN power enable signal.
0 = Wired LAN enabled
1 = Wired LAN disabled

3.1.3 CODEC I2S Audio

The I2S core uses this area of memory. The I2S core is used when interfacing to the TI CODEC, and supports AUDIO OUT only. See Section 4.6 for more information regarding the CODEC I2S Interface.

Address: 0x4C100000

15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
L7 (MSB) …. L0 (LSB)	R7 (MSB) …. R0 (LSB)	
0x00	0x00	Reset
W	W	R/W

L7:L0 Left Channel playback data
R7:R0 Right Channel playback data

3.1.4 Reserved Memory Block

Address Range: 0x4C18 0000 – 0x4C27 FFFF

- These memory blocks are reserved for future use.

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3.1.5 SPI Interface Register

Address: 0x4C28 0000

- This register holds SPI data during a read/write between the processor and on-board EEPROM and CODEC. The SPI interface used is implemented by the processor and not the IO Controller.

7	6	5	4	3	2	1	0	
-	-	-	CDCS	EECS	EECK	EETX	EERX	
-	-	-	0	0	0	0	-	Reset
-	-	-	R/W	R/W	R/W	R/W	R	R/W

CDCS: CODEC chip select.
0 = not selected
1 = DAC chip selected
EECS: EEPROM chip select.
0 = not selected
1 = EEPROM chip selected
EECK: EEPROM spi clock.
EETX: EEPROM spi data transmit.
EERX: EEPROM spi data receive.

3.1.6 Interrupt/Mask Register

Address: 0x4C30 0000

- This register contains the information used by the IO Controller to generate an interrupt to the processor.

7	6	5	4	3	2	1	0	
uP_nIRQCMSK	uP_nIRQC	-	-	-	WMSK	-	WIRQ	
0	-	-	-	-	0	-	-	Reset
R/W	R	-	-	-	R/W	-	R	R/W

uP_nIRQCMSK: Interrupt C input Mask
0 = interrupt not masked
1 = interrupt masked
uP_nIRQC: Interrupt C input to Card Engine
0 = interrupt
1 = no interrupt
WMSK: wired LAN chip interrupt mask.
0 = interrupt not masked
1 = interrupt masked
WIRQ: wired LAN chip interrupt request (IRQ).
0 = interrupt
1 = no interrupt

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3.1.7 Mode Register

Address: 0x4C38 0000

- This register holds the values of the mode pins.

7	6	5	4	3	2	1	0	
-	-	-	-	MDP3	MDP2	MDP1	MDP0	
-	-	-	-	-	-	-	-	Reset
-	-	-	-	R	R	R	R	R/W

MDP3: mode pin 3. Mode pin 3 determines the boot source. See Section 4.2 for more information on Mode pin 3.
0 = area/bank 0 will activate BOOT_nCS for boot from off-board memory.
1 = area/bank 0 will activate FLASH_nCS for boot from on-board flash.
MDP2: mode pin 2.
0 = undefined
1 = undefined
MDP1: mode pin 1.
0 = undefined
1 = undefined
MDP0: mode pin 0.
0 = Area/Bank 0 will be 8-bit width at boot
1 = Area/Bank 0 will be 16-bit width at boot

3.1.8 Flash Register

Address: 0x4C40 0000

- This register holds status information for the flash.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	FST1	FPEN	
-	-	-	-	-	-	-	0	Reset
-	-	-	-	-	-	R	W	R/W

FST1: flash status pin. This is the flash RY/BY# pin.
0 = flash busy
1 = flash ready
FPEN: flash program enable.
0 = normal flash operations
1 = program flash enabled

3.1.9 Power Management Register

Address: 0x4C48 0000

- This register holds the values of the power management pins. If any one of these signals is active (logic low), an interrupt will be generated to the processor.

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7	6	5	4	3	2	1	0	
-	-	-	-	-	SUSPEND	SW_RESET	STANDBY	
-	-	-	-	-	-	-	-	Reset
-	-	-	-	-	R	R	R	R/W

SUSPEND
0 = Signal is active
1 = Signal is inactive
RESET
0 = Signal is active
1 = Signal is inactive
STANDBY
0 = Signal is active
1 = Signal is inactive

3.1.10 IO Controller Code Revision Register

Address: 0x4C50 0000

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								Reset
R								R/W

3.1.11 GPIO Register

Address: 0x4C58 0000

- This register controls data for CPLD general purpose pins.

7	6	5	4	3	
GPDIR3	GPDIR2	-	-	CPLD_GPIO_3_DATA	
0	0	-	-	0	Reset
R/W	R/W	-	-	R/W	R/W

2	1	0	
CPLD_GPIO_2_DATA	-	CPLD_GPIO_1_DATA	
0	-	1	Reset
R/W	-	W	R/W

GPDIR3: MFP21-CPLD_GPIO_3 Direction Control
0 = output
1 = input

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GPDIR2: CPLD_GPIO_2 Direction Control
0 = output
1 = input

CPLD_GPIO_3_DATA: MFP21-CPLD_GPIO_3 Data bit
On write – sets value of pin if pin is an output
On read – returns value of pin

CPLD_GPIO_2_DATA: CPLD_GPIO_2 Data bit
On write – sets value of pin if pin is an output
On read – returns value of pin

CPLD_GPIO_1_DATA: CPLD_GPIO_1 Data bit. This signal is output only. Note: Application board LED signal.
0 = Sets value of pin to 0. (turn led on)
1 = Sets value of pin to 1. (turn led off)

3.1.12 Reserved Memory Block

Address Range: 0x4C60 0000 – 0x4C67 FFFF

- This memory block is reserved for future use.

3.1.13 Reserved Memory Block

Address Range: 0x4C68 0000 – 0x4C6F FFFF

- This memory block is reserved for future use.

3.1.14 CompactFlash (CF) Chip Select

Address Range: 0x4C70 0000 – 0x4C77 FFFF

- This area of memory is used when accessing off-board CompactFlash.

3.1.15 ISA-like Bus Chip Select

Address Range: 0x4C78 0000 – 0x4C7F FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 5 for read and write timing diagrams.

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4 IO Controller Functions

This section describes in detail the different IO Controller function blocks. See Section 2.3 for the IO Controller block diagram.

Note: A specific software protocol must be followed to access IO devices on Sharp Card Engines. Please see Logic's Application Note 303: *Interfacing to IO Devices via the Static Memory Controller on LH7xxxx Card Engines* for examples of the protocol when accessing registers within the CPLD. This document can be found at: http://www.logicpd.com/auth/.

4.1 Chip Select Decoder Logic

This logic decodes processor chip select into smaller segments of memory. See Section 3.1 for the chip select 3 memory map.

4.2 Boot Chip Select Decoder Logic

The card engine can boot from on-board flash or an off-board EPROM (planned for a future application board). The boot device is determined by a jumper setting (mode pin 3) on the application board. When mode pin 3 is a 1, the on-board flash is selected for boot (bank 0 and CS0), and when mode pin 3 is a 0, the off-board EPROM is selected for boot. This logic implements the following table.

FLASH	EPROM	Mode Pin 3	Function
CS0	--	1	Boot from Flash (bank 0)
--	CS0	0	Boot from EPROM (bank 0),

4.3 ISA-like Bus Logic

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic shifts the falling edge of the read and write signals (from the processor) to meet ISA timing. Since the LH75401-10/11 does not have an external bus clock signal available, an external 25MHz clock source is used to generate the timing for the ISA signals. The IO controller will hold-off the processor by asserting nWAIT while the ISA transaction finishes. It is essential that devices on the ISA-like bus be re-chip-selected every time they are accessed. Burst operations or continuous reads (reads where the device remains selected and only the address changes to read the next location) are not supported for the ISA-like bus. See Section 5 for sample read and write ISA-like timing diagrams and a description of how the timing is derived.

Note: The current card engine configuration only implements CompactFlash on this bus, and does not have an ISA device connected to the bus.

4.4 Wired LAN Bus Logic

This logic shifts the falling edge of the read and write signals (from the processor) to meet the required Wired LAN timing. The rising edge is not changed.

4.5 Buffer Control Logic

This logic controls the output enable and direction of the on-board buffers.

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4.6 CODEC I2S Interface

See Logic's LH75401-10/11 "Application Note: Communicating to the CODEC via I2S" in order to communicate to the CODEC via I2S. See the Texas Instruments TLV320DAC23 data sheet for the complete command set and registers.

4.7 Interrupt Logic

This logic generates the processor's IRQ2, from information in the Interrupt/Mask register or if any of the power management signals are low. See Section 3.1.6 for a detailed description of the Interrupt/Mask register and Section 3.1.9 for the Power Management Register.

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5 ISA Timing Diagrams

5.1 Notes on LH75401-10/11 ISA-like timing

Since the LH75401 does not have an external bus clock signal available, an external 25MHz clock source is used to generate the timing for the ISA signals. When the IO controller sees the uP access the CF_CE or the AEN memory space, it will start a counter based on the 25MHz clock to control the timing of the ISA transaction. Once the counter starts, the IO controller will hold-off the processor by asserting nWAIT while the ISA transaction finishes. The ISA signals will change on the rising edge of the 25MHz clock with the change in value of the ISA control counter. In the timing diagrams below, the corresponding count value is shown by each edge of the ISA signals. For timing of the LH75401 signals and nWAIT controlled access, please see the latest LH75401 datasheet.

Note that for the read operation, the use of buffers with bus-hold circuitry is required. The ISA device will put its data on the bus while nIORD is low, and sometime after nIORD goes high, it will tristate its output drivers. The LH75401 will read the data off of the bus on the rising edge of the LH75401 internal HCLK before the LH75401 CS is brought high. The bus-hold circuitry of the buffers will keep the ISA read data on the bus during this time, ensuring the processor gets a valid read.

5.2 ISA-like Bus, Read Cycle Timing Diagram

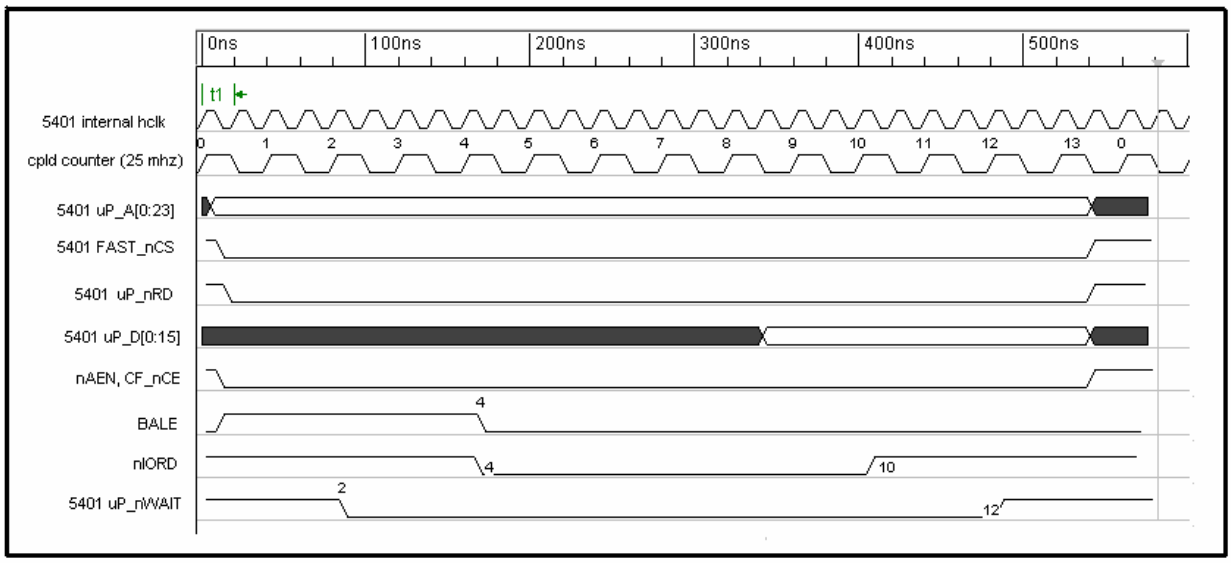


Figure 5.1: ISA-like Bus, Read Cycle Timing

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5.3 ISA-like Bus, Write Cycle Timing Diagram

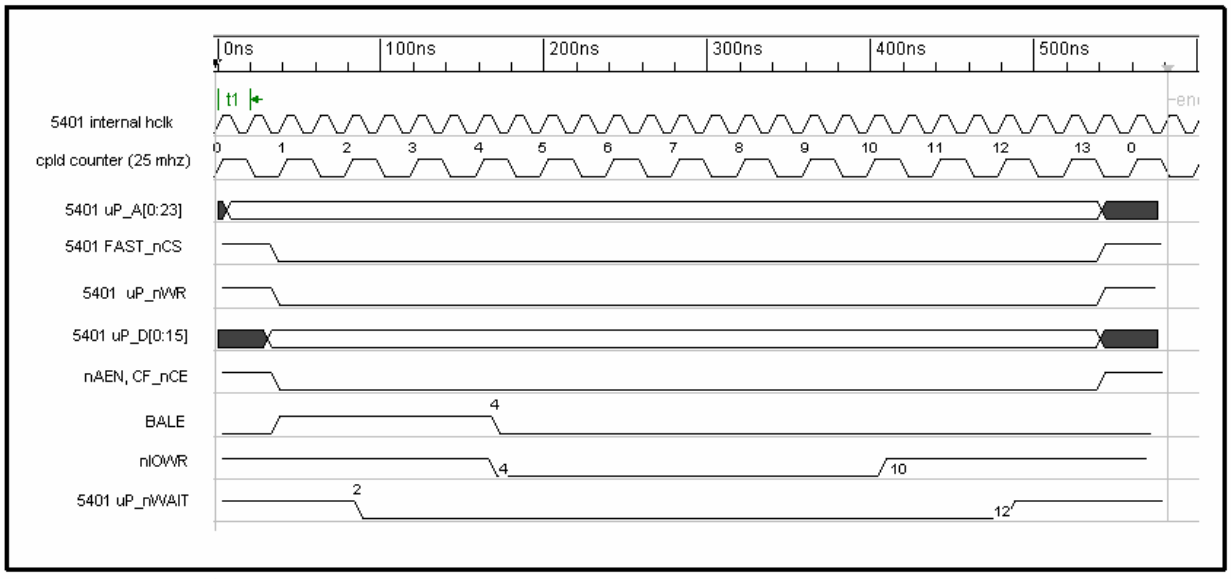


Figure 5.2: ISA-like Bus, Write Cycle Timing

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6 IO Controller Pin Information

Pin	Signal Name	Input/Output
C7	nAEN	Output
A7	BALE	Output
B1	BOOT_nMCS	Output
B10	BUFF_DIR_DATA	Output
C9	BUFF_nOE	Output
K10	RSVD_1	Output
K9	CF_nCE	Output
B7	nCHRDY	Input
B4	CPLD_CS_CODEC	Output
C5	CPLD_CS_EEPROM	Output
A2	FAST_nCS	Input
E8	FLASH_STS1	Input
G1	FL_VPEN	Output
B2	FLASH_nCS	Output
K2	CPLD_GPIO1	Output
F10	CPLD_GPIO2	Input
E3	MFP21-CPLD_GPIO3	Output
F7	I2S_BCK	Input
E9	I2S_DI	Output
B8	nIORD	Output
A8	nIOWR	Output
E10	LRCIN	Input
B5	MSTR_RST	Output
F4	CPLD_SCLK	Output
E1	CPLD_RX	Input
E2	CPLD_TX	Output
B3	SRAM_SIZE_1	Input
C4	SRAM_SIZE_2	Input
J4	SRAM_nCS	Input
F2	SRAM_nCS1	Output
K4	SRAM_nCS2	Output
E7	SRAM_nCS3	Output
C10	SRAM_nCS4	Output
J2	nSTANDBY	Input
K3	nSUSPEND	Input
J3	uP_SW_nRESET	Input
F1	VIDEO_nCS	Input
A4	WRLAN_CS	Output
G3	WRLAN_ENABLE	Output
H5	WRLAN_INT	Input
A9	WRLAN_nIORD	Output
B9	WRLAN_nIOWR	Output

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A5	uP_BUS_CLK	Input
K5	uP_CPLD_IRQ	Output
D10	uP_DACK0	Input
D9	uP_DREQ0	Input
G2	uP_A17	Input
H4	uP_A18	Input
C2	uP_A19	Input
D3	uP_A20	Input
D1	uP_A21	Input
D2	uP_A22	Input
E4	uP_A23	Input
K6	uP_MD0	Input/Output
J6	uP_MD1	Input/Output
H9	uP_MD10	Input/Output
J9	uP_MD11	Input/Output
G9	uP_MD12	Input/Output
G10	uP_MD13	Input/Output
G8	uP_MD14	Input/Output
F9	uP_MD15	Input/Output
H6	uP_MD2	Input/Output
K7	uP_MD3	Input/Output
J7	uP_MD4	Input/Output
H7	uP_MD5	Input/Output
J8	uP_MD6	Input/Output
K8	uP_MD7	Input/Output
J10	uP_MD8	Input/Output
H10	uP_MD9	Input/Output
H2	uP_MODE0	Input
H1	uP_MODE1	Input
J1	uP_MODE2	Input
K1	uP_MODE3	Input
A3	uP_nBLE1	Input
C1	uP_nCS0	Input
J5	uP_IRQC	Input
A6	uP_nMBLE0	Input
B6	uP_nRD	Input
C6	uP_nWAIT	Output
D8	uP_nWR	Input
A1	CPLD_TDI	JTAG
F3	CPLD_TMS	JTAG
F8	CPLD_TCK	JTAG
A10	CPLD_TDO	JTAG
D5, G6	VCCINT	POWER
C8, D4, E6, F5, G7, H3	VCCIO	POWER
C3, D7, E5, F6, G4, H8	GNDIO	GND
D6, G5	GNDINT	GND

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