LH75401-10/11
Card Engine

NOVO

LOGIC

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
1	Paul Mueller	First Draft Version	PGM	04/29/03
A	Paul Mueller	Production Release	KTL	05/02/03
B	Himanshu Khadilkar	Editing	HK	06/23/03
C	James Wicks	Added mode line description note	JW	09/19/03
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E	Erik Reynolds, Michael Anderson, James Wicks	Edit to coincide with the LH75401-11 Release	ECR	01/14/04

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC REV	APPROVAL	DATE
F	Jed Anderson	Corrected typo in Section 1.7.2 where the DC Core Supply Active Current was mistakenly listed as “T70”; Corrected Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes; Corrected Figure Numbers 2.4 and 3.2 to follow numbering scheme	LH75401-10 80000132 Rev A LH75401-11 80000227 Rev A01	JCA	11/15/06

Please check www.logicpd.com for the latest revision of this manual, erratas, and additional application notes.

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LH75401 CARD ENGINE

The LH75401 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

CARD ENGINE ADVANTAGE

- Reduce TIme to Market
  - ⟶ 6 to 9 month savings typical
- Product-Ready Hardware Platform
- Production Quality Software
  - Bootloader/Monitor
  - Board Support Packages
  - Supports other operating systems
- Engineering Support

ORDERING INFORMATION

- Zoom™ Starter Development Kit (Model # SDK-LH75401-11-0204)

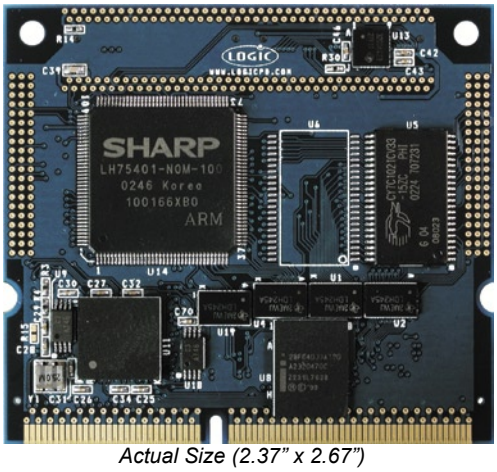
CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

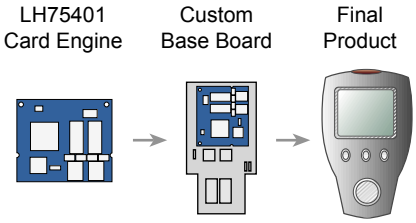
CONTACT

For more information on our EmbeddedProduct Solutions, please contact Logic Sales at www.logicpd.com or 612.672.9495.

The LH75401 Card Engine is a complete System on Module offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. The use of custom peripheral boards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation micro controller Card Engines when new funtionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Sharp LH75401 16/32 bit ARM7TDMI RISC micro processor running up to 70 MHz
- **SDRAM Memory** Up to 2 Mbytes
- **Flash Memory** Up to 8 Mbytes on board
- **Display** Programmable color LCD controller
  - Built in driver supports up to 320 x 240 (QVGA) x 12 bit color
  - Supports STN, Color STN, HR-TFT, AD-TFT, TFT
- **Touch Screen** Processor Integrated four or five wire resistive touch screen controller
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN 91C111 (MAC & PHY)
- **Audio** Audio Codec Stereo Output (TI TLV320DAC23)
- **PC Card Expansion** Compact Flash type 1 card (memory storage only)
- **Serial Ports** 3 X UARTS
  - 2 X 16C550 like, standard UARTS
  - 1 CAN Version 2.0b or 1 82510 UART
- **SSP** Supports either Motorola SPI™, National Semiconductor MICROWIRE™, TI SSI
- **GPIO** Programmable depending on peripheral requirements
- **Software**
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37"(60.2 mm) long x 2.67"(67.8 mm) wide x 0.17"(4.4 mm) high
  - 144 pin SODIMM connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit (Model # SDK-LH75401-11-0204)

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1.2 Acronyms

ADC	Analog to Digital Converter
AHB	Advanced Hardware Bus
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FET	Field Effect Transistor
FIFO	First In First Out
FIQ	Fast Interrupt Request
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
IO	Input Output
LCD	Liquid Crystal Display
LOLO	LogicLoader™
NC	No Connect
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
TTL	Transistor Transistor Logic
UART	Universal Asynchronous Receive Transmit
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

LH75401-10/11 IO Controller Specification
LogicLoader™ User's Manual
LH75401 Universal Microcontroller User's Guide
Altera MAX 7000A CPLD data sheet (EPM7128)
Altera Device Package Information data sheet
Altera Ordering Information
Texas Instruments TLV320DAC23 data manual

1.4 Card Engine Advantages

Logic's Card Engines accelerate your products time to market. In addition, the Card Engines provide the following advantages:

- Product Ready Hardware & Software solutions allow immediate application development which results in embedded product development cycle with less time, less cost, less risk, and with more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More Innovation – Allows you to focus on your IP
- Common Card Engine Footprint (See Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

1.5 Card Engine Interface

The Card Engine's common interface allows you to easily migrate to new processors and technology. Logic is in constant research and development of new technologies to improve performance, lower cost and increase feature capabilities. By using the common footprint, you can leverage Logic's work without having to re-spin your product. Contact Logic sales for more information.

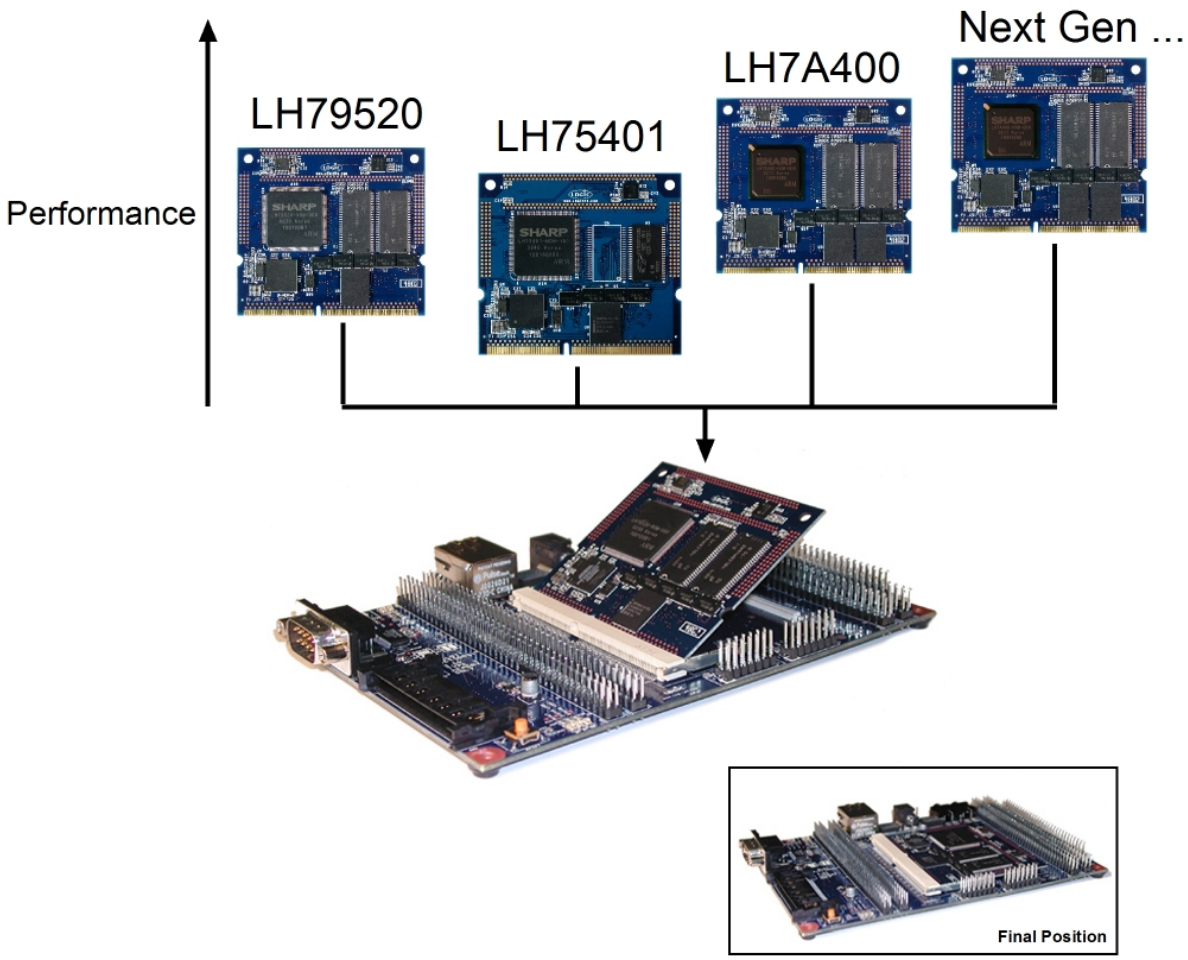


Figure 1.1: Card Engine Advantages

Encapsulating a significant amount of your design onto the Card Engine reduces risk of obsolescence issues. If a component on the Card Engine design becomes obsolete you don't have to re-spin your board, Logic will design for alternative part that is transparent to your product. Manufacturing also becomes much easier. Card Engines are delivered to you fully tested, making your manufacturing process simpler and less costly.

1.6 LH75401-10/11 Card Engine Block Diagram

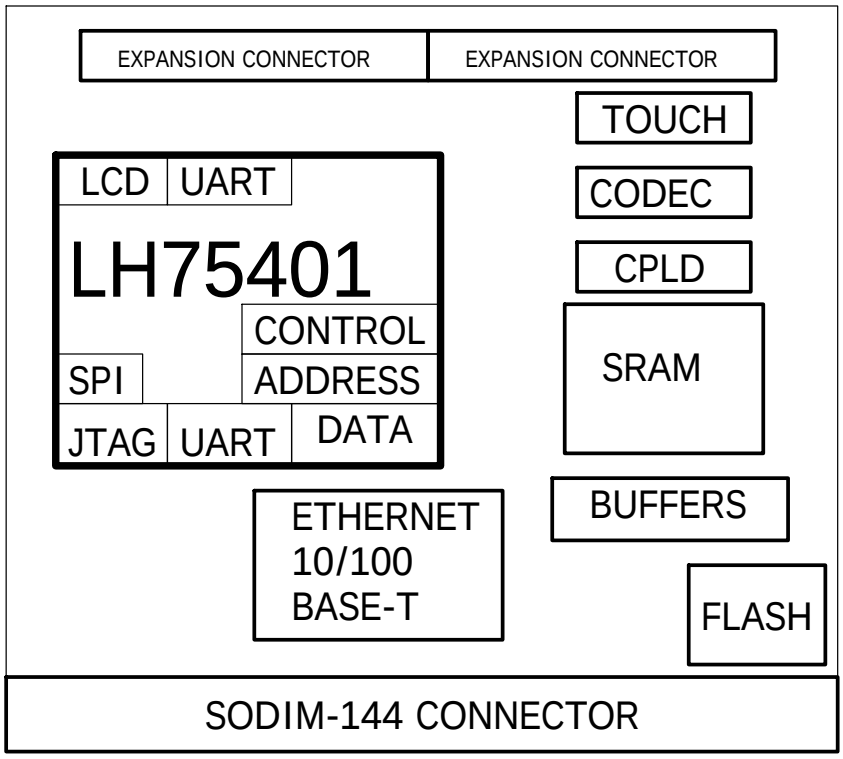


Figure 1.2: LH75401-10/11 Card Engine Block Diagram

1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	unit
DC IO and Peripheral Supply Voltage	3.3V	-0.3 to 4.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.4	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.7.2 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	TBD	320	TBD	mA	2
DC IO Supply Standby Current	TBD	300	TBD	mA	2
DC IO Supply Sleep Current	TBD	300	TBD	mA	2
DC Core Supply Voltage	1.62	1.8	1.98	V	1
DC Core Supply Active Current	TBD	40	70	mA	2
DC Core Supply Standby Current	TBD	30	40	mA	2
DC Core Supply Sleep Current	TBD	0	3	mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.37 x 2.67		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.6		VIO	V	
Output Signal Low Voltage	GND		0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. This test was performed with the 91C111 chip power disabled.
3. Contact Logic for more information on an industrial temperature LH75401-10/11 Card Engine
4. May vary depending on Card Engine configuration.

2 Electrical Specification

2.1 MicroController

2.1.1 LH75401 Microcontroller

The LH75401-10/11 Card Engine uses Sharp's highly integrated system on a chip LH75401 microcontroller. Sharp's LH75401 has a 32-bit ARM7TDMI-S RISC core. Sharp's LH75401 microcontroller is a system on a chip providing many integrated on-chip peripherals including:

- Integrated ARM7TDMI-S™ Core
  32 bit ARM7TDMI™ RISC Core❑
- 32 KB on-chip SRAM
  - ❑ 16 KB Tightly Coupled Memory(TCM) SRAM
  - ❑ 16 KB Internal SRAM
- Integrated Touchscreen Controller
- Clock and Power Management
- Eight Channel, 10-bit Analog-to-Digital Converter
- Serial Interfaces
  - ❑ Two 16C550-type UART
  - ❑ One 82510-type UART
- Synchronous Serial Port
- Real Time Clock (RTC)
- Three Counter/Timers
- Low Voltage Detector
- JTAG Debug interface and Boundary Scan
- Single 3.3 V Supply
- 5 V Tolerant Inputs
- 144-pin LQFP Package
- -40°C to +85°C Operating Temperature
- CAN Controller that supports CAN version 2.B

See Sharp's LH75401 Universal Microcontroller User's Guide for additional information.
http://www.sharpsma.com/

IMPORTANT NOTE: Please see http://www.sharpsma.com/ for any errata on the LH75401.

2.1.2 LH75401 Microcontroller Block Diagram

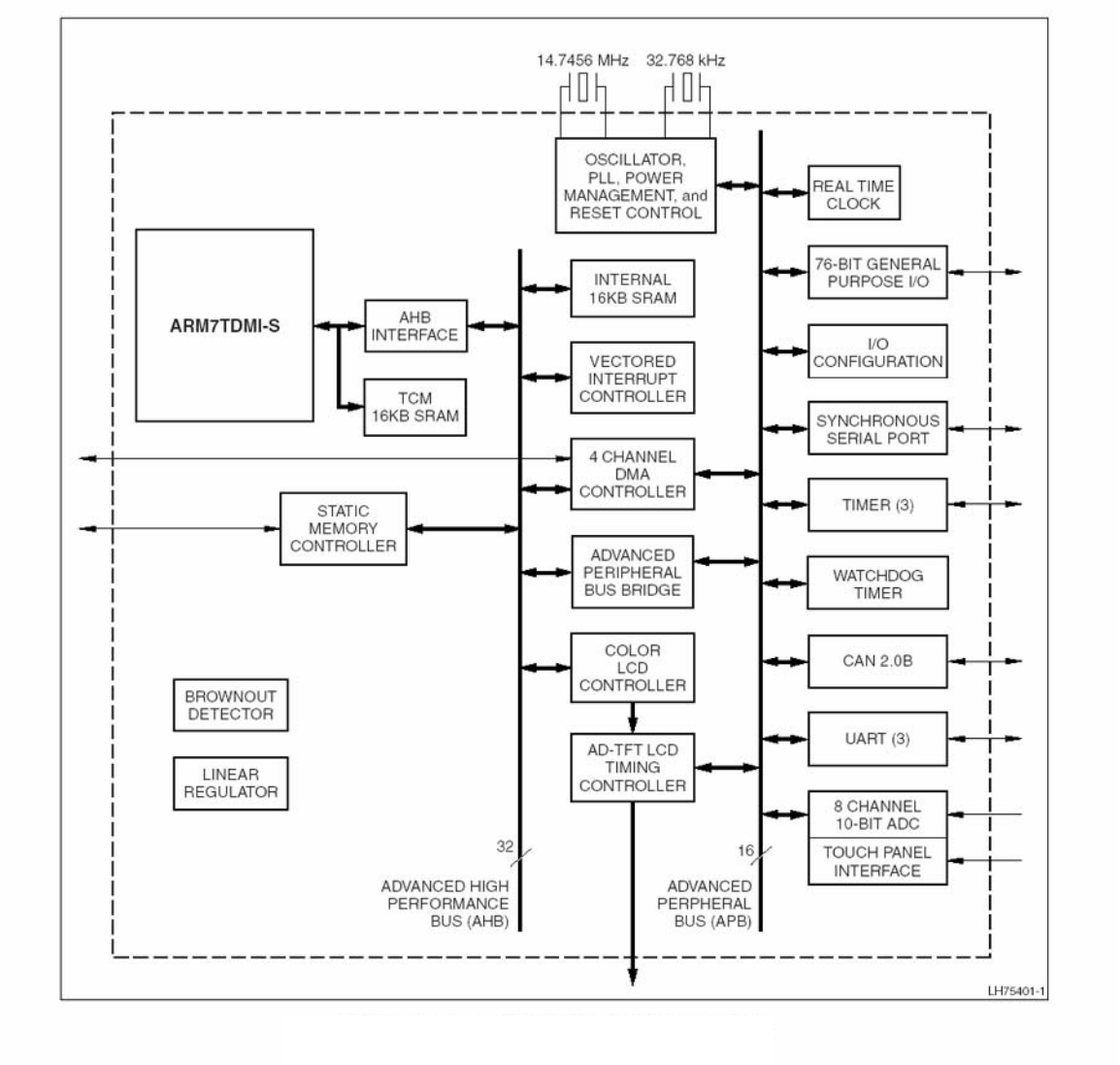


Figure 2.1: LH75401 Microcontroller Block Diagram

2.2 Clocks

The Sharp LH75401 processor requires a 14.7456 MHz (LH75401-10) or 20.0000 MHz (LH75401-11) crystal that is driven by the internal PLL.. This frequency is scaleable through software to generate a HCLK signal, which serves as the system clock. By using 14.7456 MHz or 20.0000 MHz crystal the exact frequencies required for proper UART operation are obtained. The 32.786 kHz crystal oscillator output is divided by 32768 to produce the 1 Hz RTC.

The LH75401 is software configurable to select between asynchronous, synchronous, and FastBus extension clocking mode. The microcontroller has a sophisticated clocking architecture and can be software programmable tailored to an application to vary the microcontroller performance, power consumption, and bus throughput. See the LH75401 Universal Microcontroller User's Guide for more details.

The LH75401-10's microcontroller core clock speed is initialized to 51.6096 MHz on the Card Engine and the Bus speed is 51.6096 MHz in the LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH75401-11's microcontroller core clock speed is initialized to 70.0000 MHz on the Card Engine and the Bus speed is 70.0000 MHz in the LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH75401-10 Card Engine provides an external Bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector at a frequency of 25 MHz. The uP_BUS_CLK is required for the wired LAN and the CPLD and may be used for other peripheral devices via the expansion connectors.

LH75401 Microcontroller Signal Name	LH75401-10/11 Card Engine Net Name	Default Software Value in LogicLoader™
HCLK	N/A	51.6096 MHz/70.0000 MHz
N/A	uP_BUS_CLK	25.000 MHz

IMPORTANT NOTE: The uP_BUS_CLK is not an output from the processor. The uP_BUS_CLK signal is created from a 25 MHz oscillator which drives the Wired LAN and CPLD timings.

2.3 Memory

2.3.1 SRAM

The LH75401-10/11 Card Engine uses a 16-bit memory bus to interface to SRAM. The memory can be configured as 256 KB, 512 KB, 1 MB, or 2 MB to meet the user's memory requirements and cost constraints. The default memory configuration is a 512 KB configuration.

2.3.2 Direct Memory Access (DMA)

The Sharp LH75401 microcontroller has an internal DMA controller with 4 DMA data streams; only one external DMA channel is available to the user. The standard LH75401-10 Card Engine uses external DMA Channel 0 to interface with the onboard audio CODEC - Texas Instruments TLV320DAC23. If an external DMA channel is required, please contact Logic Product Development.

2.3.3 NOR Flash

The LH75401-10/11 Card Engine uses a 16-bit memory bus to interface to StrataFlash. The on board Card Engine memory is typically configured as 4 MBytes but can be configured as 4 or 8 MBytes to meet the user's flash requirements and cost constraints. A user should consult Logic when specifying flash size because it is one of the most expensive components in the LH75401-10/11 Card Engine.

A user can expand their non-volatile storage capability using the LH75401-10/11 Card Engine Application Kit as a design reference. Users can expand their non-volatile storage capability by external flash IC's, CompactFlash, or NAND Flash. See the LH75401-10 Application Kit for reference designs or contact Logic for other reference designs of peripheral interfaces.

2.3.4 CompactFlash (memory-mapped mode only)

The LH75401 microcontroller does not have an on chip integrated CompactFlash controller. However, for applications requiring larger non-volatile storage, the LH75401-10/11 Card Engine provides the necessary signals using the CPLD for a CompactFlash card interface in memory-

mapped mode only. The Zoom™ Starter Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support the hot-swappable capability. See the LH75401-10/11 IO Controller Specification for further details.

IMPORTANT NOTE: Additional hardware is required on the user's daughter board to provide hot-swapping capability.

IMPORTANT NOTE: The CPLD CompactFlash interface supports memory-mapped mode only. Designs requiring other CompactFlash modes should use an external controller or select a Card Engine with an integrated CompactFlash interface.

2.4 10/100 Ethernet Controller

The LH75401-10/11 Card Engine uses the SMSC 91C111 10/100 Ethernet single chip solution. The Card Engine Ethernet interface provides an easy to use interface. The Card Engine provides six signals from the 91C111: ETHER_TX(+), ETHER_TX(-), ETHER_RX(+), ETHER_RX(-), ETHER_nACT_LED, and ETHER_nLNK_LED. The four analog PHY interface signals (ETHER_TX(+), ETHER_TX(-), ETHER_RX(+), and ETHER_RX(-)) require an external impedance matching circuit. Logic provides an example circuit schematics in the LH75401-10/11 Application Kit for reference.

IMPORTANT NOTE: Eneep signal on the SMSC 91C111 is connected to R15(np) (zero ohm resistor) that is not populated. Eneep signal has an internal weak pull up in the SMSC 91C111. If Eneep signal is tied low it will disable the serial EEPROM interface.

2.5 Audio Codec

The LH75401-10/11 Card Engine uses the TI TLV320DAC23GQE high performance low cost stereo audio codec. Low power consumption and flexible power management allow selective control of the DAC functions on this component to optimize low power designs. The TLV320DAC23GQE audio codec has a single channel stereo input and single channel stereo output, but the LH75401-10/11 Card Engine does not support stereo input on its standard card engine.

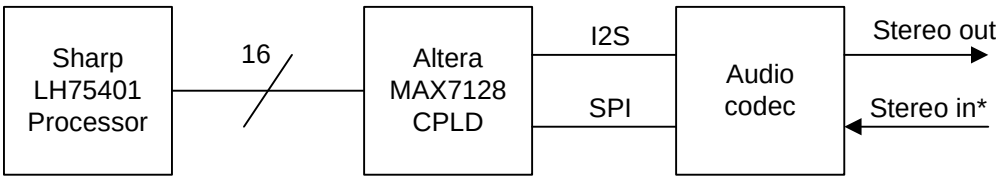


Figure 2.2: Audio CODEC Block Diagram

IMPORTANT NOTE: Stereo In not supported in default LH75401-10/11 Card Engine

The LH75401-10/11 Card Engine supports a 10-bit stereo out. The audio codec uses a 5.6448 MHz crystal. The audio codec is software programmable via the SPI interface in the CPLD. See the CPLD Interface Specification for programming information. The audio codec provides software programmable sample rates, volume control, mute, and power management. See the TI Audio Codec TLV320DAC23 specification for programmable register settings and additional features and functionality.

Logic has interfaced other high performance audio codecs to the Card Engines. Contact Logic for assistance in selecting an appropriate audio codec for your application.

2.6 Video Interface

Sharp's LH75401 microcontroller has a built in LCD controller supporting STN, TFT, HR-TFT and AD-TFT panels at VGA (640 x 480) Black and White, Grayscale, or 4 bpp VGA color or up to QVGA (320 x 240) Color. See the LH75401 Universal Microcontroller User's Guide for further information on the integrated LCD controller. The LCD controller signals from the LH75401-10/11 are located on one of the Card Engine's 80-pin expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic Product Development before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor bus load.

2.7 Serial Interface

The LH75401-10/11 Card Engine comes with the following serial channels: UARTA, UARTB, UARTC, and SPI. If additional serial channels are required, please contact Logic for reference designs.

2.7.1 UARTA

UARTA has been configured to be the LH75401 main serial port. It has similar functionality to the industry standard 82510. This SCIF interface is a high-speed serial interface with a FIFO (asynchronous or synchronous) and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Zoom™ Starter Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA is available off the 144-pin SO-DIMM connector and is capable of supporting baud rates up to 3.225M bits/sec (given system clock as 51.6096MHz or 70.0000MHz). Please see the LH75401 Universal Microcontroller User's Guide for further information.

2.7.2 UARTB

Serial Port UARTB has dual functionality, its primary function is as an asynchronous 16C550 compatible UART. This SCIF interface is also a high-speed serial interface with a 1-16 byte programmable FIFO (asynchronous or synchronous) and is capable of sending and receiving serial data simultaneously. This port can also be programmed to utilize the on-chip DMA to reduce processor bandwidth required to service UART activities. The signals from the Card Engine are TTL level signals not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTB's baud rate can also be set to all common serial baud rates from 110bps to 921.6K bits/sec.

Serial Port UARTB is multiplexed with IRQ lines D and E. If you use UARTB, you can not use IRQ lines D and E; conversely, if you use IRQ lines D and/or E, you can not use UARTB.

2.7.3 UARTC

Serial Port UARTC also has dual functionality, its primary function is as an asynchronous 16C550 compatible UART. This SCIF interface is also a high-speed serial interface with a 1-16 byte programmable FIFO (asynchronous or synchronous) and is capable of sending and receiving serial data simultaneously. This port can also be programmed to utilize the on-chip DMA to reduce processor bandwidth required to service UART activities. The signals from the Card Engine are TTL level signals not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTC's baud rate can also be set to all common serial baud rates from 110bps to 921.6K bits/sec.

Serial Port UARTC is multiplexed to allow CAN 2.0b functionality. The CAN 2.0B controller is an AMBA-compliant peripheral that connects as a slave to the APB.

2.7.4 SPI

The SPI interface on the LH75401 is a SSP (synchronous serial port) used to facilitate synchronous serial communications with slave peripheral devices. This serial port is a Master-only device, with programmable clock bit-rate and prescale factors. It supports three data frame formats:

- Texas Instruments' SSI
- Motorola SPI™
- National Semiconductor Microwire™

The SPI interface signals are available off the 144-pin SO-DIMM connector. Please see the LH75401 Universal Microcontroller User's Guide for further information.

2.8 CAN

The LH75401 processor has an integrated CAN controller. The CAN communications are performed serially at a maximum frequency of 1Mbit/s with a 64byte receive FIFO. The controller has full compliance with the 2.0A and 2.0B Bosch specifications. The CAN pins are multiplexed with the UARTC on the LH75401-10/11 Card Engine. An external CAN transceiver is required for interfacing with the CAN controller on the LH75401-10/11 Card Engine, please contact Logic Product Development for recommendations concerning interfacing.

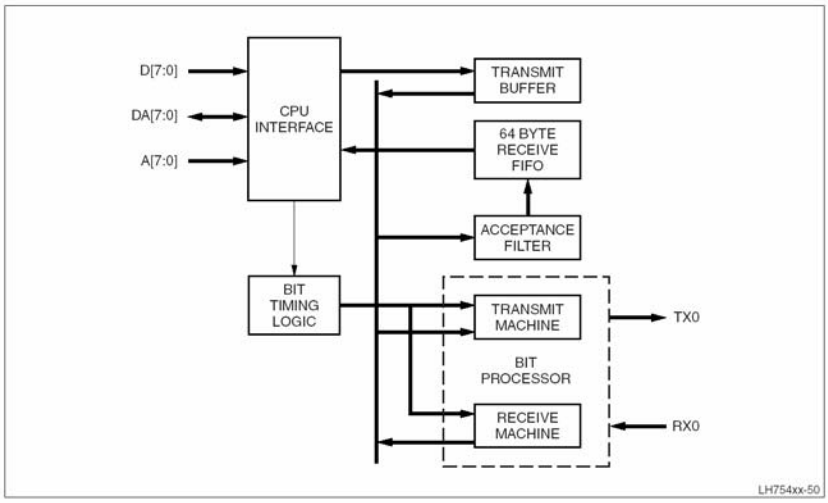


Figure 2.3 CAN Controller Block Diagram

2.9 Touch Interface

Touch interface is supported on the LH75401-10/11 Card Engine for standard 4-wire resistive touch panels. The LH75401 processor has 8 Analog-to-Digital Converter (ADC) channels, of which 4 are used for the analog touch interface (AN0-AN3).

The analog touch interface signals on the external connectors are: TOUCH_TOP, TOUCH_BOTTOM, TOUCH_RIGHT and TOUCH_LEFT.

IMPORTANT NOTE: The net names reflect the side of the touch screen that they should be attached to and do not necessarily mean X or Y axis, as the terms "X" and "Y" can be interpreted in different ways.

2.10 General Purpose Analog & Digital I/O

Logic designed the LH75401-10/11 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO on the Card Engine that interface to the LH75401, and the Altera CPLD. Some of these GPIO are interrupt capable while other signals are input or output only. Please see the Pin Descriptions section of this data sheet.

The LH75401 microcontroller has 4 Analog-to-Digital conversion channels that are available to the user through the expansion bus connectors (the remaining 4 channels are used for the touch screen interface as previously mentioned). If certain peripherals are not used, such as the LCD Controller, Chip Selects, IRQs, UARTs, or SPI port multiple GPIO pins become available. Please see the table in section 5 entitled “Multiplexed Signal Trade-Offs.” This table lists the available GPIO trade-offs that are available when certain peripheral functions are not used.

2.11 CPLD

Please see the LH75401-10/11 IO Controller Specification for CPLD information.

2.12 Serial EEPROM Interface

Logic designed the LH75401-10/11 Card Engine to have a low cost 1 kbit serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the LH75401 microcontroller via the CPLD through a SPI interface. See Figure 5 below. Please see the LH75401-10/11 IO Controller Specification for CPLD information.

Figure 2.4: Serial EEPROM Block Diagram

2.13 Expansion Options

The LH75401-10/11 Card Engine was designed for expansion and provides all the necessary control signals and bus signals to expand the user’s design. Many of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. See the LH75401-10/11 Card Engine schematics for more detail. A user can expand the Card Engine’s functionality such as PCI, Compact Flash, PCMCIA, ISA devices, PCI devices, etc.. Logic has expanded the Card Engine to other audio codecs, Ethernet IC’s, UARTs, Co-processors, etc.. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The LH75401-10/11 Card Engine was designed to be configurable to meet user's applications and budget needs. The Card Engine supports a variety of embedded operating systems and comes in the following hardware configurations:

- Flexible memory footprint: 256k bytes, 512k bytes, 1 MByte, 2MByte SRAM
- Flexible FLASH footprint: 4 or 8 MBytes StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional TI TLV320DAC23GQE Audio Codec

Please contact Logic Product Development for additional hardware configurations to meet your application.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. All internal card engine peripheral hardware reset pins are connected to either the MSTR_nRST net or to the RESET_HIGH net as shown in the figure below. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally to the card engine. Logic suggests that custom designs implemented with the LH75401-10/11 Card Engine use the MSTR_nRST signal as the "pin hole" reset used in commercial embedded systems.

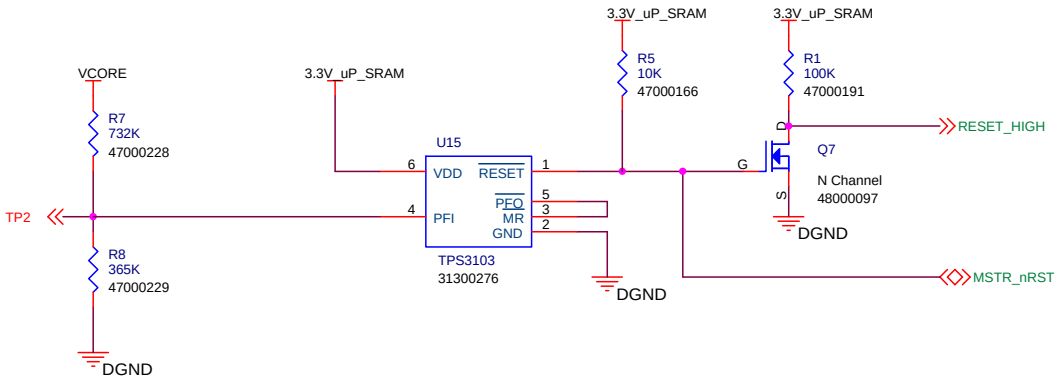


Figure 3.1: Reset Circuit

The MSTR_nRST signal is an active low output of the reset chip, located on the card engine. The RESET_HIGH signal is an active high output of the reset circuit and is not provided as part of the card engine connector interface.

IMPORTANT NOTE: The custom design should guard the assertion of the reset lines during a low power state so the microprocessor cannot be reset and powered on in a low or bad power condition (will cause data corruption and possible temporary system lockup). See section entitled "Power Management" for further details.

There are three conditions that will generate a low on the output reset pin of the reset chip (the MSTR_nRST signal): power-on condition, a low pulse on the MSTR_nRST signal, and the power fail comparator input (PFI pin) falling below the internal comparator threshold.

Power On:
At power on, MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 2.941V. Once the 3.3V_uP_SRAM supply becomes higher than 2.941V, an internal timer will delay the rising edge of MSTR_nRST from 65 to 195 mS (130 mS typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (custom design or application board) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic also suggests analog or digital de-bouncing of an external assertion source of the MSTR_nRST signal.

Power Fail:
If the power fail comparator input pin (PFI pin) falls below the internal comparator threshold of 0.551V, it will create a low pulse on the MR input pin of the reset chip. The low assertion of the MR pin will assert the MSTR_nRST signal and will hold it low after the MR pin is deasserted (PFI is above the comparator level – power is restored) for 65 to 195 mS (130 mS typical).

Please see the TI TPS3103 data sheet at http://www.ti.com for additional details on reset timing and thresholds.

3.2.2 Soft Reset

Logic has created a soft reset signal named uP_SW_nRESET that can be used to reset the LH75401 microprocessor's internal registers without affecting the peripherals on the rest of the board and without losing data stored in SRAM or other volatile storage. The uP_SW_nRESET signal is an input to LH75401-10/11 Card Engine's CPLD.

3.3 Interrupts

The LH75401 responds to ARM exceptions and vectored interrupts generated by the onboard-vectored interrupt controller (VIC). The LH75401 accepts inputs from 32 interrupt sources--23 are from internal sources, and 7 are from external sources and 2 can be controlled by software. All interrupts are routed to the VIC where priorities are determined by hardware and the appropriate interrupt signal is dispatched to the ARM7 exception-handling hardware. Lower numbered interrupts have higher priority than higher-numbered interrupts. Each external interrupt has rising edge, falling edge, HIGH level, or LOW-level trigger options. The LH75401-10/11 Card Engine interrupts are set to trigger on a LOW level by default. The LH75401-10/11 Card Engine provides 5 available interrupt sources. Each of the interrupts can be separately setup as FIQs via software. Refer to Sharp's LH75401 Universal Microcontroller User's Guide for further information.

IMPORTANT NOTE: See LH75401-10/11 IO Controller Specification for detailed information on the use of the CPLD interrupt (signal uP_CPLD_IRQ).

3.4 JTAG Debugger Interface

There are many different third party JTAG debuggers available for Sharp ARM microcontrollers. The JTAG connection enables a user to recover a board that has corrupted flash memory and to debug real time applications. The following signals make up the JTAG interface to the LH75401, for connection to a JTAG emulator: uP_TRST, uP_TDI, uP_TMS, uP_TCK, uP_TDO, and uP_RTCK. These signals should interface directly to a 20-pin 0.1" through-hole connector as demonstrated in the Sharp LH75401 Universal Microcontroller User's Guide, or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20 pin connector out, realize it may not be numbered as a standard 20 pin 0.1" IDC through-hole connector. See LH75401-10/11 Card Engine Application Kit reference design for further details. Different IC manufacturers define the 14 pin IDC connector pin-out differently.

3.5 Power Management

3.5.1 System Power Supplies

The LH75401-10/11 Card Engine was designed to have the following five power areas, 3.3V_uP_SRAM, 3.3V, 3.3VA, 3.3V_WRLAN and VCORE for a flexible hardware design. All power areas are inputs to the card engine with the exception of 3.3V_WRLAN, which is an output from the card engine.

3.5.1.1 3.3V_uP_SRAM

The 3.3V_uP_SRAM input pins are designed to be connected to a 3.3V power supply with optional backup battery. If the design is required to maintain SRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using STANDBY mode with its software BSPs to prepare the system for the critical power condition. In order to do this, STANDBY mode puts the processor into the standby state. Please see the description of STANDBY mode later in this section.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane power the majority of the peripheral's digital supply pins on the LH75401-10/11 Card Engine. This supply must stay within the acceptable levels as specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a STANDBY sequence and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane power all analog power supply pins of both the LH75401 microprocessor and applicable peripherals on the LH75401-10/11 Card Engine. This supply must stay within the acceptable levels as specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a STANDBY sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This "power" supply net is an output from the card engine. It is controlled through a registered bit in the on-board CPLD. See the "LH75401-10/11 IO Controller Specification" for specific details on this control bit. Logic's software BSPs assert this signal as appropriate. This is done because the software power management in the 91C111 does not put the part in a low enough power state for many applications.

The custom application board should use this power supply output pin to supply the Ethernet impedance matching resistors with power. They should not be connected to 3.3V directly or the entire Ethernet controller circuit on the card engine will try to power itself through the impedance matching resistors. Please see Logic's schematics for the Zoom™ Starter Kit or other reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the card engine is to power the 91c111 separately and give the ability to shut it off completely but independently. The 3.3V_WRLAN output from the card engine is required to completely isolate the LAN circuit such that it is not back powered through the impedance matching resistors.

3.5.1.5 VCORE

The VCORE input pins are designed to be connected to a 1.8V power supply with optional backup battery. If the design is required to maintain SRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using STANDBY mode with its software BSPs to prepare the system for the critical power condition. In order to do this, STANDBY mode puts the processor into the standby state. Please see the description of STANDBY mode later in this section.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_ SDRAM	3.3 VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to refresh.
3.3V	3.3 VDC	Connects to the digital peripherals on the Card Engine.
3.3VA	3.3 VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
3.3V_WRLAN	NA	The 3.3V_WRLAN is located on the Card Engine only and provides power to the SMSC 911C111 processor. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the CPLD IO Controller Spec. for information on controlling the WRLAN_E.
VCORE	See note	Connects to the processor core voltage. See specific processor for VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperature, etc.

Figure 3.2: Power Plane Diagram

IMPORTANT NOTE: The purpose of the PMOS FET to control the power to the SMSC 91C111 is because the software power management in the 91C111 is not suitable for many applications.

IMPORTANT NOTE: The LH75401-10/11 Card Engine hardware architecture was designed for low power battery operated applications. However, the Altera CPLD on the LH75401-10/11 Card Engine is not an ideal part for low power battery operated designs. This specific component was chosen for cost. If one is using the LH75401-10/11 Card Engine as a reference design, one can consider other programmable logic devices that are optimized for power, not cost.

3.5.2 Peripherals

Most peripherals provide software programmable power states. The audio codec and touch controller have programmable power states. Please see the appropriate data sheet for more information and the CPLD Interface Specification for details. The SMSC 91C111 controller has

software programmable power states but may not be sufficient for some applications. Logic has provided hardware to cut power to the 91C111 IC.

3.5.3 System Power Management

Good power management design happens in the hardware and software of any system. Typically, the power management design of any embedded system can be one of the most complicated parts and has a dramatic effect on the overall product cost, performance, usability, and customer satisfaction. Many factors effect good power management design in the hardware including: power supply selection (efficiency), clocking design, IC and component selection, etc. The LH75401-10/11 Card Engine electronics were designed to provide maximum flexibility to the software and system integrator.

There are many different software configurations which drastically effect the power consumption of the LH75401-10/11 Card Engine including: microprocessor core clock frequency, microprocessor bus clock frequency, microprocessor peripheral clocks, microprocessor bus utilization, microprocessor power management states (normal, sleep, standby, module-standby), peripheral power states and modes, product user scenarios, interrupt handling, display settings (resolution, backlight, refresh, bits per pixel, etc..) These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. These items are covered in the appropriate documents such as the Bootloader User's Manual or appropriate BSP manual.

3.5.4 Microcontroller

The LH75401-10/11 Card Engine power management's scheme was designed to be easy to use. There are five power management states provided in the LH75401 microcontroller: ACTIVE, STANDBY, SLEEP, STOP1, and STOP2. Sharp's LH75401 provides complex power management features. Please see the LH75401 Universal Microcontroller User's Guide for more details.

IMPORTANT NOTE: The BSP's available from Logic for the different operating systems supported on the LH75401 may not support all five of the power management states. Please see the appropriate BSP documentation for power management modes for more detail.

3.5.4.1 Active Mode

The LH75401-10/11 Card Engine normal operating state is ACTIVE. The LH75401 system on a chip enters this mode on reset and returns to this mode when any interrupt is received, if operating in any other power mode. The LH75401 cannot transition directly between the other power modes; it will always return to active mode before entering any other power mode.

3.5.4.2 Standby Mode

The Standby mode halts the clocks to the CPU while leaving the remainder of the chip active. The LH75401 transitions from the Standby mode to the Active mode when an interrupt is received.

3.5.4.3 Sleep Mode

The Sleep mode halts all system clocks. Only the PLL and the internal oscillators remain active. If the 32.768 kHz internal oscillator is in use, it will also remain active. The LH75401 transitions from the Sleep mode to the Active mode when an interrupt is received.

When transitioning from the Active mode to the Sleep mode, the LH75401 Power Management system automatically performs the following sequence:

- Acquires control of the AHB, to ensure that all transactions are completed.
- Ensures that all SRAM devices are placed in the self-refresh mode of operation.

- Halts all output clocks that are driven by HCLK, HCLK_CPU, and PCLK
- Waits for IRQ or FIQ to be asserted (which will return the LH75401 to the Active mode).

When an IRQ or FIQ occurs, the LH75401 returns to the Active mode, restarts the output clocks, resumes SDRAM refresh and then cedes control of the AHB.

3.5.4.4 Stop1 Mode

The Stop1 mode halts all system clocks and disables the PLL but keeps the internal oscillators active. If the 32.768 kHz internal oscillator is in use, it will remain active. The LH75401 transitions from the Stop1 mode to the Active mode when an interrupt is received.
When transitioning from the Active mode to the Stop1 mode, the LH75401 Power Management system automatically performs the following sequence:

- Acquire control of the AHB, to ensure that all transactions are completed.
- Ensure that all SRAM devices are placed in the self-refresh mode of operation.
- Wait for IRQ or FIQ to be asserted (which will return the LH75401 to the Active mode).

When an IRQ or FIQ occurs, the LH75401 returns to the Active mode, restarts the output clocks (which may require a delay for the PLL to reacquire lock, if the PLL is in use), then returns control of the AHB.

3.5.4.5 Stop2 Mode

The Stop2 mode halts all system clocks and disables both the PLL and the internal oscillators that feed it. If the 32.768 kHz internal oscillator is in use, it will remain active. The LH75401 transitions from the Stop2 mode to the Active mode when an interrupt is received.

When transitioning from the Active mode to the Stop2 mode, the LH75401 Power Management system automatically performs the following sequence:

- Acquire control of the AHB, to ensure that all transactions are completed.
- Ensure that all SRAM devices are placed in the self-refresh mode of operation.
- Halts all clocks, disable the PLL, disable the 14.7456 MHz/20.0000 MHz oscillator.
- Wait for IRQ or FIQ to be asserted (which will return the LH75401 to the Active mode).

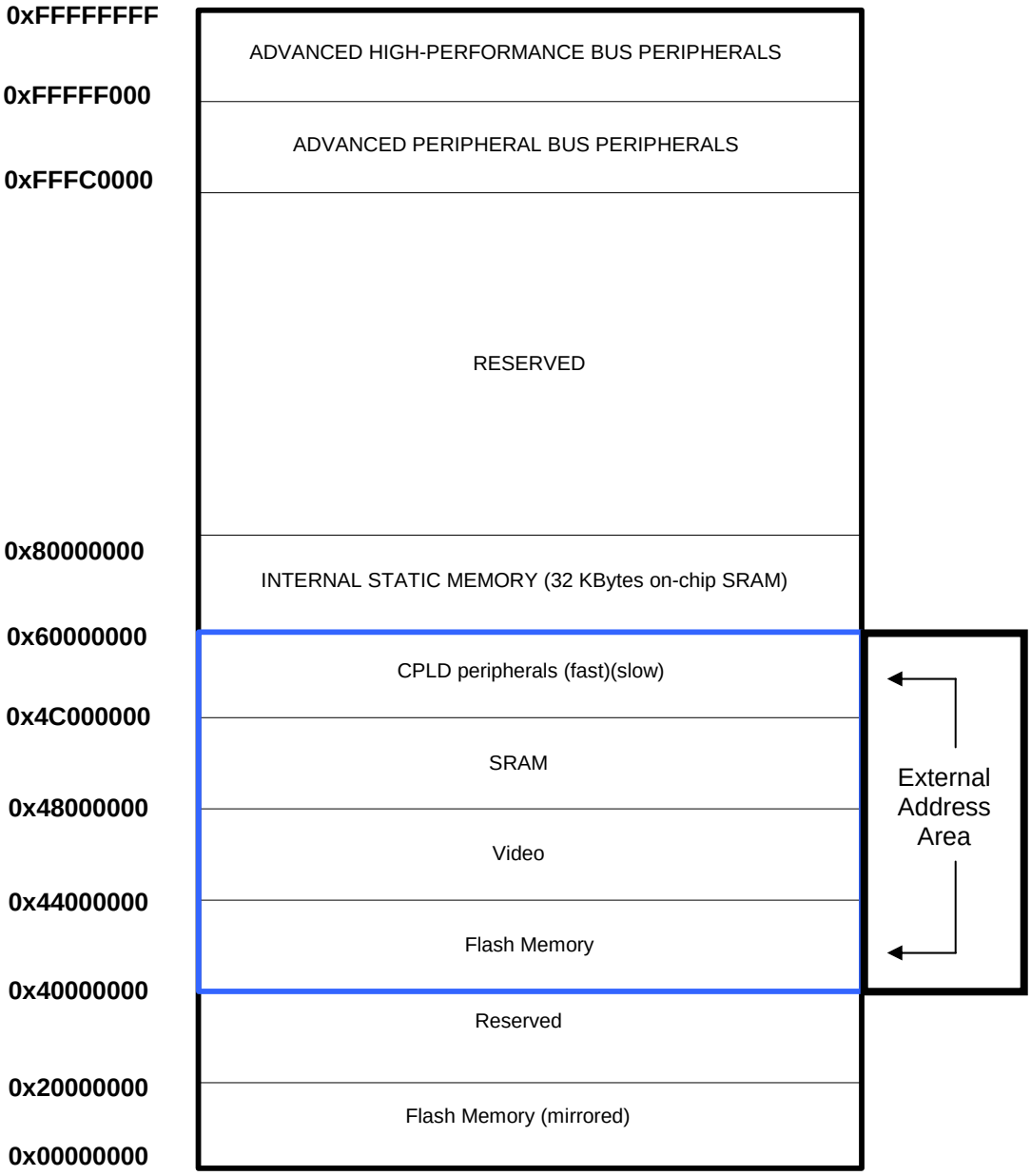
When an IRQ or FIQ occurs, the LH75401 returns to the Active mode, restarts the output clocks (which may require a delay for the PLL to reacquire lock, if the PLL is in use), then returns control of the AHB.

3.6 ESD Considerations

The LH75401-10 Card Engine was designed to interface to a customer's peripheral board. The Card Engine was designed to be low cost and adaptable to many different applications. The LH75401-10/11 Card Engine does not provide any ESD protection circuitry on the card and must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SRAM Memory Map



Note, this is the standard boot memory map for the LH75401 processor. No re-mapping has been performed.

Figure 4.1: LH75401 Card Engine General Memory Map

4.2 External Static Memory Map

4.2.1 Card Engine Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the card engine.

Chip Select	Bank	Start Address	Memory Description
nCS3	3	0x4C00 0000	CPLD peripherals (fast)/(slow)[2]
nCS2	2	0x4800 0000	SRAM
nCS1	1	0x4400 0000	Video[3]
nCS0	0	0x4000 0000	Boot Device (FLASH or EEPROM[3])

Notes:

2. CPLD peripherals are those components that get a decoded chip select from the CPLD. (i.e. CPLD memory mapped registers, onboard SMSC 91C111 Ethernet controller, etc... Please see the LH75401-10/11 IO Controller Specification document for details.)

3. Components planned for future applications.

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the card engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SO-DIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O[1]	Active Low. This signal initiates a hard reset (power on) – external memory contents are lost during reset. Every peripheral on the card engine with a reset line is reset with the assertion of this signal. Refer to LH75401 processor datasheet for register states during or after power on reset. This signal has a 10k pull up on the card engine.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	uP_SW_nRESET	I[1]	Active Low. This signal initiates a soft reset (manual reset) – external memory contents are retained during reset. This pin is connected to the CPLD, please see LH75401-10/11 IO Controller Specification for detailed information on the use of the CPLD based reset. This signal has a 10k pull up on the card engine.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nMCS	O	Active Low. Buffered chip select for area 4 of LH75401-10/11 memory. This is the "fast" peripheral chip select area. This is set to a 16 bit wide area and should not be changed. See memory map for details.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8		NC	No internal connection (not implemented on the LH75401-10/11)
9	DGND	I	Digital Ground (0V)
10	VIDEO_nMCS	O	Active Low. Buffered chip select for area 2 of LH75401-10/11 memory. This is the "video" chip select area. This chip select is also capable of controlling additional external SRAM. This is set to a 16 bit wide area and can be changed based on the user's needs. See memory map for details.
11	ETHER_nACT_LED	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nMCS	O	Active Low. This signal is the buffered chip select for boot ROM and is connected to area 0 of LH75401-10/11 memory when uP_MODE3 is low. When uP_MODE3 is high, this signal is activated at a specific memory mapped address in the slow chip select area (16 bit wide area 2). The memory width for area 0 is selectable with uP_MODE0 and uP_MODE1. See memory map for details.
13	ETHER_nLNK_LED	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. This signal is driven by the ISA bus master or DMA controller to signal valid write data on the data bus. A peripheral may use this signal to latch the data in. See the LH75401-10/11 IO Controller Specification for further details.

Pin #	Signal Name	I/O	Description
15	nSTANDBY	I[1]	Active Low. CPU power mode signal. This signal is registered in the CPLD. Please reference the LH75401-10/11 IO Controler Specification for implementation. This signal has a 10k pull up on the card engine.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the LH75401-10/11 IO Controller Specification for further details.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid. See the LH75401-10/11 IO Controller Specification for further details.
21		NC	No internal connection (not implemented on the LH75401-10/11)
22	nCHRDY	I[1]	Active Low. The I/O channel ready signal line allows the resources to indicate to the ISA bus master that additional cycle time is required. Peripherals using this signal must make their outputs open drain, as it is a shared bus. See the LH75401-10/11 IO Controller Specification for further details. This signal has a 10k pull up on the card engine.
23		NC	No internal connection (not implemented on the LH75401-10/11)
24	uP_TEST1	I[1]	This is connected to Test Mode Pin 1 on the LH75401 processor. Please see the section on Operating Modes in the LH75401 technical datasheet for detailed operation. This signal has a 10k pull up on the card engine.
25	uP_IRQC	I[1]	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a general-purpose input only pin. This signal is pulled up to 3.3V_uP_SRAM through a 10K resistor.
26	uP_TEST2	I	This is connected to Test Mode Pin 2 on the LH75401 processor. Please see the section on Operating Modes in the LH75401 technical datasheet for detailed operation. This signal has a 10k pull up on the card engine.
27	uP_IRQB	I[1]	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a general-purpose input only pin. This signal is pulled up to 3.3V_uP_SRAM through a 10K resistor.
28	uP_TRST	I[1]	This signal is pulled up to 3.3V_uP_SRAM through a 10K resistor.
29	uP_IRQA	I[1]	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a general-purpose input only pin. This signal is pulled up to 3.3V_uP_SRAM through a 10K resistor.
30	uP_TMS	I[1]	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal has a 10k pull up on the card engine.
31		NC	No internal connection (not implemented on the LH75401-10/11)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use. This signal has a 10k pull up on the card engine.
33		NC	No internal connection (not implemented on the LH75401-10/11)
34	uP_TDI	I[1]	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal has a 10k pull up on the card engine.
35		NC	No internal connection (not implemented on the LH75401-10/11)
36	uP_TCK	I[1]	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal has a 10k pull up on the card engine.
37	uP_nWAIT	I	Active low. The WAIT signal requests the current bus cycle be extended until this signal is de-asserted. This signal will completely halt processor operations until it is de-asserted and the bus cycle is ended. Peripherals using this signal must make their outputs open drain, as it is a shared bus. This signal has a 10K pull up resistor to 3.3V_uP_SRAM on the card engine.

Pin #	Signal Name	I/O	Description
38	uP_MODE3	I[1]	Boot select signal (0 = external boot device, 1 = onboard flash). This defaults to high (onboard flash) if left unconnected (pulled to 3.3V_uP_SRAM through a 10K pullup resistor).
39		NC	No internal connection (not implemented on the LH75401-10/11)
40	uP_MODE2	I[1]	The LH75401 processor only supports Little Endian memory operations. On development kits by Logic Product Development, the generic use of this pin is an Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left unconnected (pulled to 3.3V_uP_SRAM through a 10K pullup resistor).
41		NC	No internal connection (not implemented on the LH75401-10/11
42	uP_MODE1	I[1]	This signal is registered in the CPLD. The LH75401 can only boot from 8 bit and 16 bit sources so uP_MODE1 is not required for determining external boot widths. This signal has a 10k pull up on the card engine.
43	uP_UARTA_TX – PE1	O	SCIF port (UARTA) transmit data output. Internally pulled up on the LH75401 processor.
44	uP_MODE0	I[1]	Bus width setting. uP_MODE0 – 0 = 8 bit, 1 = 16 bit. This signal is read immediately after power on reset and determines the boot width of area 0. This changes BOOT_nCS bus size between 8 and 16 bits. This defaults to high if left unconnected (pulled to 3.3V_uP_SRAM through a 10K pullup resistor). The default state boots from the 16 bit flash chip on the card engine.
45	uP_UARTA_RX – PE2	I	SCIF port (UARTA) receive data input. Internally pulled up on the LH75401 processor.
46		NC	No internal connection (not implemented on the LH75401-10/11)
47		NC	No internal connection (not implemented on the LH75401-10/11)
48	uP_DREQ0	I[1]	Active low. DMA channel 0 external request (low level or falling edge selectable). This may also be configured as a general purpose input only pin PTD4. This is pulled down to DGND through a 10K resistor. This signal is also pulled down internally on the LH75401 processor.
49		NC	No internal connection (not implemented on the LH75401-10/11)
50		NC	No internal connection (not implemented on the LH75401-10/11)
51	nSUSPEND	I[1]	Active low. CPU power mode signal. This signal can be read from the CPLD for power management schemes. This pin is connected directly to the CPLD and it is pulled up to 3.3V_uP_SRAM by a 10k resistor.
52		NC	No internal connection (not implemented on the LH75401-10/11)
53		NC	No internal connection (not implemented on the LH75401-10/11)
54		NC	No internal connection (not implemented on the LH75401-10/11)
55	DGND	I	Digital Ground (0V)
56	uP_DACK0	O || O[1]	DMA channel 0 acknowledge (active state selectable) || Active low. PCMCIA drive enable.
57	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset).
58	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset).
59	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset).
60	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
61	3.3V_uP_SRAM	I	uP and SRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
62	3.3V_uP_SRAM	I	uP and SRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
63	3.3V_uP_SRAM	I	uP and SRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.

Pin #	Signal Name	I/O	Description
64	3.3V_uP_SRAM	I	uP and SRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
65	uP_SPI_FRM	O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI data transmission or reception. This signal is pulled-up internally on the LH75401 processor
66	uP_BUS_CLK	O	Bus clock. Operates at 25MHz. Do not connect to any loads unless first buffered for extended fanout.
67	uP_SPI_MOSI_TX	O	This output transmits synchronous SPI data. This signal is pulled-down internally on the LH75401 processor
68	DGND	I	Digital Ground (0V)
69	uP_SPI_MISO_RX	I[1]	This input receives synchronous SPI data. This signal is pulled-up internally on the LH75401 processor
70		NC	No internal connection (not implemented on the LH75401-10/11)
71	uP_SPI_SCK	O	SPI clock signal. SPI transmit/receive data is valid on the rising edge of this clock (data is output from one falling edge to the next and clocked in on the rising edge). This signal is pulled-down internally on the LH75401 processor
72		NC	No internal connection (not implemented on the LH75401-10/11)
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74		NC	No internal connection (not implemented on the LH75401-10/11)
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76		NC	No internal connection (not implemented on the LH75401-10/11)
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMBLE1	O	Active low. Buffered write enable for buffered data bus bits 15->8 - PCMCIA WE - DQM1 SRAM signal from the LH75401. All functions are valid (functionality changes based on memory area accessed).
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMBLE0	O	Active low. Buffered write enable for buffered data bus bits 7->0 - DQM0 SRAM signal from the LH75401. Both functions are valid (functionality changes based on memory area accessed)
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active low. When low, this buffered signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal can be used for buffer direction control.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	Active low. This buffered signal is the read strobe that latches data output from external peripherals. It is also the PCMCIA OE signal when areas 5 or 6 are accessed in PCMCIA mode.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the LH75401-10/11)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection (not implemented on the LH75401-10/11)
89	DGND	I	Digital Ground (0V)
90	uP_MA0	I/O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	I/O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	I/O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	I/O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	I/O	Buffered Address Bus bit 4.

Pin #	Signal Name	I/O	Description
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	I/O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	I/O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	I/O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	I/O	Buffered Address Bus bit 8.
107	VDD3.3V	I	Power Supply (3.3V)
108	uP_MA9	I/O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	I/O	Buffered Address Bus bit 10.
111		NC	No internal connection (not implemented on the LH75401-10/11)
112	uP_MA11	I/O	Buffered Address Bus bit 11.
113		NC	No internal connection (not implemented on the LH75401-10/11)
114	uP_MA12	I/O	Buffered Address Bus bit 12.
115		NC	No internal connection (not implemented on the LH75401-10/11)
116	uP_MA13	I/O	Buffered Address Bus bit 13.
117		NC	No internal connection (not implemented on the LH75401-10/11)
118	uP_MA14	I/O	Buffered Address Bus bit 14.
119		NC	No internal connection (not implemented on the LH75401-10/11)
120	uP_MA15	I/O	Buffered Address Bus bit 15.
121		NC	No internal connection (not implemented on the LH75401-10/11)
122	uP_MA16	I/O	Buffered Address Bus bit 16.
123		NC	No internal connection (not implemented on the LH75401-10/11)
124	uP_MA17	I/O	Buffered Address Bus bit 17.
125		NC	No internal connection (not implemented on the LH75401-10/11)
126	uP_MA18	I/O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	Pulled Down	I	This Signal is pulled-down to DGND through a 10K resistor.
129		NC	No internal connection (not implemented on the LH75401-10/11)
130	uP_MA19	I/O	Buffered Address Bus bit 19.
131		NC	No internal connection (not implemented on the LH75401-10/11)
132	uP_MA20	I/O	Buffered Address Bus bit 20.
133		NC	No internal connection (not implemented on the LH75401-10/11)
134	uP_MA21	I/O	Buffered Address Bus bit 21.
135		NC	No internal connection (not implemented on the LH75401-10/11)
136	uP_MA22	I/O	Buffered Address Bus bit 22.
137		NC	No internal connection (not implemented on the LH75401-10/11)
138	Pulled Down	I	This Signal is pulled-down to DGND through a 10K resistor.
139		NC	No internal connection (not implemented on the LH75401-10/11)
140	uP_MA23	I/O	Buffered Address Bus bit 23.
141		NC	No internal connection (not implemented on the LH75401-10/11)
142	NAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143		NC	No internal connection (not implemented on the LH75401-10/11)
144	VDD3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC – LCD_SPS	O	LCD Vsync/ Frame line marker (active state selectable) || General purpose I/O PTE3.
2	LCD_HSYNC – LCD_HRLP	O	LCD Hsync/ Line clock (active state selectable) || General purpose I/O PTD5.
3	LCD_DCLK	O	LCD data clock || General purpose I/O PTH7.
4	LCD_REV - LCD_DON	O	Active high. LCD display on signal || General purpose I/O PTD7.
5	LCD_MDISP	O	LCD current alternating signal/LCD enable signal || General purpose I/O PTE6.
6	LCD_VEEEN – LCD_MOD	O	Active high. LCD panel Vee enable. This signal is tied to J1A- #15
7	LCD_VDDEN	O	Active high. LCD panel Vcc enable.
8		NC	No internal connection
9	DGND	I	Digital Ground (0V)
10	LCD_CLS - PG1	O	LCDCLS Signal Output – This signal is only used with a HR-TFT interface.
11	LCD_VSYNC - LCD_SPS	O	LCDFP Signal Output – This signal is only used with a HR-TFT interface.
12	LCD_PSAVE - PG0	O	LCDPS Signal Output –This signal is only used with a HR-TFT interface.
13		NC	No internal connection (not implemented on the LH75401-10/11)
14	LCD_HSYNC - LCD_HRLP	O	LCDHSYNC/ Line clock (active state selectable) || General purpose I/O PTD5.
15	LCD_VEEEN - LCD_MOD	O	This signal is tied to J1A-#6. LCDMOD is only used with a HR-TFT interface
16	LCD_REV – LCD_DON – PG2	O	Active high. LCD display on signal || General purpose I/O PTD7.
17	uP_STATUS_1 – PF1/CTCAP0D	O	Processor status pin. UP_STATUS_1 can be used to output various states the card engine is in.
18	uP_STATUS_2 – PF2/CTCAP0E	O	Processor status pin. UP_STATUS_2 can be used to output various states the card engine is in.
19		NC	No internal connection (not implemented on the LH75401-10/11)
20		NC	No internal connection (not implemented on the LH75401-10/11)
21		NC	No internal connection (not implemented on the LH75401-10/11)
22		NC	No internal connection (not implemented on the LH75401-10/11)
23		NC	No internal connection (not implemented on the LH75401-10/11)
24	DGND	I	Digital Ground (0V)
25	uP_A/D4	I	Analog input: 0 to 3.3V swing possible.
26	uP_A/D9	I	Analog input: 0 to 3.3V swing possible
27	AGND	I	Analog Ground (0V)
28	HP_OUTL	O	Left stereo mixer-channel amplified headphone output.
29	HP_OUTR	O	Right stereo mixer-channel amplified headphone output.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line-in input of the audio CODEC. 1V RMS Typical, 2V RMS max (if current limited to 1mA or less).
32	CODEC_INR	I	Right channel stereo line-in input of the audio CODEC. 1V RMS Typical, 2V RMS max (if current limited to 1mA or less).
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
35	AGND	I	Analog Ground (0V)

Pin #	Signal Name	I/O	Description
36	TOUCH_LEFT	I	Four wire resistive touch panel left position connection.
37	TOUCH_RIGHT	I	Four wire resistive touch panel right position connection.
38	TOUCH_BOTTOM	I	Four wire resistive touch panel bottom position connection.
39	TOUCH_TOP	I	Four wire resistive touch panel top position connection.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0 – R4	O	The LCD data bus used to transmit data to the LCD module.
42	R1 – R5	O	The LCD data bus used to transmit data to the LCD module. RED 1.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5.
48	G0 – G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 0.
49	G1 – G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 1.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5.
54	B0 – B4	O	The LCD data bus used to transmit data to the LCD module.
55	DGND	I	Digital Ground (0V)
56	B1 – B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 1.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5.
61	CF_nCE	O[1]	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word operation to the card. See the LH75401-10/11 IO Controller Specification for further details.
62	RSVD_1	I	This signal is routed to the onboard CPLD and is reserved for future use. See the LH75401-10/11 IO Controller Specification for further details.
63	CPLD_GPIO_1	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD See the LH75401-10/11 IO Controller Specification for further details.
64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See the LH75401-10/11 IO Controller Specification for further details.
65		NC	No internal connection
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection (not implemented on the LH75401-10/11)
68		NC	No internal connection (not implemented on the LH75401-10/11)
69		NC	No internal connection (not implemented on the LH75401-10/11)
70		NC	No internal connection (not implemented on the LH75401-10/11)
71		NC	No internal connection (not implemented on the LH75401-10/11)
72		NC	No internal connection (not implemented on the LH75401-10/11)
73		NC	No internal connection (not implemented on the LH75401-10/11)
74	BUFF_nOE	O[1]	Active low. Controls the outputs of the buffers on the card engine. When low, the buffers are active, when high, the buffers will be tri-state. See the LH75401-/11 IO Controller Specification for further details.
75		NC	No internal connection (not implemented on the LH75401-10/11)

Pin #	Signal Name	I/O	Description
76	BUFF_DIR_DATA	O	Active high/low. Controls the direction of the data lines through the buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). See the LH75401-10/11 IO Controller Specification for further details.
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the LH75401-10/11)
79	POWER_SENSE1	I	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different card engines.
80	POWER_SENSE2	I	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK reference schematics for details on implementation if the design may require support for different card engines.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I[2]	This is the test clock input for the CPLD JTAG port. This signal has a 10k pull down on the card engine.
2	CPLD_TDO	O[1]	This input transmits data out of the CPLD JTAG port. This signal has a 10k pull up on the card engine.
3	CPLD_TMS	O[1]	This input indicates the mode of CPLD JTAG port. This signal has a 10k pull up on the card engine.
4	CPLD_TDI	I[1]	This input receives data on the CPLD JTAB port. This signal has a 10k pull up on the card engine.
5		NC	No internal connection (not implemented on the LH75401-10/11)
6		NC	No internal connection (not implemented on the LH75401-10/11)
7		NC	No internal connection (not implemented on the LH75401-10/11)
8		NC	No internal connection (not implemented on the LH75401-10/11)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the LH75401-10/11)
11		NC	No internal connection (not implemented on the LH75401-10/11)
12		NC	No internal connection (not implemented on the LH75401-10/11)
13		NC	No internal connection (not implemented on the LH75401-10/11)
14		NC	No internal connection (not implemented on the LH75401-10/11)
15		NC	No internal connection (not implemented on the LH75401-10/11)
16		NC	No internal connection (not implemented on the LH75401-10/11)
17		NC	No internal connection (not implemented on the LH75401-10/11)
18		NC	No internal connection (not implemented on the LH75401-10/11)
19		NC	No internal connection (not implemented on the LH75401-10/11)
20		NC	No internal connection (not implemented on the LH75401-10/11)
21	DGND	I	Digital Ground (0V)
22		NC	No internal connection (not implemented on the LH75401-10/11)
23		NC	No internal connection (not implemented on the LH75401-10/11)
24		NC	No internal connection (not implemented on the LH75401-10/11)
25		NC	No internal connection (not implemented on the LH75401-10/11)
26		NC	No internal connection (not implemented on the LH75401-10/11)
27		NC	No internal connection (not implemented on the LH75401-10/11)
28		NC	No internal connection (not implemented on the LH75401-10/11)

Pin #	Signal Name	I/O	Description
29		NC	No internal connection (not implemented on the LH75401-10/11)
30		NC	No internal connection (not implemented on the LH75401-10/11)
31		NC	No internal connection (not implemented on the LH75401-10/11)
32	DGND	I	Digital Ground (0V)
33		NC	No internal connection (not implemented on the LH75401-10/11)
34		NC	No internal connection (not implemented on the LH75401-10/11)
35		NC	No internal connection (not implemented on the LH75401-10/11)
36		NC	No internal connection (not implemented on the LH75401-10/11)
37		NC	No internal connection (not implemented on the LH75401-10/11)
38		NC	No internal connection (not implemented on the LH75401-10/11)
39		NC	No internal connection (not implemented on the LH75401-10/11)
40		NC	No internal connection (not implemented on the LH75401-10/11)
41	uP_UARTB_TX – IRQD	O	UART2 transmit output signal on the LH75401. This signal is internally pulled-up on the LH75401.
42	uP_UARTB_RX – IRQE	I	UART2 receive input signal on the LH75401. This signal is internally pulled-up on the LH75401.
43		NC	No internal connection (not implemented on the LH75401-10/11)
44	DGND	I	Digital Ground (0V)
45		NC	No internal connection (not implemented on the LH75401-10/11)
46	MFP16 – uP_UARTC_TX – CAN_TX – PE3	O	UART0 transmit output signal on the LH75401. This signal is internally pulled-up on the LH75401.
47	MFP17 – uP_UARTC_RX – CAN_RX – PE2	I	UART0 receive input signal on the LH75401. This signal is internally pulled-up on the LH75401.
48	MFP9 – uP_PG5/CTCLK	O	Common external clock
49	MFP10 – uP_PG6/CTCAP0A/CTCMP0A	O	Capture or Compare register A
50	MFP11 – uP_PG7/CTCAP0B/CTCMP0B	O	Capture or Compare register B
51	MFP12 – uP_PJ1	O	This signal is Port J1 which is also one of the analog I/O ports AN6 on the LH75401 processor.
52	MFP13 - uP_PJ3	O	This signal is Port J3 which is also one of the analog I/O ports AN8 on the LH75401 processor.
53		NC	No internal connection (not implemented on the LH75401-10/11)
54		NC	No internal connection (not implemented on the LH75401-10/11)
55	DGND	I	Digital Ground (0V)
56	MFP16 – uP_UARTC_TX – CAN_TX – PE3	O	UART0 transmit output signal on the LH75401. This signal is internally pulled-up on the LH75401.
57	MFP17 – uP_UARTC_RX – CAN_RX – PE2	I	UART0 receive input signal on the LH75401. This signal is internally pulled-up on the LH75401.
58	MFP18 – uP_PF6/CTCAP2B/CTCMP2B	I/O	This Signal is Port F6 on the LH75401 processor.
59	MFP19 – uP_PF5/CTCAP2A/CTCMP2A	I/O	This Signal is Port F5 on the LH75401 processor.
60	MFP20 – uP_PF4/CTCAP1B/CACMP1B	I/O	This Signal is Port F4 on the LH75401 processor.

Pin #	Signal Name	I/O	Description
61	MFP21 – CPLD_GPIO_3	I/O	This signal is a general purpose I/O. It is controlled by a memory mapped address in the CPLD. See the LH75401-10/11 IO Controller Specification for further details.
62		NC	No internal connection (not implemented on the LH75401-10/11)
63		NC	No internal connection (not implemented on the LH75401-10/11)
64		NC	No internal connection (not implemented on the LH75401-10/11)
65		NC	No internal connection (not implemented on the LH75401-10/11)
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection (not implemented on the LH75401-10/11)
68		NC	No internal connection (not implemented on the LH75401-10/11)
69		NC	No internal connection (not implemented on the LH75401-10/11)
70		NC	No internal connection (not implemented on the LH75401-10/11)
71		NC	No internal connection (not implemented on the LH75401-10/11)
72		NC	No internal connection (not implemented on the LH75401-10/11)
73	MFP32 – nRESETOUT	O	System Reset Output
74		NC	No internal connection (not implemented on the LH75401-10/11)
75	MFP34 – CODEC_CLKOUT	O	Specifically dealing the with the TLV320DAC23 Audio Codec, this is a buffered version of the external clock input to the Codec, available in 1x or 0.5x frequencies.
76		NC	No internal connection (not implemented on the LH75401-10/11)
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the LH75401-10/11)
79		NC	No internal connection (not implemented on the LH75401-10/11)
80	uP_RTCK	O	Returned JTAG test clock. This signal has a 10k pull up on the card engine.

5.4 Multiplexed Signal Trade-Offs

5.4.1 J1C Connector SO-DIMM 144-Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
43	uP_UARTA_TX – PE1	UARTTX1	Debug UART Output	PE1	Port E bit 1 I/O
45	uP_UARTA_RX – PE0	UARTRX1	Debug UART Input	PE0	Port E bit 0 I/O

5.4.2 J1A Expansion Connector Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1	LCD_VSYNC – LCD_SPS	LCDFP	LCDFP Signal Output	PH5 or LCDSPS	Port H bit 5 I/O or LCDSPS Signal Output
2	LCD_HSYNC – LCD_HRLP	LCDHRLP	LCDHRLP Signal Output	PH6	Port H bit 6 I/O
3	LCD_DCLK	LCDDCLK	LCD Clock Output	PH7	Port H bit 7 I/O
5	LCD_MDISP	LCDSPL	LCDSPL Signal Output	PH4 or LCDEN	Port H bit 4 I/O or LCDEN Signal Output
7	LCD_ VDDEN – PG3	LCDCLS	LCDCLS Signal Output	PG3	Port G bit 3 I/O
10	LCD_CLS – VDDEN – PG1	LCDCLS	LCDCLS Signal Output	PG1	Port G bit 1 I/O
11	LCD_VSYNC – LCD_SPS	LCDFP	LCDFP Signal Output	PH5 or LCDSPS	Port H bit 5 I/O or LCDSPS Signal Output
12	LCD_PSAVE – PG0	LCDPS	LCDPS Signal Output	PG0	Port G bit 0 I/O
14	LCD_HSYNC – LCD_HRLP	LCDLP	LCDLP Signal Output	PH6	Port H bit 6 I/O or LCD_HRLP Signal Output
15	LCD_VEEEN - LCD_MOD	LCDVEEEN	Analog Supply Enable	LCDMOD	HRTFT Output Signal used by the Row Driver.
16	LCD_REV – LCD_DON – PG2	LCDREV	LCDREV Signal Output	PG2 or LCDDSPLEN	Port G bit 2 I/O or LCDDSPLEN Signal Output
17	uP_STATUS_1 - PF1/CTCAP0D	PF1	Port F bit 1 I/O	CTCAP0D	CTCAP0D
60	LCD_D17	LCDVD17	LCD Data 17 I/O	PC6	Port C bit 6 I/O

5.4.3 J1B Expansion Connector Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
41	uP_UARTB_TX - IRQD	UARTTX1	UART B TX Output Only	UARTIRTX0	IRDA TX Output Only
42	uP_UARTB_RX – IRQE	UARTRX1	UART B RX Input Only	UARTIRRX0	IRDA RX Input Only
46	MFP16 - uP_UARTC_TX - CAN_TX - PE3	UARTTX0	UART C TX	PE3 or CAN_TX	PORT E bit 3 or CAN transmit output signal
47	MFP17 -	UARTRX0	UART C RX	PE2 or	PORT E bit 2 or receive input

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
	uP_UARTC_RX - CAN_RX - PE2			CAN_RX	signal
48	MFP9 - uP_PG5/CTCLK	PG5	Port G bit 5	CTCLK	Common External clock
49	MFP10 - uP_PG6/CTCAP0A/CTCMP0A	PG6	Port G bit 6	CTCAP0A or CTCMP0A	Timer 0 Capture input or Timer 0 Compare output
50	MFP11 - uP_PG7/CTCAP0B/CTCMP0B	PG7	Port G bit 7	CTCAP0B or CTCMP0B	Timer 0 Capture input or Timer 0 Compare output
56	MFP16 - uP_UARTC_TX - CAN_TX - PE3	UARTTX0	UART0 transmit output signal	PE3 or CAN_TX	Port E bit 3 or CAN controller transmit output signal
57	MFP17 - uP_UARTC_RX - CAN_RX - PE2	UARTRX0	UART0 receive input signal	PE2 or CAN_RX	Port E bit 2 or CAN controller receive input signal
58	MFP18 - uP_PF6/CTCAP2B/CTCMP2B	PF6	Port F bit 6	CTCAP2B or CTCMP2B	Timer 2 Capture input or Timer 2 Compare output
59	MFP19 - uP_PF5/CTCAP2A/CTCMP2A	PF5	Port F bit 5	CTCAP2A or CTCMP2A	Timer 2 Capture input or Timer 2 Compare output
60	MFP20 - uP_PF4/CTCAP1B/CACMP1B	PF4	Port F bit 4	CTCAP1B or CTCMP1B	Timer 1 Capture input or Timer 1 Compare output

6 Mechanical Specifications

6.1 Interface Connectors

The LH75401-10/11 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM Connector must be 3.7mm mating height.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

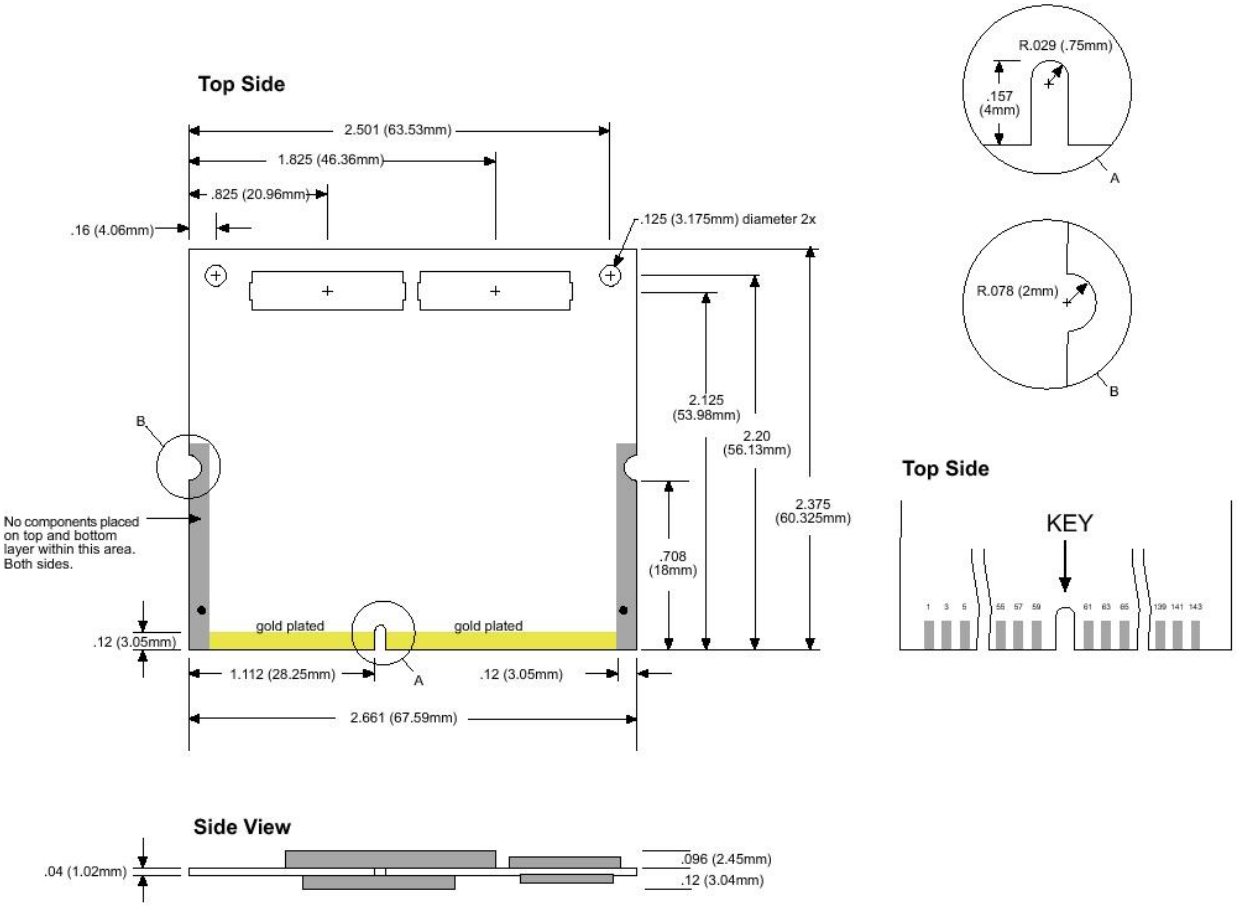


Figure 6.1: Card Engine Mechanical Drawing

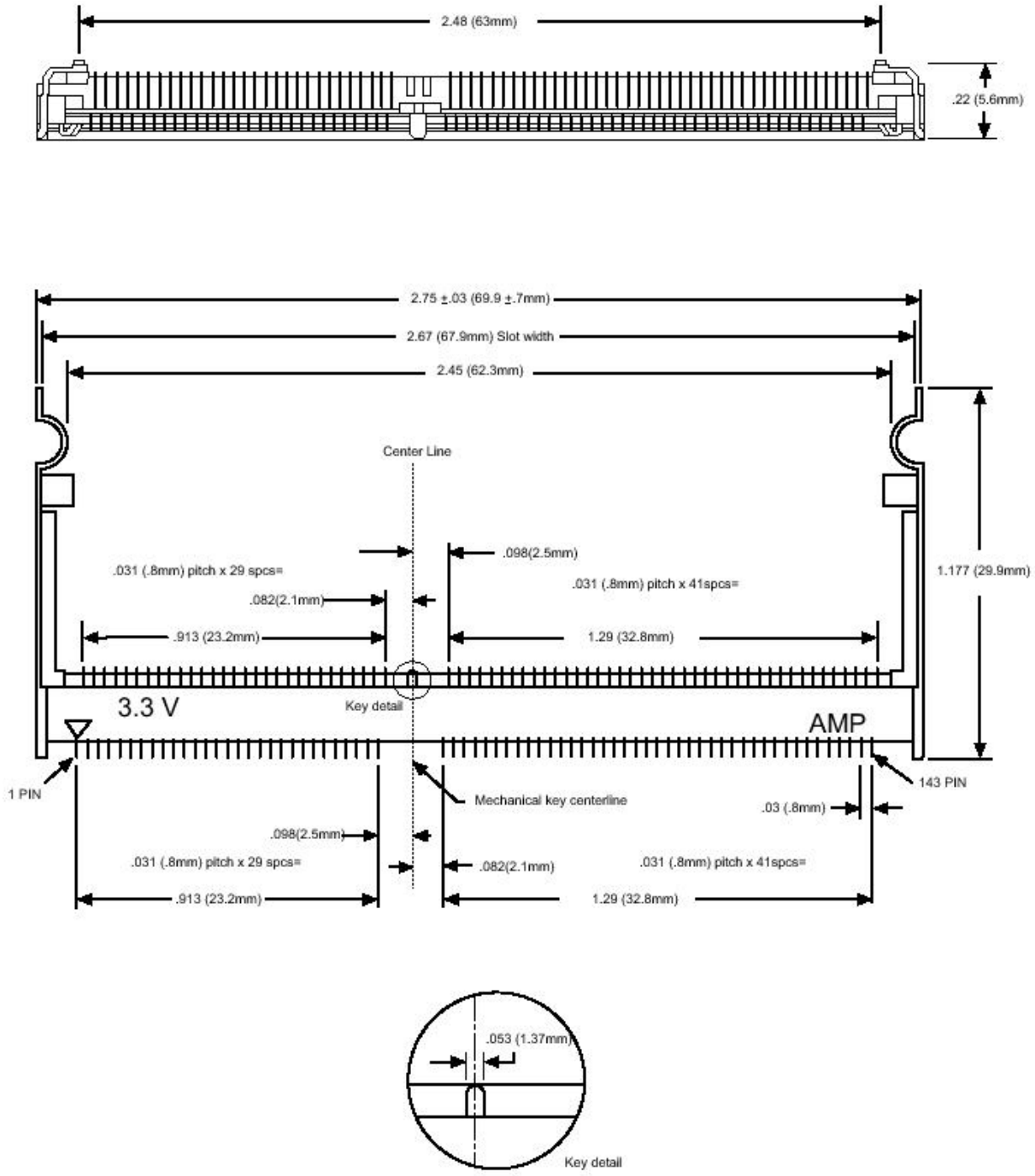


Figure 6.2: SODIMM Connector Specification

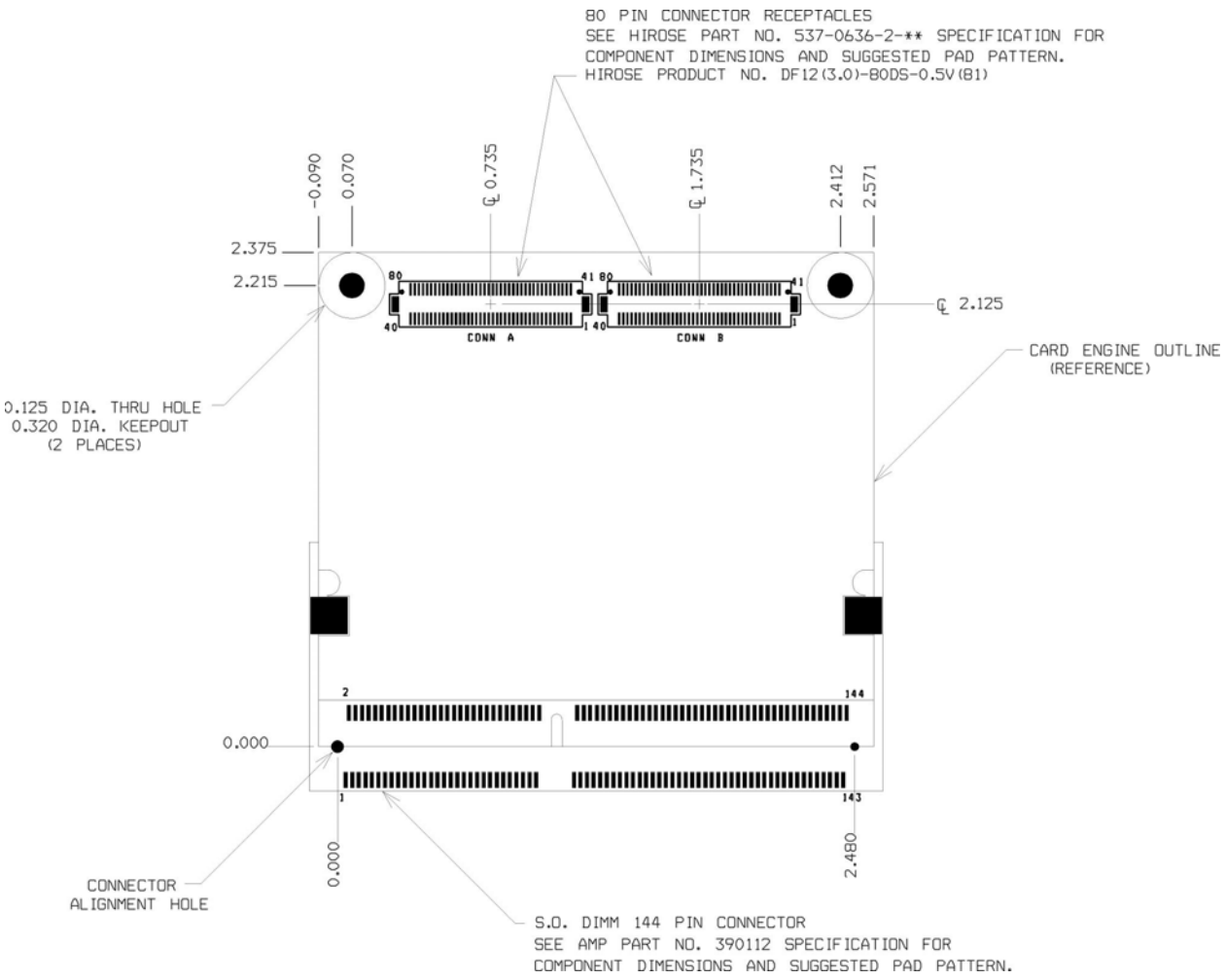


Figure 6.3: Recommended PCB Layout

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