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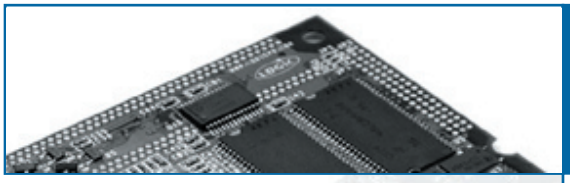

Zoom™

Card Engine

LH79524-10 Card Engine
IO Controller Specification

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CPLD REV	APPROVAL	DATE
A	Nathan Kro	Initial Release	---	KTL	8/30/04
B	James Wicks	Section 3.1.14 Correction: GPIO1 active bit 1 description.	0_6	KTL	9/10/04
C	Kurt Larson	Updated register and bit locations to match previous products	0_7	KTL	10/12/04
D	Kurt Larson	NAND flash updates	0_B	KTL	11/12/04
E	James Wicks	Updated Product Brief Section	0_B	KTL	12/08/04
F	Jed Anderson	Added note to reference App Note 303 in Section 4	0_B	JCA	12/30/05

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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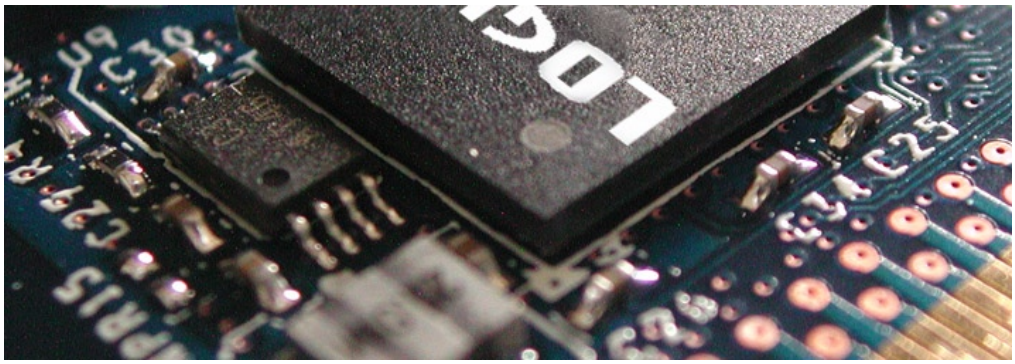
LH79524-10 I/O CONTROLLER

Logic offers production-ready I/O controller devices and design packages for customers cerating custom Card Engine designs and CPLD code for Logic's Card Engines. Logic has optimized the VHDL code to fit in the smallest possible programmable logic device. This results in an embedded product development cycle with **less time, less cost, less risk ... more innovation.**



- **I/O Controller was written in VHDL and contains the following:**
  - SPI interface to onboard EEPROMS and Audio Codec
  - CF Card Support (memory mode only)
  - ISA-like bus interface
  - Buffer control logic
  - Chip select decoder logic
  - Interrupt encoder logic
  - Flash program control logic
  - Processor mode control logic
  - IC code revision register
  - Additional GPIO
  - Status indicator signals
  - On-board power management signals
  - Memory mapped NAND flash controller

- **Source Code**
  - includes all VHDL code (licensable .vhd source code files)

- **Ordering Information**
  - The I/O Controller design package is available as part of the SOM Hardware Design Package. For more information, please contact Logic Sales at product.sales@logicpd.com.

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

For more information on our EmbeddedProduct Solutions, please contact Logic Sales at www.logicpd.com or 612.672.9495.

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PN: 1001030 Rev A

1.2 Acronyms

BALE	Buffered Address Latch Enable
CF	CompactFlash
CS	Chip Select
GPIO	General Purpose Input Output
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Electrically Programmable Read Only Memory
IO	Input Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LAN	Local Area Network
LED	Light Emitting Diode
MB	Megabyte (2^20 bytes)
SPI	Serial Peripheral Interface

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Xilinx XC2C128 CoolRunner-II CPLD data sheet (DS093)
- Xilinx Device Package Information data sheet (UG112)
- Xilinx Ordering Information

1.4 IO Controller Advantages

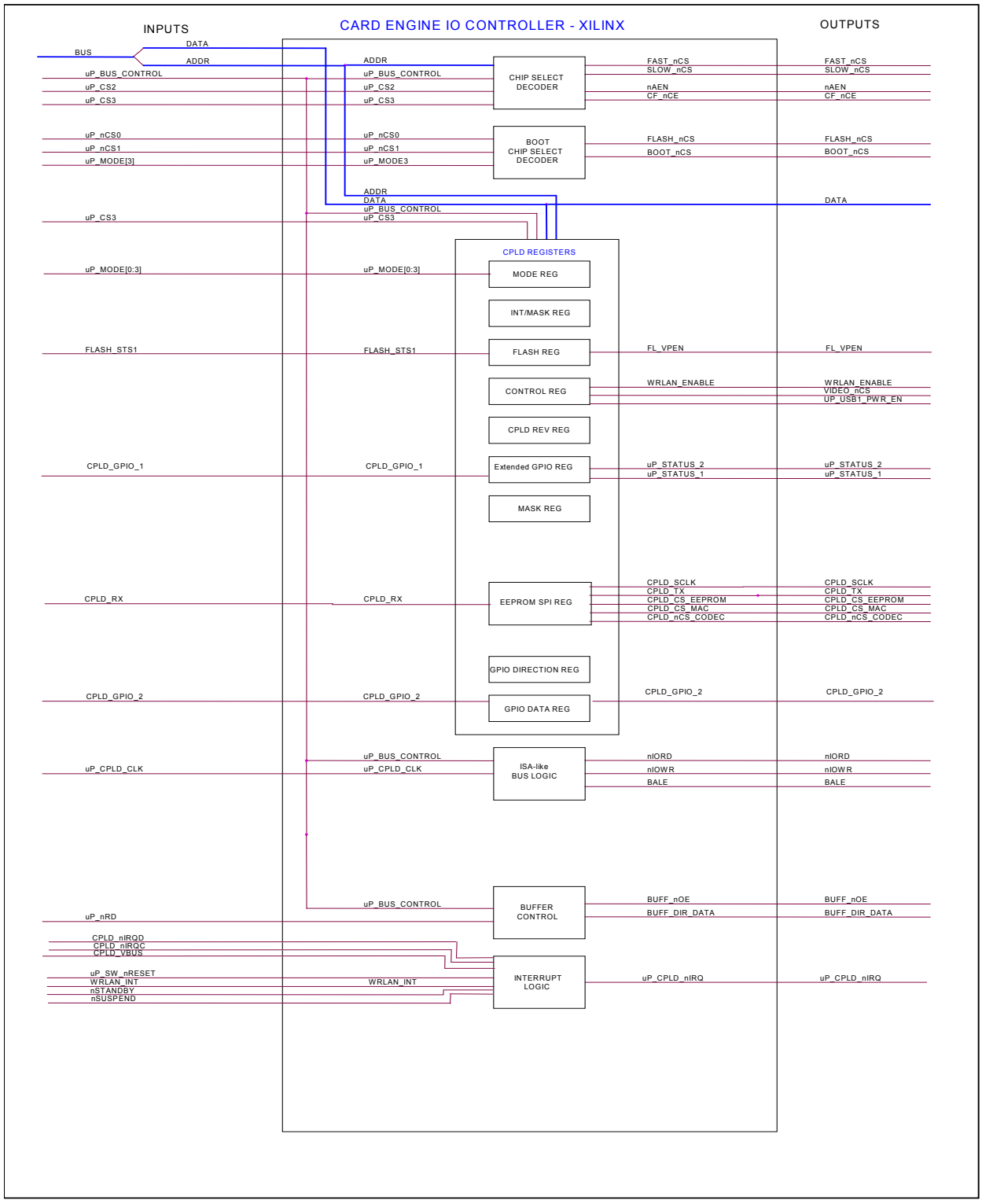
Some of the key features in the IO Controller include:

- Multiple Parallel to SPI Interface
- Chip Select Decoder
- Interrupt Decoder
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player

The IO Controller VHDL source code is available for purchase. Contact Logic for more information.

2 IO Controller Block Diagram

Figure 2.1: IO Controller Block Diagram



3 IO Controller Address and Register Definitions

Address Range	Memory Block Description	Size
0x4C00 0000 – 0x4FFF FFFF	Fast Peripherals Chip Select 3 (CS3)	32MB
0x4800 0000 – 0x49FF FFFF	Slow Peripherals Chip Select 2 (CS2)	32MB

3.1 Fast Peripherals Chip Select 3 (CS3)

Address Range	Memory Block Description	Size
0x4C00 0000 – 0x4C0F FFFF	Reserved	1MB
0x4C10 0000 – 0x4C1F FFFF	Card Engine Control Reg	1MB
0x4C20 0000 – 0x4C2F FFFF	Reserved	1MB
0x4C30 0000 – 0x4C3F FFFF	Reserved	1MB
0x4C40 0000 – 0x4C4F FFFF	Reserved	1MB
0x4C50 0000 – 0x4C5F FFFF	EEPROM/SPI Reg	1MB
0x4C60 0000 – 0x4C6F FFFF	Interrupt & Mask Reg	1MB
0x4C70 0000 – 0x4C7F FFFF	Mode Reg	1MB
0x4C80 0000 – 0x4C8F FFFF	Flash Reg	1MB
0x4C90 0000 – 0x4C9F FFFF	Power Reg	1MB
0x4CA0 0000 – 0x4CAF FFFF	IO Controller Code Revision Reg	1MB
0x4CB0 0000 – 0x4CBF FFFF	Extended GPIO Reg	1MB
0x4CC0 0000 – 0x4CCF FFFF	GPIO Data Reg	1MB
0x4CD0 0000 – 0x4CDF FFFF	GPIO Direction Reg	1MB
0x4CE0 0000 – 0x4CEF FFFF	Reserved - On-Board Expansion	1MB
0x4CF0 0000 – 0x4CFF FFFF	Reserved - Off-Board Expansion	1MB
0x4D00 0000 – 0x4FFF FFFF	Open – Available for User	16MB

Each memory block for chip select 3 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.1.1 Reserved

Address Range: 0x4C00 0000 – 0x4C0F FFFF

- This memory block is reserved.

3.1.2 Card Engine Control Register

Address Range: 0x4C10 0000 – 0x4C1F FFFF

- This register holds control bits for the card engine.

7	6	5	4	3	2	1	0	
nSWINT	0	0	0	USB1P	0	0	WRLAN_ENABLE	
1	0	0	0	1	0	0	0	reset
R/W	R	R	R	R/W	R	R	R/W	R/W

nSWINT: Software interrupt. This bit can be set in the CPLD to force the uP_CPLD_nIRQ bit low back to the processor to create a software interrupt. This bit functions independently of all other interrupts and is not required to be set or cleared in order to receive interrupts from other CPLD sources.
0 = Create an interrupt on this signal.
1 = Do not create a software interrupt.

USB1P: Power enable for USB1. A USB driver should drive this bit low during initialization. It will allow a connection interrupt to be generated on the USB_VBUS bit when a USB cable is plugged into the adapter board and another powered device.
0 = USB power enabled
1 = USB power disabled

WRLAN_ENABLE: Wired LAN power enable signal. This bit puts the ethernet twisted pair port into power-down mode.
0 = Wired LAN powered down
1 = Wired LAN enabled

3.1.3 Reserved

Address Range: 0x4C20 0000 – 0x4C2F FFFF

- This memory block is reserved.

3.1.4 Reserved

Address Range: 0x4C30 0000 – 0x4C3F FFFF

- This memory block is reserved.

3.1.5 Reserved

Address Range: 0x4C40 0000 – 0x4C4F FFFF

This memory block is reserved.

3.1.6 EEPROM/SPI Interface Register

Address Range: 0x4C50 0000 – 0x4C5F FFFF

- This register holds SPI data during a read/write between the processor and on-board EEPROM. This SPI interface used for the EEPROM is directly controlled by the processor and is not timed by the IO Controller.

7	6	5	4	
0	0	CPLD_CS_nCODEC	CPLD_CS_MAC	
0	0	1	0	reset
R	R	R/W	R/W	R/W

3	2	1	0	
CPLD_CS_EEPROM	CPLD_SCLK	CPLD_TX	CPLD_RX	
0	0	0	X	reset
R/W	R/W	R/W	R	R/W

CPLD_CS_nCODEC: Onboard CODEC chip select.
0 = CODEC chip selected for serial communication
1 = CODEC is not selected

CPLD_CS_MAC: Onboard EEPROM chip select intended for MAC Address storage.
0 = not selected
1 = MAC Address EEPROM chip selected for serial communication

CPLD_CS_EEPROM: Onboard EEPROM chip select for generic data storage. Logic's LogicLoader software uses this EEPROM for boot script storage.
0 = not selected
1 = EEPROM chip selected for serial communication

CPLD_SCLK: Used for a SPI clock signal to onboard devices.
0 = Drives the external CPLD_SCLK signal low
1 = Drives the external CPLD_SCLK signal high

CPLD_TX: CPLD SPI data transmit to onboard peripherals.
0 = Drives the external CPLD_TX signal low
1 = Drives the external CPLD_TX signal high

CPLD_RX: CPLD SPI data receive from onboard peripherals.
0 = Indicates a low level was read on the CPLD_RX pin
1 = Indicates a high level was read on the CPLD_RX pin

3.1.7 Interrupt & Mask Register

Address Range: 0x4C60 0000 – 0x4C6F FFFF

- This register contains the bits used by the IO Controller to generate an interrupt to the processor via net uP_CPLD_nIRQ. The bits in this register are not latched. Upon reading this register, the actual state of the corresponding interrupt will be returned.

7	6	5	4	
CMSK	nIRQC	nIRQD	USB_VBUS	
1	x	x	x	Reset
R/W	R	R	R	R/W

3	2	1	0	
UMSK	WMSK	DMSK	WRLAN_nINT	
1	1	1	x	Reset
R/W	R/W	R/W	R	R/W

CMSK: Masks CPLD_nIRQC interrupt.
0 = IRQC is not masked
1 = IRQC is masked

nIRQC: IRQC interrupt. An external source is requesting an interrupt.
0 = An interrupt is being asserted on this signal
1 = No interrupt

nIRQD: IRQD interrupt. An external source is requesting an interrupt.
0 = An interrupt is being asserted on this signal
1 = No interrupt

USB_VBUS: USB insertion interrupt. Active High.
0 = Interrupt occurring, device is inserted
1 = No interrupt
* External signal is inverted in CPLD to make register interface active low

UMSK: Masks USB_VBUS interrupt.
0 = USB_OVRNCRNT is not masked
1 = USB_OVRNCRNT is masked

WMSK: Masks WRLAN_nINT interrupt.
0 = WRLAN_nINT is not masked
1 = WRLAN_nINT is masked

DMSK: Masks CPLD_nIRQD interrupt.
0 = IRQD is not masked
1 = IRQD is masked

WRLAN_nINT: Wired LAN interrupt.
0 = Wired LAN peripheral is requesting an interrupt
1 = No interrupt

3.1.8 Mode Register

Address Range: 0x4C70 0000 – 0x4C7F FFFF

- Reading this register will return the current state of the mode pins.

7	6	5	4	
0	0	0	0	
0	0	0	0	reset
R	R	R	R	R

3	2	1	0	
uP_MODE3	uP_MODE2	uP_MODE1	uP_MODE0	
x	x	x	x	reset
R	R	R	R	R

uP_MODE3: mode pin 3. Mode pin 3 selects between on-board and off-board boot device. See Section 4.2 for detailed information on mode pin 3.
0 = Selects off-board boot device on BOOT_nCS
1 = Selects on-board boot device (flash memory) on FLASH_nCS

uP_MODE2: mode pin 2. Mode pin 2 represents the endian setting for the processor. (The LH79524 supports little endian only. The value of this bit is ignored.) The user can use this pin as a generic input signal.
0 = Big endian (this bit can only be read and has no affect on card engine)
1 = Little endian (this bit can only be read and has no affect on card engine)

uP_MODE1, uP_MODE0: mode pin 1 and mode pin 0. These mode pins represent the bus width at boot. Bit uP_MODE0 is the latched value of uP_A21 at reset and bit uP_MODE1 is the latched value of uP_A22 at reset.

(Note: See LH79524 datasheet for specific setting options at boot time.)

3.1.9 Flash Register

Address Range: 0x4C80 0000 – 0x4C8F FFFF

- This register holds status information for the flash.

7	6	5	4	3	2	1	0	
0	NANDSPD	0	0	FPOP	RDYnBSY	STS1	FL_VPEN	
0	1	0	0	1	x	x	0	reset
R	R/W	R	R	R/W	R	R	R/W	R/W

NANDSPD: NAND operation mode
0 = Clearing this bit allows user to use nCS0/PM0 signal as nCS0 for NAND_nCE. NAND_nRE and NAND_nWE signals are based on processor nOE and nWE signals qualified by nCS0, which alleviates the restriction of staying in memory areas limited by A23 and A22 while using the NAND interface
1 = This mode is the default on reset and allows user to use A23 and A22 to drive the NAND_nRE and NANND_nWE signals while using nCS0/PM0 pin as PM0 for NAND_nCE

FPOP: Flash selection bit. This bit is set to 1 by default on reset
0 = Boot from NOR flash in area 1, NAND flash device is in area 0 when Mode Pin 3 = 1. Boot from off-board NOR device in area 1, NAND flash is in area 0 when Mode Pin 3 = 0
1 = Boot from NOR flash in area 1, off-board memory device is in area 0 when Mode Pin 3 = 1. Boot from off-board NOR device in area 1, NOR flash is in area 0 when Mode Pin 3 = 0

RDYnBSY: Flash status pin. This is the RY/BY# pin for the upper 16 bit flash chip.
0 = Flash busy
1 = Flash ready

STS1: Flash status pin. This is the RY/BY# pin for the lower 16 bit flash chip.
0 = Flash busy
1 = Flash ready

FL_VPEN: Flash program enable.
0 = normal flash operations
1 = program flash enabled

3.1.10 Power Register

Address: 0x4C90 0000 – 0x4C9F FFFF

- This register reflects the state of power-related signals on the LH79524-10. When any of these signals are low, the net "uP_CPLD_nIRQ" will be driven low in order to interrupt the processor.

7	6	5	4	3	2	1	0	
0	0	0	nSTANDBY	0	nSUSPEND	SW_nRESET	0	
0	0	0	x	0	x	X	0	reset
R	R	R	R	R	R	R	R	R/W

nSTANDBY: Standby interrupt. An external request is being made to enter standby state.
0 = An interrupt is being asserted on this signal
1 = No interrupt

nSUSPEND: Suspend interrupt. An external request is being made to enter suspend state.
0 = An interrupt is being asserted on this signal
1 = No interrupt

SW_nRESET: Software reset interrupt. An external software reset is being requested.
0 = An interrupt is being asserted on this signal
1 = No interrupt

3.1.11 IO Controller Code Revision Register

Address Range: 0x4CA0 0000 – 0x4CAF FFFF

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								reset
R								R

3.1.12 Extended GPIO Register

Address Range: 0x4CB0 0000 – 0x4CBF FFFF

- This register controls status LED's.

7	6	5	4	3	2	1	0	
0	0	0	0	0	LED1	LED2	GPIO_1	
0	0	0	0	0	1	1	1	reset
R	R	R	R	R	R/W	R/W	R/W	R/W

LED1: LED1 output bit (net uP_STATUS_2).
0 = Drive uP_STATUS_2 low

1 = Allow uP_STATUS_2 to float to High-Z state so the pin can be driven external and read from the CPLD as an input

LED2: LED2 output bit (net uP_STATUS_1).
0 = Drive uP_STATUS_1 low
1 = Allow uP_STATUS_1 to float to High-Z state so the pin can be driven external and read from the CPLD as an input

CPLD_GPIO_1: Controls state of general purpose input/output bit CPLD_GPIO_1. Outputs register value when configured as output, reads pin state when configured as input.
0 = Set pin low if configured as output, read pin state low if configured as input (See GPIO Direction Reg bit 0)
1 = Set pin high if configured as output, read pin state high if configured as input(See GPIO Direction Reg bit 0)

3.1.13 GPIO Data Register

Address: 0x4CC0 0000 – 0x4CCF FFFF

- This register controls the state of the CPLD general-purpose input/output pin 2 (CPLD_GPIO_2). Note: The direction (input or output) of the CPLD pins are set in the GPIO Direction Register in Section 3.1.14.

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	CPLD_GPIO_2	
0	0	0	0	0	0	0	1	reset
R	R	R	R	R	R	R	R/W	R/W

CPLD_GPIO_2: Controls state of general purpose input/output bit CPLD_GPIO_2. Outputs register value when configured as output, reads pin state when configured as input.
0 = Set pin low if configured as output, read pin state low if configured as input (See GPIO Direction Reg bit 1)
1 = Set pin high if configured as output, read pin state high if configured as input (See GPIO Direction Reg bit 1)

3.1.14 GPIO Direction Register

Address: 0x4CD0 0000 – 0x4CDF FFFF

- This register controls the direction for the CPLD general purpose input/output pins. Note: The value (high or low) of the CPLD pins are read/written in the GPIO Data Register in Section 3.1.13 and the Extended GPIO register in Section 3.1.12.

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	GPIO1	GPIO2	
0	0	0	0	0	0	1	1	reset
R	R	R	R	R	R	R/W	R/W	R/W

GPIO1: GPIO1 active bit 1.

0 = External CPLD signal CPLD_GPIO_1 is an output
1 = External CPLD signal CPLD_GPIO_1 is an input

GPIO2: GPIO2 direction bit 2.
0 = External CPLD signal CPLD_GPIO_2 is an output
1 = External CPLD signal CPLD_GPIO_2 is an input

3.1.15 Reserved On-Board Memory Blocks

Address Range: 0x4CE0 0000 – 0x4CEF FFFF

- These two memory blocks are reserved for future on-board expansion.

3.1.16 Reserved Off-Board Memory Blocks

Address Range: 0x4CF0 0000 – 0x4CFF FFFF

- These sixteen memory blocks are reserved for off-board IO controller expansion.

3.1.17 Open Memory Blocks – Available for User

Address Range: 0x4D00 0000 – 0x4FFF FFFF

- These sixteen 1MB memory blocks are open and available for the user to utilize. Accesses to these areas assert FAST_nCS chip select, found on the card engine at J1C.

3.2 Slow Peripherals Chip Select 2 (CS2)

Address Range	Memory Block Description	Size
0x4800 0000 – 0x481F FFFF	Reserved	2MB
0x4820 0000 – 0x483F FFFF	CF Chip Select	2MB
0x4840 0000 – 0x485F FFFF	ISA-like Bus Chip Select	2MB
0x4860 0000 – 0x48AF FFFF	Reserved - On-Board Expansion	(1MB)x5
0x48B0 0000 – 0x48FF FFFF	Reserved - Off-Board Expansion	(1MB)x5
0x4900 0000 – 0x49FF FFFF	Open – Available for User	16MB

Each memory block for chip select 2 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.2.1 CompactFlash (CF) Chip Select

Address Range: 0x4820 0000 – 0x483F FFFF

- This area of memory is used when accessing the off-board memory mapped CompactFlash Type 1 Memory Only slot. Accesses to this address range assert the external card enable net CF_nCE, nIORD, and nIOWR.

3.2.2 ISA-like Bus Chip Select

Address Range: 0x4840 0000 – 0x485F FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 5 for read and write timing diagrams.

3.2.3 Reserved On-Board Memory Blocks

Address Range: 0x4860 0000 – 0x48AF FFFF

- These memory blocks are reserved for future on-board expansion.

3.2.4 Reserved Off-Board Memory Blocks

Address Range: 0x48B0 0000 – 0x48FF FFFF

- These memory blocks are reserved for off-board IO controller expansion.

3.2.5 Open Memory Blocks – Available for User

Address Range: 0x4900 0000 – 0x49FF FFFF

- These memory blocks are open and available for the user to utilize. Accesses to these areas assert SLOW_nCS chip select, found on the card engine at J1C.

4 IO Controller Functions

This section describes the different IO Controller function blocks. See Section 2 for the IO Controller block diagram.

Note: A specific software protocol must be followed to access IO devices on Sharp Card Engines. Please see Logic's Application Note 303: *Interfacing to IO Devices via the Static Memory Controller on LH7xxxx Card Engines* for examples of the protocol when accessing registers within the CPLD. This document can be found at: https://www.logicpd.com/auth/.

4.1 Chip Select Decoder Logic

This logic decodes processor chip selects 2 and 3 into smaller segments of memory. See Section 3.1 for the chip select 3 memory map, and Section 3.2 for the chip select 2 memory map.

CPLD signal FAST_nCS is output when uP_CS3 is low and uP_MA23 is high. CPLD signal SLOW_nCS is output when uP_CS2 is low and uP_MA23 is high. Signals FAST_nCS and SLOW_nCS are brought off the card engine through the expansion bus connectors.

4.2 Boot Chip Select Decoder Logic

Note: Mode pin 3 (uP_MODE3) selects between on-board and off-board boot device.

The card engine can boot from on-board NOR or NAND flash or an off-board memory device. The boot device selection is determined by a jumper setting (mode pin 3) on the application board. The boot device is located in area 1 (CS1) or area 0 (CS0) depending on the LH79524 boot configuration. The CPLD implements the following table.

Flash register bit (3) is used to generate the flash chip selects. See Section 3.1.9 for more information on the flash register.

NOR Flash (on-board) (FLASH_nCS)	NAND Flash (on-board) (NAND_nCE)	Off-board memory (BOOT_nCS)	Mode Pin 3	Flash Reg (3)	Function
CS1 (area 1)	CS0 (area 0)	Not Selectable	1	1	Boot from NOR flash in area 1, NAND flash device is in area 0.
CS1 (area 1)	Not Selectable	CS0 (area 0)	1	0	Boot from NOR flash in area 1, off-board memory device is in area 0.
Not Selectable	CS0 (area 0)	CS1 (area 1)	0	1	Boot from off-board NOR device in area 1, NAND flash is in area 0.
CS0 (area 0)	Not Selectable	CS1 (area 1)	0	0	Boot from off-board NOR device in area 1, NOR flash is in area 0.

The chip selects for area 0 and 1 are routed to the flash and off-board memory device by signals NAND_nCE, FLASH_nCS, and BOOT_nCS.

4.3 SPI Interface

4.3.1 Usage Notes

Communicate to onboard devices that require SPI communication by using the EEPROM/SPI Interface Register. The bits in this register directly control the input and output signals used to serial transmit and receive data to the devices.

Read and write to the register with data intended for output on the signals. For example, in order to transmit a high bit to the onboard CODEC, a starting value of 0b00100000 may be in the EEPROM/SPI register. Write 0b00000010 followed by 0b00000110 to the register. This will enable communication to the CODEC by asserting the CPLD_nCS_CODEC bit low, drive the

CPLD_TX bit high, then the second write will cause a rising edge on the CPLD_SCLK signal so the CODEC clocks in the CPLD_TX bit. A final write of 0b00100100 will terminate the single bit transfer to the CODEC.
To communicate with the onboard CODEC or EEPROM's, longer transfers are typically necessary, but will follow the same pattern.

Reading from the device can be accomplished by asserting the appropriate chip select, writing to the register to toggle the CPLD_SCLK bit, then reading from the register to find the new value of CPLD_RX that was asserted by the device.

4.4 ISA-like Bus Logic (CompactFlash and ISA Peripherals in Area 2)

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic outputs the ISA chip select, CompactFlash chip select, BALE, read (nIORD), and write (nIOWR) signals. It also creates two timing delays in the ISA-like bus timing: first, the delay between the falling edge of the chip select (CompactFlash or ISA) and falling edge of read (nIORD) or write (nIOWR) signal, and second, the delay between the rising edge of the read or write signal and rising edge of the chip select.

The first delay is created by shifting the falling edge of the read (nIORD) or write (nIOWR) signal to create a delay from the chip select. The rising edge of the read and write signals are not delayed by the rising edge of the processor read/write signals. See Section 5 for sample read and write ISA-like timing diagrams.

The ISA device chip select is output by the CPLD when an access to address 0x4840 0000 – 0x485F FFFF is made, and the CompactFlash chip select is output when an access to address range 0x4820 0000 – 0x483F FFFF is made. To create a timing delay between the rising edge of the read or write signal and the rising edge of the chip select, the chip select rising edge is delayed from the processor's area 2 chip select by a single bus clock cycle. See Section 5 for sample read and write ISA-like timing diagrams.

4.5 Buffer Control Logic

This logic controls the direction of buffers if they were to be used externally from the card engine.

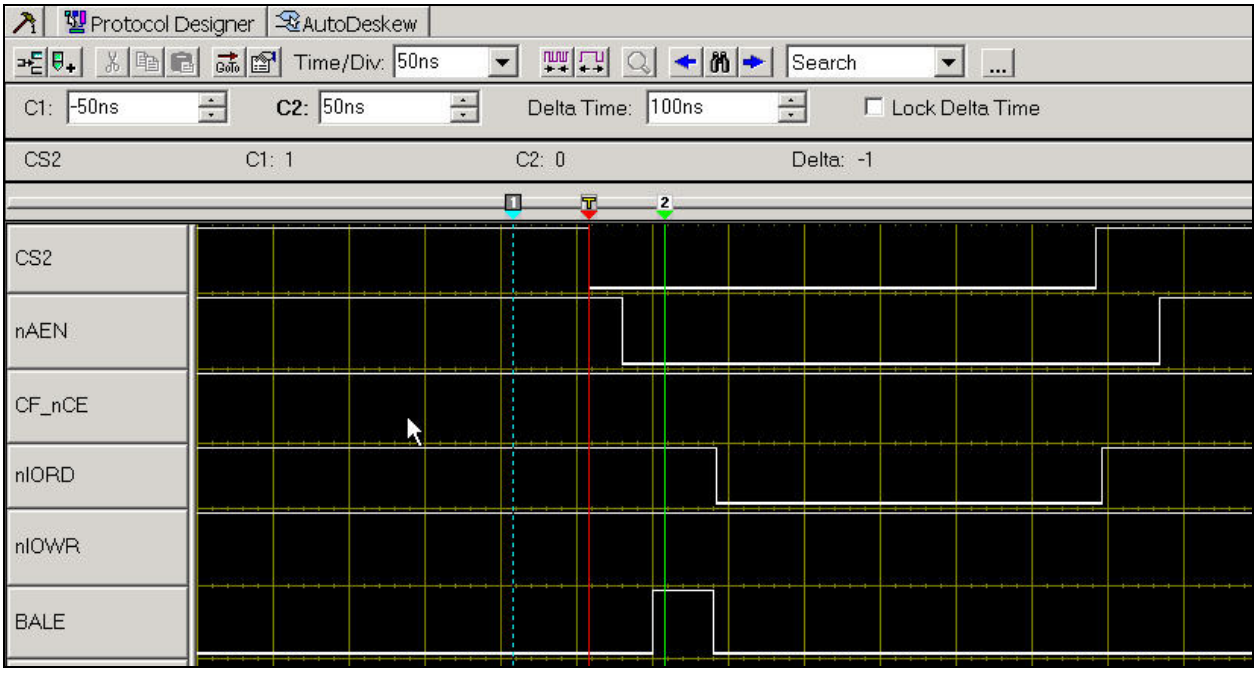
4.6 Interrupt Logic

This logic generates the processor's uP_CPLD_nIRQ, from information in the Interrupt/Mask register, Section 3.1.7, and the Power Management register, Section 3.1.10.

5 ISA Timing Diagrams

5.1 ISA-like Bus, Read Cycle Timing Diagram

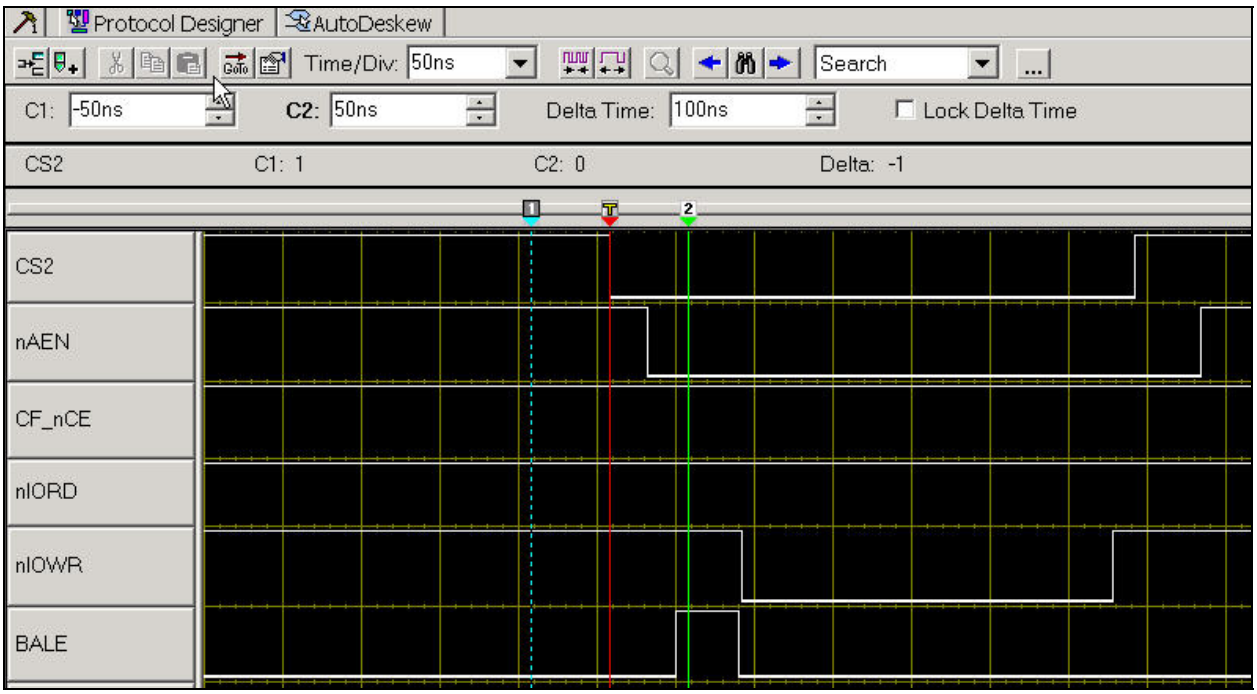
Figure 5.1: ISA-like Bus, Read Cycle Timing



Note: All timing parameters shown in nanoseconds (nS).

5.2 ISA-like Bus, Write Cycle Timing Diagram

Figure 5.2: ISA-like Bus, Write Cycle Timing



Note: All timing parameters shown in nanoseconds (nS).

6 IO Controller Pin Information

Pin	Signal Name	Input/Output
1	NAND_nCE	Output
2	VIDEO_nCS	Output
3	NAND_new	Output
4	NAND_nRE	Output
6	uP_D7	Input/Output
7	uP_D6	Input/Output
8	uP_D5	Input/Output
9	uP_D4	Input/Output
10	uP_D3	Input/Output
11	uP_D2	Input/Output
12	uP_D1	Input/Output
13	uP_D0	Input/Output
14	uP_nCS1	Input
15	BOOT_nCS	Output
16	FLASH_nCS	Output
17	uP_nCS2	Input
18	uP_nCS3	Input
19	uP_MODE3	Input
22	uP_CPLD_CLK	Input
23	uP_nWR	Input
24	MSTR_nRST	Input
27	uP_nRD	Input
28	uP_nCS0	Input
29	uP_MODE2	Input
30	FLASH_STS1	Input
32	CPLD_CS_nCODEC	Output
33	CPLD_CS_MAC	Output
34	CPLD_CS_EEPROM	Output
35	CPLD_SCLK	Output
36	CPLD_TX	Output
37	CPLD_RX	Input
39	FL_VPEN	Output
40	WRLAN_ENABLE	Output
41	uP_STATUS_1	Output
42	uP_STATUS_2	Output
43	CPLD_GPIO_1	Input/Output
44	NC	NC
45	CPLD_TDI	JTAG
46	NC	NC
47	CPLD_TMS	JTAG
48	CPLD_TCK	JTAG
49	CPLD_GPIO_2	Input/Output
50	uP_CPLD_nIRQ	Output
52	WRLAN_nINT	Input

53	CPLD_nIRQC	Input
54	NC	NC
55	CPLD_nIRQD	Input
56	uP_A23	Input
58	uP_A22	Input
59	NC	NC
60	uP_A21	Input
61	uP_A20	Input
63	NC	NC
64	uP_A19	Input
65	NC	NC
66	NC	NC
67	CF_nCE	Output
68	RSVD_1	Input
70	nIOWR	Output
71	nIORD	Output
72	BALE	Output
73	NC	NC
74	nAEN	Output
76	nCHRDY	Input
77	uP_nWAIT	Output
78	nSTANDBY	Input
79	nSUSPEND	Input
80	NC	NC
81	uP_SW_nRESET	Input
82	NC	NC
83	CPLD_TDO	JTAG
85	NC	NC
86	NC	NC
87	NC	NC
89	SLOW_nMCS	Output
90	FAST_nMCS	Output
91	BUFF_DIR_DATA	Output
92	uP_USB1_PWR_EN	Output
93	NC	NC
94	uP_USB1_nOVR_CRNT – VBUS	Input
95	NC	NC
96	NC	NC
97	NAND_RYnBY	Input
99	NC	NC
26, 57	VCC	VCORE
5, 20, 38, 51, 88, 98	VCCIO	3.3V
21,25,31,62,69,75,84,100	GND	GND

