LH79524-10
Card Engine

NOVO

LOGIC

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
1	Ron Ross	Document Created	--	--
A	Nathan Kro, Kurt Larson	Content Additions, Release Revision A	KTL	11/29/04
B	James Wicks	Changed J1C pin 18 from 3.3V to 2.5V	JAW	04/14/05
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Please check www.logicpd.com for the latest revision of this manual, errata's, and additional application notes.

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LH79524 CARD ENGINE

CARD ENGINE ADVANTAGE

- Reduce TIme to Market
  - 6 to 9 month savings typical
- Product-Ready Hardware Platform
- Production Quality Software
  - Bootloader/Monitor
  - Board Support Packages (BSPs)
  - Supports other operating systems
- Engineering Support

ORDERING INFORMATION

Zoom™ Starter Development Kit
- (Model # SDK-LH79524-10-3216)

CUSTOMER SUPPORT

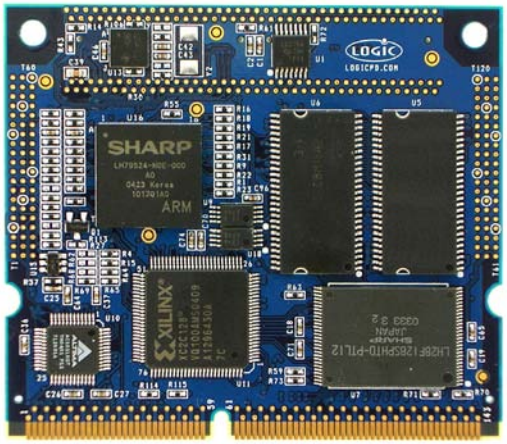
Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

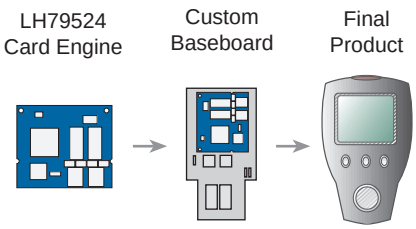
For more information on our Embedded Product Solutions, please contact Logic Sales at: product.sales@logicpd.com or 612.672.9495.

The LH79524 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The LH79524 Card Engine is a complete System on Module (SOM) offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. The use of custom base boards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation microcontroller Card Engines when new functionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Sharp LH79524 32-bit ARM720T RISC processor running up to 77.414 MHz
- **SDRAM Memory** Up to 64 Mbytes
- **Flash Memory** NOR or NAND
  - 0 or 16 Mbytes NOR
  - Scalable NAND (contact Logic for availability)
- **Display** Programmable color LCD controller
  - Built-in driver supports up to 800 x 600 x 16-bit color
  - Supports STN, color STN, HR-TFT, AD-TFT, TFT
- **Touch Screen** Processor integrated
- **Network Support** 10/100 Base-T Ethernet controller (application/debug)
- **Audio** Stereo output audio codec (TI TLV320DAC23)
- **PC Card Expansion** CompactFlash® Type 1 card (memory mode only)
- **Serial Ports** Two 16C550-like, standard UARTs
- **IrDA** SIR supports up to 115.2 Kbps
- **GPIO** Programmable depending on peripheral requirements
- **SSP** Supports either Motorola SPI™, National Semiconductor MICROWIRE™, TI™ SSI
- **USB 2.0 Full Speed** One device
- **Software**
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact size: 2.37"(60.2 mm) long x 2.67"(67.8 mm) wide x 0.17"(4.4 mm) high
  - 144-pin SODIMM connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit (Model # SDK-LH79524-10-3216)

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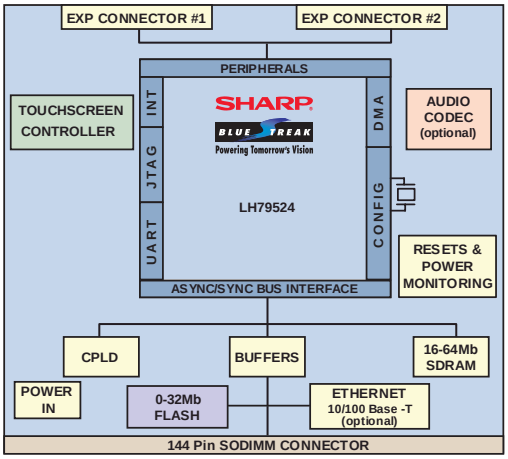
PN: 1000990 Rev D

LH79524 CARD ENGINE

System on Module Block Diagram



Actual size (60.2mm x 67.8 mm)

The Card Engine CPLD provides the following functionality:

- SPI interface to onboard EEPROMS and audio codec
- CompactFlash® card support (memory mode only)
- ISA-like bus interface
- Buffer control logic
- Chip select decoder logic
- Interrupt encoder logic
- Flash program control logic
- Processor mode control logic
- IC code revision register
- Additional GPIO
- Status indicator signals
- On-board power management signals
- Memory mapped NAND flash controller

The CPLD code is available free of charge for customers designing the Card Engine into their final product or for purchase if implementing in a custom board solution.

Please contact Logic Sales at product.sales@logicpd.com for more information.

Standard Configurations for LH79524

Logic Model Number	SDRAM (MB)	NOR Flash (MB)	NAND Flash (MB)	Ethernet	Audio	Touch	Temp. Rating
CENGLH79524-10-403HC(R)	32	16	-	Y	Y	Y	0-70 deg C

(R) An R in the model number denotes a RoHS compliant configuration.
**Please contact Logic for custom configurations and availability.*

System on Module Advantage: Less time, less cost, less risk ... More Innovation

Development Kit w/SOM and optional Dispplay Kit

Development Kit simplifies:
- *Application specific code development*
- *Evaluation of the MCU / System on Module*
- *The transfer of application code, OS and BSPs into production*

Card Engine (with common footprint)

Card Engine complete with:
- *BSPs (Windows® CE, Linux, and other RTOS)*
- *Bootloader provides in-field device management, manufacturing, and test capabilities*

Custom Baseboard (with Card Engine)

Baseboard provides:
- *Power*
- *Connectors*
- *Custom peripherals*
- *Custom form factor*

Final Product

Final Product results:
- *Accelerated time to market*
- *Reduced development cost*
- *Customer focuses on core competencies*

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PN: 1000990 Rev D

1.2 Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I²S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MMC	Multimedia Card
NC	No Connect
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System-on-Chip
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

- LH79524-10 Card Engine IO Controller Specification
- LogicLoader™ User's Manual
- LH79524 Universal Microcontroller User's Guide
- Xilinx XC2C64 CPLD data sheet
- Texas Instruments TLV320AIC23 Audio CODEC data sheet

1.4 Card Engine Advantages

Logic's Card Engines accelerate your product's time-to-market, and provide the following advantages:

- Product Ready Hardware and Software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – Allows you to focus on other aspects of your design
- Common Card Engine Footprint (See Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations are available to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

1.5 Card Engine Interface

Logic's common Card Engine interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common Card Engine footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

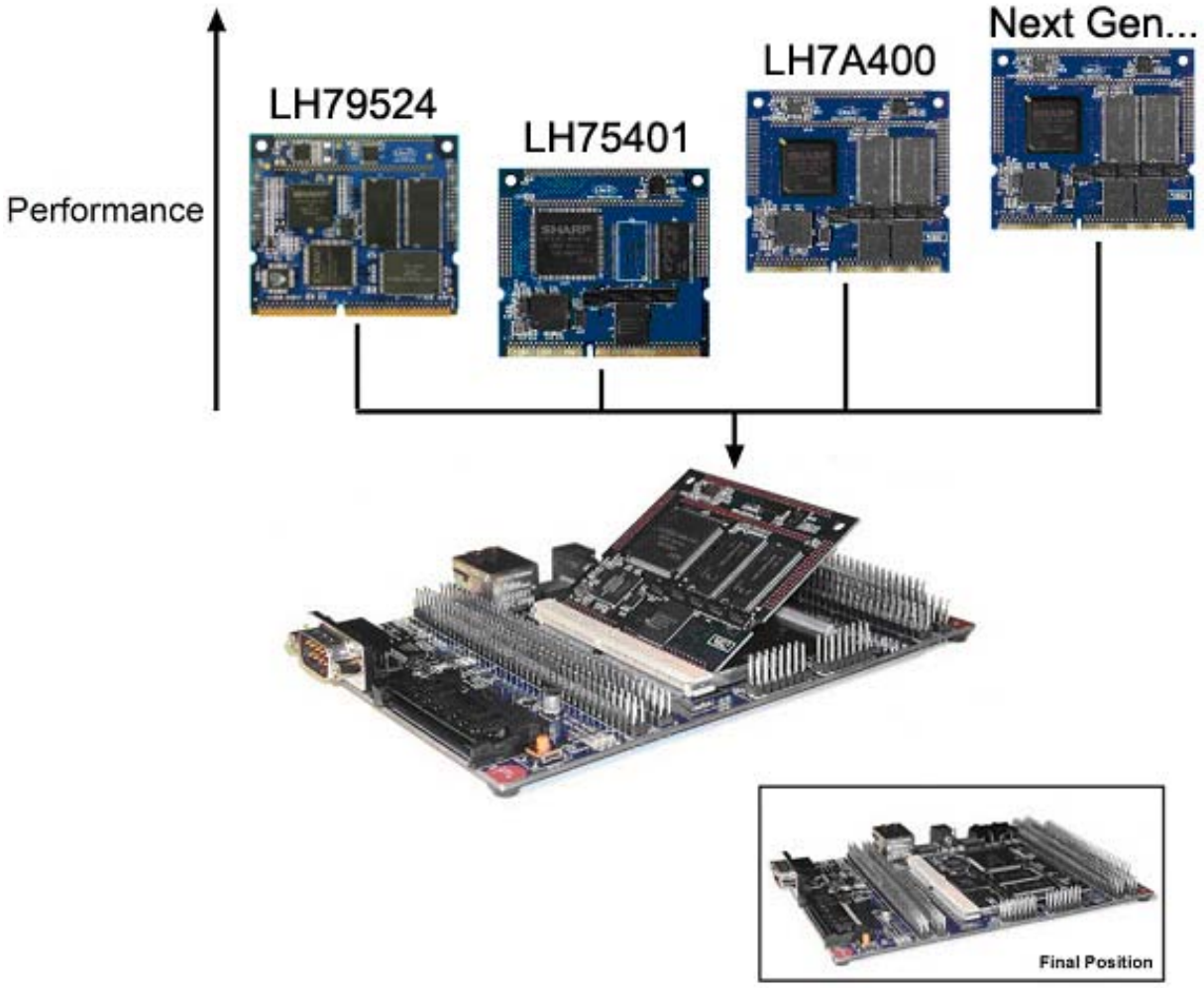

Figure 1.1: Card Engine Advantages

In fact, encapsulating a significant amount of your design onto the Card Engine reduces any long-term risk of obsolescence. If a component on the Card Engine design becomes obsolete, Logic will simply design for alternative part that is transparent to your product. Furthermore, Logic tests all Card Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

1.6 LH79524-10 Card Engine Block Diagram

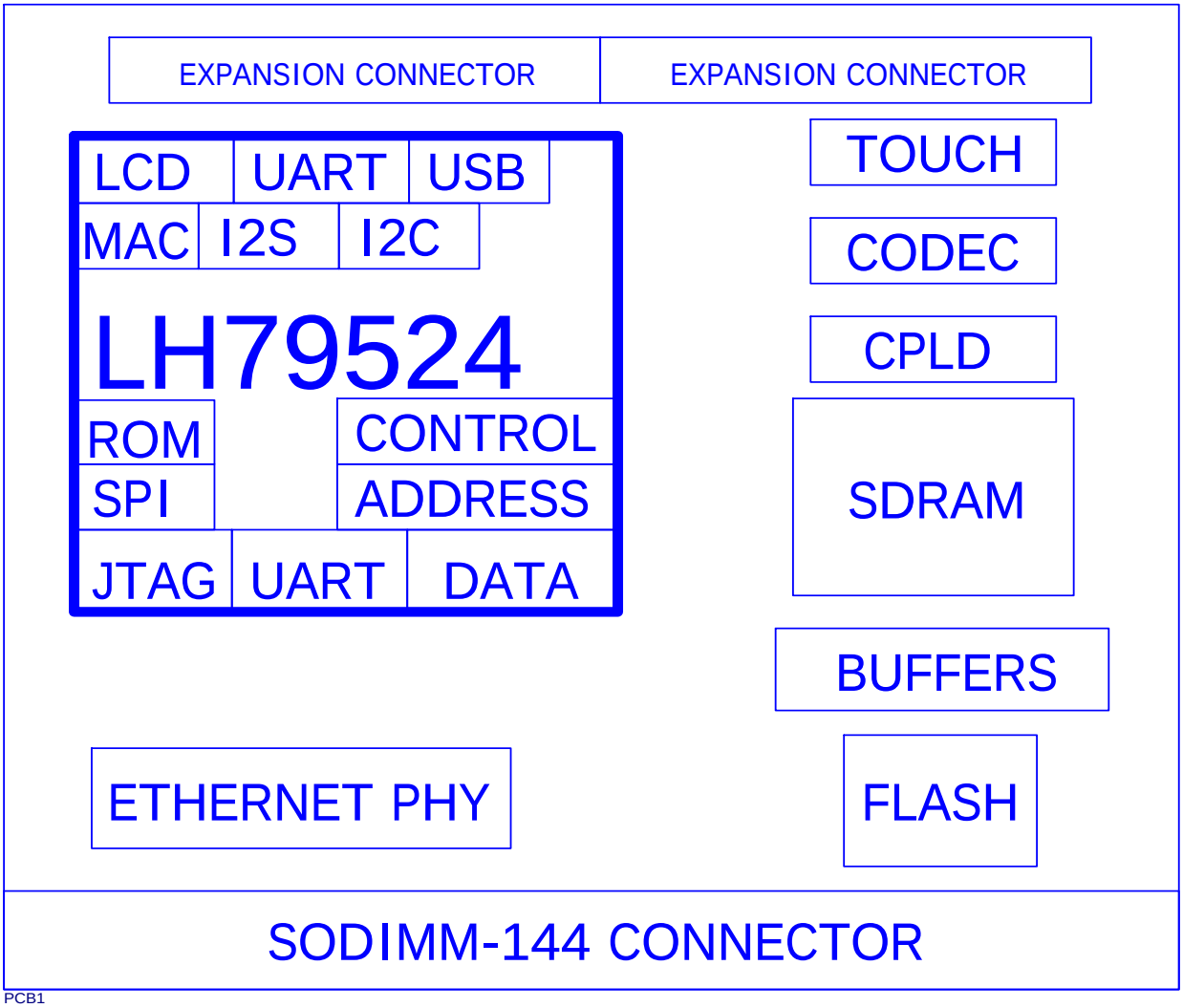

Figure 1.2: LH79524-10 Card Engine Block Diagram

1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	unit
DC IO and Peripheral Supply Voltage	3.3V	-0.3 to 3.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.4	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.7.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	Note 4	234	275	mA	4
DC IO Supply Standby Current	Note 4	TBD	TBD	mA	4
DC IO Supply Sleep Current	Note 4	TBD	TBD	mA	4
DC Core Supply Voltage	1.62	1.8	1.98	V	1
DC Core Supply Active Current	Note 4	68	160	mA	4
DC Core Supply Standby Current	Note 4	TBD	TBD	mA	4
DC Core Supply Sleep Current	Note 4	0	TBD	mA	4
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.6		VIO	V	
Output Signal Low Voltage	GND		0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. Not applicable
3. Contact Logic for more information on an industrial temperature LH79524-10 Card Engine.
4. May vary depending on Card Engine configuration.

2 Electrical Specification

2.1 Microcontroller

2.1.1 LH79524 Microcontroller

The LH79524-10 Card Engine uses Sharp's highly integrated system on a chip LH79524 microcontroller. It contains a 32-bit ARM720T RISC core and provides many integrated on-chip features including:

Integrated ARM720T™ Core
- 32 bit ARM720T™ RISC Core
- High Performance (77.414 MHz CPU Speed)
- 32-bit External Data Bus
- 8KB Cache with Write Back Buffer
- MMU (Windows CE™ Enabled)

16 KB on-chip SRAM

Flexible, Programmable Memory Interface
- SDRAM Interface
  - 24-bit External Address Bus
  - 32-bit External Data Bus
- SRAM/Flash/ROM Interface
  - 24-bit External Address Bus
  - 32-bit External Data Bus
- On-Chip Boot ROM Controller
  - Allows Booting from 8-, 16-, or 32-Bit Devices
  - Glueless Support for NAND Flash

Multi-stream DMA Controller
- Four 32-bit Burst-Based Data Streams

Integrated LCD Controller
- Up to 800 x 600 Resolution at 16-bit color
  - (1024 x 768 at 8 bits color)
- STN, Color STN, HR-TFT, AD-TFT, TFT
- Up to 65,536 Colors

Low Power Modes
- Active Mode: 85 mA (TYP.)
- Standby Mode: 50 mA (TYP.)
- Sleep Mode: 3.8 mA (TYP.)
- Stop Mode 1: 420 µA (TYP.)
- Stop Mode 2: 25 µA (TYP.)

USB Device
- Compliant with USB 2.0 Specifications (Full Speed)
- Four Endpoints

Ethernet MAC, MII Interface
- IEEE 802.3 Compliant
- 10 and 100 Mbit/s Operation

Analog-to-Digital Converter/Brownout Detector
- 10-bit ADC
- Pen Sense Interrupt
- Integrated Touch Screen Controller (TSC)

Vectored Interrupt Controller
- 16 Standard and 16 Vectored IRQ Interrupts
- Interrupts Individually Configurable as IRQ or FIQ

- I^2C Module
- Integrated Codec Support Features
- Watchdog Timer
- Three UART's
  - 16-entry FIFOs for Rx and Tx
  - IrDA SIR Support on all UARTs
- Three 16-bit Timers with PWM capability
- Real Time Clock
  - 32-bit Up-counter with Programmable Load
  - Programmable 32-bit Match Compare Register
- Synchronous Serial Port
  - Supports Data Rates Up to 1.8452 Mbit/s
  - Compatible with Common Interface Schemes
- Programmable General Purpose I/O Signals
  - 108 available pins on 14 ports
- JTAG Debug Interface and Boundary Scan
- 5 V Tolerant I/O
  - On-Chip regulator allows single 3.3 V supply

See Sharp's LH79524 Universal Microcontroller User's Guide for additional information.
http://www.sharpsma.com/

IMPORTANT NOTE: Please see http://www.sharpsma.com/ for any errata on the LH79524.

2.1.2 LH79524 Microcontroller Block Diagram

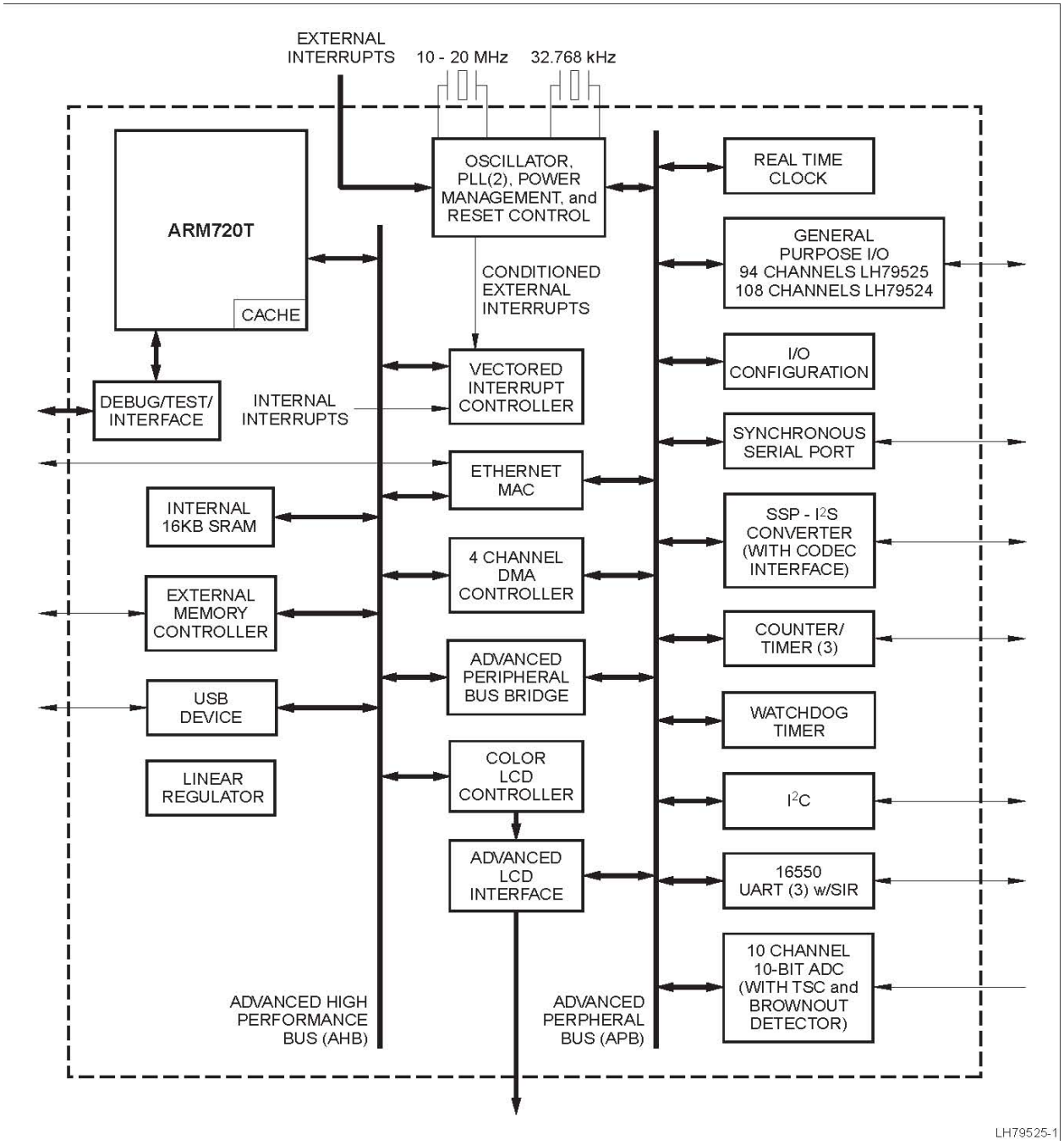

Figure 2.1: LH79524 Microcontroller Block Diagram

2.2 Clocks

The LH79524 requires 2 crystals in order to have proper internal timing. The first is a 11.2896 MHz crystal, which is used to generate many of the processors internal clocks through a series of dividers. The crystal signal is run through a PLL to generate the FCLK signal. FCLK is then used internally as the Synchronous Bus Mode core clocking for the ARM720T core and cache. The 11.2896 MHz crystal is also used to create the HCLK, HCLK_CPU, PCLK, and peripheral clock signals. One such peripheral clock is set up through a second PLL to produce a 48.0 MHz clock for USB operations. One more signal stemming from the 11.2896MHz crystal input is the uP_AUX_CLK signal, which is produced through a programmable divider on the card engine. The uP_AUX_CLK is provided on the 144-pin SO-DIMM expansion connector as the LH79524 CLKOUT, and is set to a default of 11.2896MHz.

The second required crystal runs at 32.768 kHz and is the only permanently running clock in the LH79524, using a ripple divider to conserve power. This divider produces the 1 Hz signal for the RTC interface as well as intermediate frequencies of 16kHz and 8kHz for the state controller and PLL interlocks.

The LH79524 is able to operate in either asynchronous, synchronous, or FastBus extension clocking modes. Choosing between these three modes depends on the desired application as each has certain advantages or disadvantages in system throughput and power consumption.

IMPORTANT NOTE: Please see Sharp's LH79524 Universal Microcontroller User's Guide for additional information about the Standard Bus Clocking Modes and the relation between FCLK and HCLK.

The LH79524's microcontroller core clock speed is initialized to 77.4 MHz on the Card Engine and the Bus speed is set at 51.6 MHz in the LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH79524-10 Card Engine provides an external Bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector. The uP_BUS_CLK, which is connected to the processor's SCLK, is set to a default of 100 MHz. SDCLK also serves as the SDRAM and CPLD clock on the LH79524-10 Card Engine.

LH79524 Microcontroller Signal Name	LH79524-10 Card Engine Net Name	Default Software Value in LogicLoader™
FCLK	N/A	77.4 MHz
HCLK	N/A	51.6 MHz
SDCLK	uP_BUS_CLK	51.6 MHz
CLKOUT	uP_AUX_CLK	11.2896 MHz

2.3 Memory

2.3.1 Synchronous DRAM

The LH79524-10 Card Engine uses a 32-bit memory bus to interface to SDRAM. The memory can be configured as 16, 32 or 64MBytes to meet the user's memory requirements and cost constraints. Logic's default memory configuration on both the IDK and SDK boards is specified as 64MBytes.

2.3.2 Direct Memory Access (DMA)

The Sharp LH79524 processor has one external DMA channel muxed with UART0 CTS and RTS signals. If CTS and RTS functionality on UART0 are not required, the external DMA channel is available to the user. If an external DMA channel is required, please contact Logic Product Development for assistance gaining support for the device.

2.3.3 NOR Flash

The LH79524-10 Card Engine uses a 16-bit memory bus to interface to Sharp MLC NOR memory chips. The onboard Card Engine memory can be configured as 8 or 16MBytes to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 16MB on the SDK. Because flash is one of the most expensive components on the LH79524-10 Card Engine, it is important to contact Logic when determining the necessary flash size.

It is possible to expand the system's non-volatile storage capability by adding external flash IC's, CompactFlash, or NAND flash. See the LH79524-10 Application Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND Flash

The LH79524 processor supports direct connection to NAND flash chips. The user's system design can take multiple forms, including: NOR flash alone, NOR boot flash + NAND for data storage, or NAND flash alone. The LH79524 has an internal boot ROM that allows the LH79524-10 card engine to boot directly from a discrete NAND device. Logic Product Development standard product supports 64Mbytes of NAND flash on the Card Engine. However, the NAND device footprint is scalable from 32Mbytes, 64MB, 128MB, and higher depending on discrete NAND flash availability. Please contact Logic Product Development for assistance with higher density NAND devices.

2.3.5 CompactFlash (memory-mapped mode only)

The LH79524-10 Card Engine supports a CompactFlash memory mapped mode only slot that compliments the processor's memory support. The LH79524_10 Card Engine uses the CPLD to provide the necessary signals for a CompactFlash card interface in memory mapped mode only. The Zoom™ Starter Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. If hot swapping capability is desired, it can be achieved by using additional hardware on the user's base board. See the *LH79524-10 IO Controller Spec* document for further details on the use of the memory-mapped CompactFlash interface.

IMPORTANT NOTE: The CPLD CompactFlash interface supports memory-mapped mode only. If additional PC card slot functionality is required, please contact Logic Product Development for further information on services available to design PC card interfaces or alternate products that directly support PC cards.

2.4 10/100 Ethernet Controller

The LH79524-10 Card Engine couples a Broadcom AC101L Ethernet PHY to the LH79524 MAC MII interface. To facilitate use, six signals from the AC101L are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LED's. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides example circuit schematics in the LH79524-10 SDK Application Kit for reference.

2.5 Audio CODEC

The LH79524 processor has an internal SSP to I2S converter that is connected to the onboard Texas Instruments TLV320AIC23 audio CODEC. From the CODEC there are 4 outputs,

CODEC_OUTL, CODEC_OUTR, and HP_OUTL, HP_OUTR (Headphone). All of these signals are available from the 80-pin expansion connectors.

The audio CODEC uses a 11.2896MHz reference clock output from the processor. The audio CODEC is software programmable via a bit banged SPI interface through the CPLD. See the *LH79524-10 IO Controller Spec* for programming information. The audio CODEC provides software programmable sample rates, volume control, mute, and power management. See the TI Audio CODEC specification for programmable register settings.

If you are looking for a different CODEC option, Logic has previously interfaced different high performance audio CODEC's into other Card Engines. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

2.6 Video Interface

Sharp's LH79524 microcontroller has a built in LCD controller supporting STN, TFT, and HR-TFT panels at up to 800 x 600 x 16-bit or 1024 x 768 x 8-bit color resolution. See the LH79524 Universal Microcontroller User's Guide for further information on the integrated LCD controller. The signals from the LH79524's LCD controller are organized by bit and color and can all be interfaced through the J1A expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Logic Product Development has many LCD panel kits that directly connect the SDK platform. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.7 Serial Interface

The LH79524-10 Card Engine comes with the following serial channels: UARTA, UARTB/SIR, and UARTC/I2S/SSP. If additional serial channels are required, please contact Logic for reference designs. UARTB supports both wired serial and infrared communications. UARTC is muxed with the I2S and SSP on chip peripherals and only one can be used at a time. The card engine default selects I2S for communication with the onboard CODEC.

2.7.1 UARTA

UARTA has been configured to be the LH79524-10 development kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the SDK and IDK kits. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2K bits/sec, though it supports all common serial baud rates from 2.4kbps to 920.6kbps. UARTA is available off the 144-pin SO-DIMM connector. Please see the LH79524 Universal Microcontroller User's Guide for further information.

2.7.2 UARTB

Serial Port UARTB has dual functionality, its primary function is as an asynchronous 16C550 compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTB's baud rate can also be set to all common serial baud rates from 2.4kbps to 920.6kbps.

The UARTB pins are multiplexed with GPIO Ports A0, A1 and when UARTB is not in use, the GPIO pins can be used instead. UARTB is available off the J1B 80-pin expansion connector.

2.7.3 UARTC

Like UARTA and UARTB, UARTC supports serial communications. Unlike the previous UART's, however, UARTC also supports I2S and SSP.

The card engine default software selects I2S for communication with the onboard CODEC when the audio driver is loaded.

Please see Sharp's LH79524 Universal Microcontroller User's Guide for more information on using this part.

2.8 USB Interface

The LH79524 card engine is configured with one available USB device interface and is fully compliant with the USB 1.1, OpenHCI, and Intel UHCI specifications. This USB client supports full-speed (12M bits/sec) operation and both suspend and resume signaling. The USB device interface on the LH79524 is able to transmit, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector. Please see the LH79524 Universal Microcontroller User's Guide for further information on how to properly use these features.

IMPORTANT NOTE: In order for USB to be correctly implemented on the LH79524 card engine, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 1.1 requirements specify that the impedance on each driver must be between 28Ω and 44Ω. For reference, see the impedance matching circuit on the Logic SDK or IDK application boards.

2.9 Touch Interface

The LH79524 SoC has an internal 4 and 5 wire touch interface circuitry. The Card Engine interface implements a 4-wire touch circuit to all Logic Product Development LCD kits which use standard 4 wire touch screen panels.

2.10 General Purpose Analog & Digital I/O

Logic designed the LH79524-10 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Card Engine that interface to the LH79524, and the Xilinx CPLD. Some of these GPIO pins are interrupt capable while other signals are input or output only. Please see the Pin Descriptions section of this data sheet. The LH79524 microcontroller contains an internal Analog to Digital Converter (ADC); which provides a total of 8 analog inputs available off of the J1A expansion connector. The touch interface is multiplexed with 4 of these signals. If certain peripherals are not desired, such as the LCD Controller, Chip Selects, IRQs, UARTS, I2S, CompactFlash, Smart Card Interface, or BMI interface, then multiple GPIO pins become available. Please see the table in Section 0 for a list of the available GPIO trade-offs.

2.11 CPLD

Please see the LH79524-10_IO_Controller_Spec document for CPLD information.

2.12 Serial EEPROM Interface

Logic designed the LH79524-10 Card Engine to have a low-cost 1 kb serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the LH79524 microcontroller via the

CPLD through a SPI interface. See Figure 2.2 below. For more information please view the *LH79524-10 IO Controller Specification*.

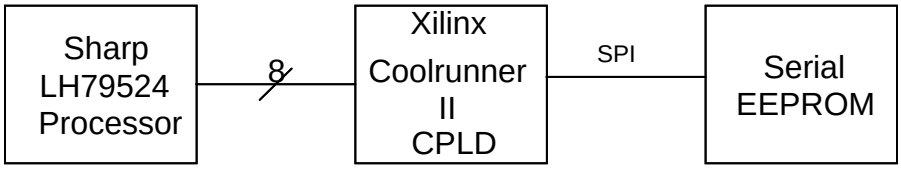

Figure 2.2: Serial EEPROM Block Diagram

2.13 Expansion Options

The LH79524-10 Card Engine was designed for expansion, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. See the LH79524-10 Card Engine schematics for more detail. A user may expand the card engine's functionality by adding PCI or ISA devices. Logic has used other audio CODEC's, Ethernet IC's, co-processors, and components on the card engine boards in the past. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The LH79524-10 Card Engine was designed to meet multiple applications for specific users and budget requirements. As a result, this card engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Flexible RAM footprint: 16, 32, or 64MBytes SDRAM
- Flexible flash footprint: 8, 16, or 32MBytes NOR flash, 32, 64, 128+ MBytes NAND flash
- Optional Texas Instruments TLV320AIC23 Audio CODEC
- Optional Broadcom AC101L PHY

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all card engine peripheral hardware reset pins are connected to either the MSTR_nRST net. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the LH79524-10 Card Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems.

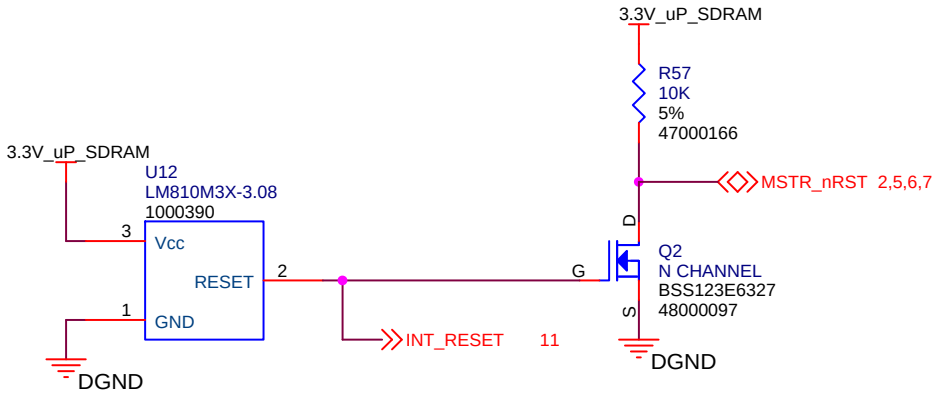

Figure 3.1: Reset Circuit

If the output of the reset chip, INT_RESET, is asserted (active high), Q2 drives net MSTR_nRST low (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details.

There are three conditions that will cause a system-wide reset: power-on, a low pulse on the MSTR_nRST signal, and U12 asserting RESET when the 3.3V_uP_SDRAM net falls out of regulation.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (Vcc) of the reset chip is between 0.4V and 3.08V. Once the 3.3V_uP_SDRAM supply surpasses 3.08V the reset chip will trigger a rising edge of MSTR_nRST after a 140-560ms delay (240ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that any external assertion source that triggers the MSTR_nRST signal, analog, or digital de-bouncing be used to generate a clean one shot reset signal.

3.2.2 Soft Reset

Logic has created a soft reset signal, SW_nRESET, to be used as defined by the user. The SW_nRESET signal triggers an interrupt through the CPLD. The interrupt is not maskable in the CPLD. Typical implementations will use this to reset the LH79524's internal registers without affecting the peripherals on the rest of the board or the data stored in SDRAM.

See Sharp's LH79524 Universal Microcontroller User's Guide for additional information on register conditions after reset.

3.3 Interrupts

The LH79524 Interrupt Controller collects interrupt request signals from on-chip and off-chip sources and processes the interrupt requests into an IRQ signal and an FIQ signal to the ARM720T core. The LH79524 processor accepts inputs from 32 interrupt sources, and on the LH79524 Card Engine, 4 sources are available to configure externally: INT7 is used onboard for the CPLD interrupt interface. By default, the LH79524-10 Card Engine interrupts are set to trigger on a LOW level and are pulled up to 3.3V by 10k resistors. Refer to Sharp's LH79524 Universal Microcontroller User's Guide for further information on using IRQ and FIQ interrupts.

3.4 JTAG Debugger Interface

The JTAG connection on the LH79524 allows recovery of corrupted flash memory and real time applications debug. When choosing a debugger board, remember that many different third-party JTAG debuggers are available for Sharp ARM microcontrollers. The following signals make up the JTAG interface to the LH79524: uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 20-pin 0.1" through-hole connector as demonstrated in the Sharp LH79524 Universal Microcontroller User's Guide, or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20-pin connector out, realize that it may not be numbered as a standard 20-pin 0.1" IDC through-hole connector. See LH79524-10 Card Engine Application Kit reference design for further details. Different IC manufacturers define the 20-pin IDC connector pin-out differently.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the LH79524-10 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, and VCORE. All power areas are inputs to the card engine with the exception of 2.5V pin, which is an output from the card engine.

3.5.1.1 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins are connected to a 3.3V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in this section below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the LH79524-10 Card Engine. This supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the LH79524 processor on the LH79524-10 Card Engine. The 3.3VA supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 2.5V

This “power” supply pin is an output from the card engine that must be implemented for proper Ethernet operation across multiple card engine platforms.

The custom application board should use the 2.5V output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 2.5V directly or the entire Ethernet controller circuit on the card engine will try to power itself through the impedance matching resistors. Please see Logic’s schematics for the SDK or IDK reference designs for details.

3.5.1.5 VCORE

The VCORE input pins are connected to a 1.8V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. Please see the description of Standby mode later in this section.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The LH79524-10 Card Engine was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the LH79524 there are many different software configurations that drastically effect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes (asynchronous, synchronous, FastBus), microcontroller power management states (run, halt, standby), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the LogicLoader™ User's Manual or appropriate BSP manual.

IMPORTANT NOTE: Most of the LH79524-10 Card Engine hardware architecture was designed for low power battery operated applications. The Altera CPLD, on the LH79524-10 Rev A and earlier Card Engine designs, was chosen to optimize cost over power savings. If power-optimization is the primary goal of the design, please ensure that the design is utilizing LH79524-10 Rev B or later card engines which incorporate a Xilinx Coolrunner CPLD.

3.5.3 Peripherals

The LH79524-10 Card Engine was designed to have the following four power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, and VCORE for a flexible hardware design. See Figure 3.3 below.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_ SDRAM	3.3VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to refresh.
3.3V	3.3VDC	Connects to the digital peripherals on the Card Engine.
3.3VA	3.3VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
VCORE	1.8V	Connects to the processor core voltage. See information on each specific processor for the VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperatures, etc.

Figure 3.2: Power Plane Diagram

3.5.4 Microcontroller

The LH79524 processor power management's scheme was designed to be easy to use. There are three power management states suggested for the LH79524 Card Engine: RUN, STANDBY, and HALT. Please see below for descriptions from all three states and the LH79524 Universal Microcontroller User's Guide for more details.

3.5.4.1 Run Mode

Run is the LH79524 Card Engine's normal operating state in which both oscillator inputs and all clocks are hardware enabled. The LH79524 can enter Run mode from either the Standby or Halt states. From the Standby state, Run can be accessed on the assertion of an interrupt (interrupts are active low). A Halt to Run transition occurs on the falling-edge of an interrupt (interrupts are active low), Power Fail, or on a user reset (Soft Reset).

3.5.4.2 Standby Mode

Standby is the LH79524-10 Card Engine's hardware power down mode, allowing for minimal power consumption. In this mode the processor is set to STOP2 state and all clocks are off except the RTC clock. Before the clocks are turned off, however, the SDRAM is put into self-refresh mode, and maintains the contents of memory while in the low power state. Standby mode can only be entered after a system power-on or on a progression from the Run state. A Run to Standby transition occurs on a Power Fail, User Reset (Soft Reset), or an interrupt.

3.5.4.3 Halt Mode

The Halt state is designed to reduce power consumption while the LH79524 is waiting for an event such as a keyboard input. In this mode, although the processor clock is halted, the input oscillator is enabled, thereby allowing software to specify the other active and inactive clocks. In this way, it is possible to maintain the LCD image yet reduce system-wide power usage at the same time. The only way to transition to the Halt state is by writing to the PWRDWNSEL register while in the Run state.

IMPORTANT NOTE: Although Halt consumes less power than Run mode, it consumes more power than the Standby Mode. Thus, on a power failure, the LH79524 system will actually leave the Halt state and transition to the Standby state (the same thing occurs on a SW_nRESET).

3.6 ESD Considerations

The LH79524-10 Card Engine was designed to interface to a customer's peripheral board. The Card Engine was designed to be low cost and adaptable to many different applications. The LH79524-10 Card Engine does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SDRAM Memory Map

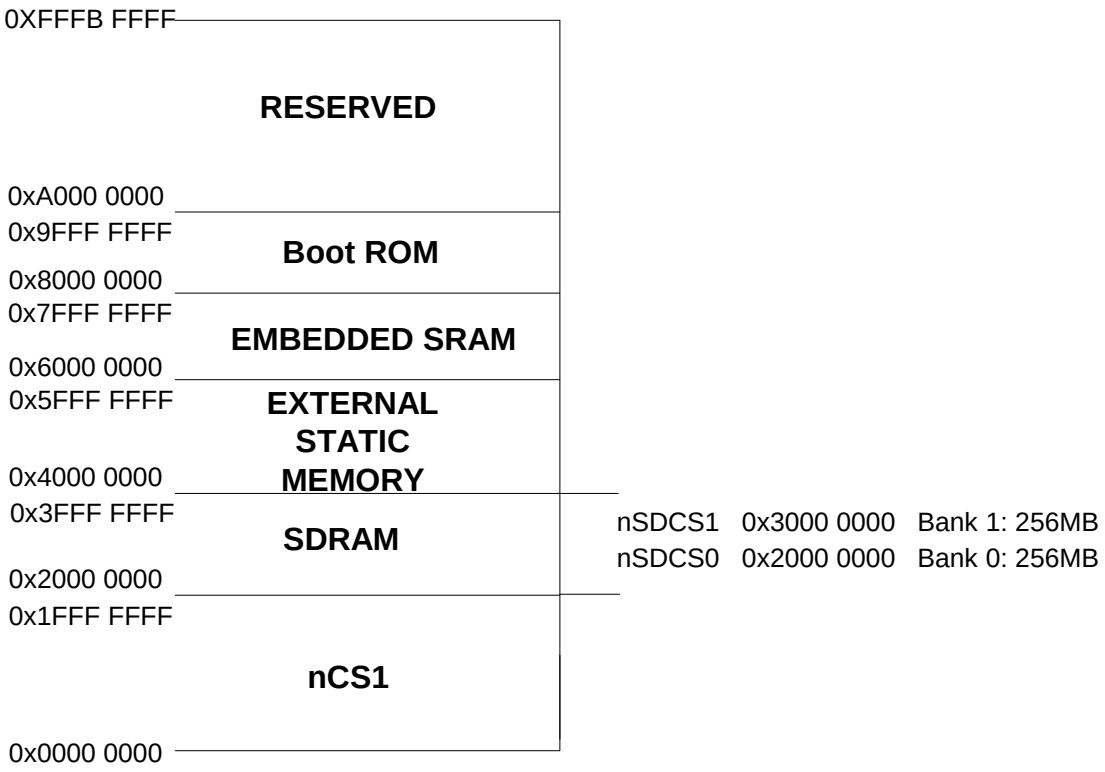

Figure 4.1: LH79524 SDRAM Memory Map Diagram

4.2 External Static Memory Map

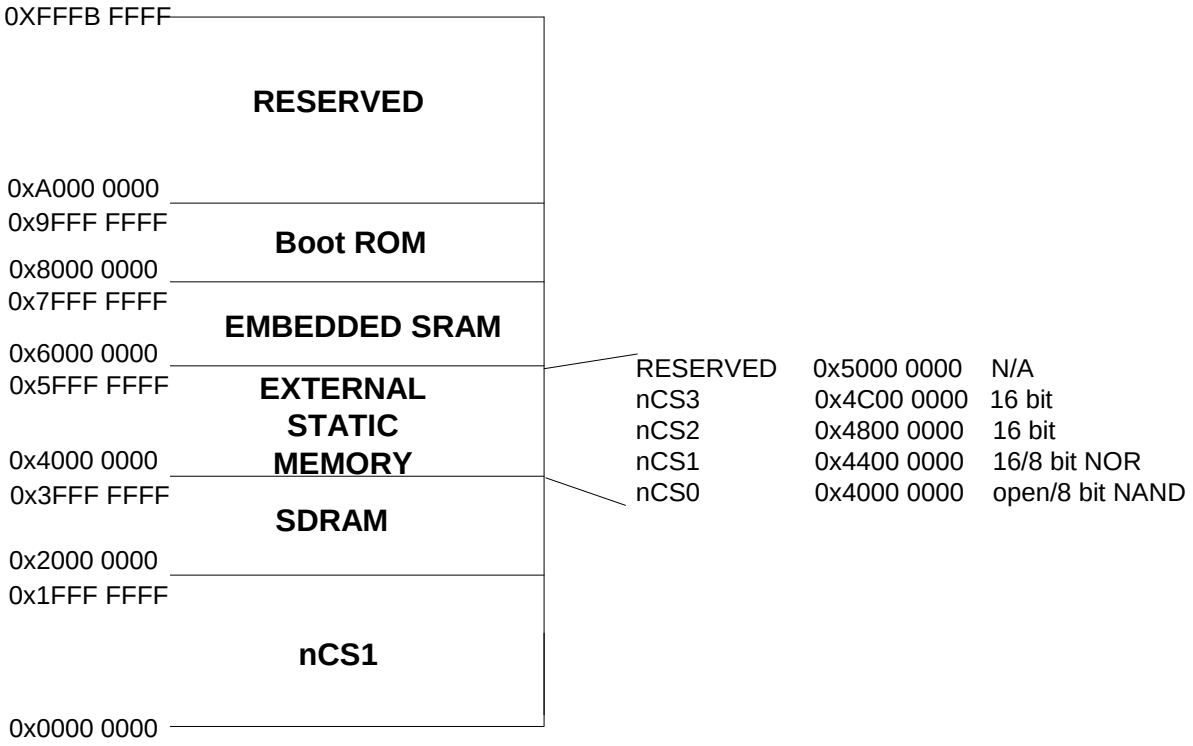

Figure 4.2: LH79524 External Static Memory Map Diagram

NOTE: The bit numbers refer to the bank width at reset. Banks 1 and 3 (nCS0 and nCS2) are 32-bits wide if flash is used as the boot device and 8-bits wide if an EEPROM is used as the boot device.

4.2.1 Card Engine Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the card engine.

Chip Select	Bank	Start Address	Memory Description
RESERVED	4	0x5000 0000	RESERVED
nCS3	3	0x4C00 0000	IO Controller Peripherals (fast[1])
nCS2	2	0x4800 0000	IO Controller Peripherals (slow[1])
nCS1	1	0x4400 0000	Boot Device (flash or Off-Board)
nCS0	0	0x4000 0000	Boot Device (flash or Off-Board)

Notes:
1. IO Controller Peripherals are components that get a decoded chip select from the CPLD. (i.e. CPLD memory mapped registers, etc... Please see the LH79524-10 IO Controller Specification document for details.) These peripherals are separated into two different chip select banks, due to difference in timing: slow and fast.

4.2.2 Chip Select 2 (CS2) – CPLD Peripherals (slow timing)

The table below indicates how the CPLD decodes chip select 2. For more detailed information see the LH79524-10 IO Controller Specification.

Address Range	Memory Block Description	Size
0x4800 0000 – 0x481F FFFF	Reserved	2MB
0x4820 0000 – 0x483F FFFF	CF Chip Select	2MB
0x4840 0000 – 0x485F FFFF	ISA-like Bus Chip Select	2MB
0x4860 0000 – 0x48AF FFFF	Reserved - On-Board Expansion	(1MB)x5
0x48B0 0000 – 0x48FF FFFF	Reserved - Off-Board Expansion	(1MB)x5
0x4900 0000 – 0x49FF FFFF	Open – Available for User	16MB

4.2.3 Chip Select 3 (CS3) – CPLD Peripherals (fast timing)

The table below indicates how the CPLD decodes chip select 3. For more detailed information see the LH79524-10 IO Controller Specification.

Address Range	Memory Block Description	Size
0x4C00 0000 – 0x4C0F FFFF	Reserved	1MB
0x4C10 0000 – 0x4C1F FFFF	Card Engine Control Reg	1MB
0x4C20 0000 – 0x4C2F FFFF	Reserved	1MB
0x4C30 0000 – 0x4C3F FFFF	Reserved	1MB
0x4C40 0000 – 0x4C4F FFFF	Reserved	1MB
0x4C50 0000 – 0x4C5F FFFF	EEPROM/SPI Reg	1MB
0x4C60 0000 – 0x4C6F FFFF	Interrupt & Mask Reg	1MB
0x4C70 0000 – 0x4C7F FFFF	Mode Reg	1MB
0x4C80 0000 – 0x4C8F FFFF	Flash Reg	1MB
0x4C90 0000 – 0x4C9F FFFF	Power Reg	1MB
0x4CA0 0000 – 0x4CAF FFFF	IO Controller Code Revision Reg	1MB
0x4CB0 0000 – 0x4CBF FFFF	Extended GPIO Reg	1MB
0x4CC0 0000 – 0x4CCF FFFF	GPIO Data Reg	1MB
0x4CD0 0000 – 0x4CDF FFFF	GPIO Direction Reg	1MB
0x4CE0 0000 – 0x4CEF FFFF	Reserved - On-Board Expansion	1MB
0x4CF0 0000 – 0x4CFF FFFF	Reserved - Off-Board Expansion	1MB
0x4D00 0000 – 0x4FFF FFFF	Open – Available for User	16MB

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the card engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T PHY receive lines. Route as differential pair with ETHER_RX(+). This signal requires external impedance matching circuitry. Refer to SDK application board for design reference.
2	MSTR_nRST	I/O	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of external memory. Refer to the reset description found in section 3.2.1 for more information on how this signal is driven. Every peripheral on the card engine with a reset line is reset with the assertion of this signal. Refer to LH79524 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T PHY receive lines. Route as differential pair with ETHER_RX(-). This signal requires external impedance matching circuitry. Refer to SDK application board for design reference.
4	uP_SW_nRESET	I	Active Low. This signal initiates a user defined state based on an ISR. This pin is connected to the CPLD, please see LH79524-10 IO Controller Specification for detailed information on the use of the CPLD. The uP_SW_nRESET must be implemented in software in order to function properly. This signal is pulled up to 3.3V through a 10K resistor.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+). This signal requires external impedance matching circuitry. Refer to SDK application board for design reference.
6	FAST_nMCS	O	Active Low. Chip select for area nCS3 of LH79524-10 memory -- the "fast" peripheral chip select area. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts FAST_nMCS. User can implement external devices using FAST_nMCS as a memory mapped chip select area. See IO controller specification for detailed information on FAST_nMCS.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-). This signal requires external impedance matching circuitry. Refer to SDK application board for design reference.

Pin #	Signal Name	I/O	Description
8	SLOW_nMCS	O	Active Low. Chip select for area nCS2 of LH79524-10 memory -- the “slow” peripheral chip select area. See memory map for details. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts SLOW_nMCS. User can implement external devices using SLOW _nMCS as a memory mapped chip select area. See IO controller specification for detailed information on SLOW_nMCS.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nCS	O	This signal is tied to the CPLD, it is disabled internally.
11	ETHER_nACT_LED	O	Active Low. This output is ON when a link is present, and BLINKS during transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nCS	O	Active Low. This signal is the chip select for boot ROM in area 0 when uP_MODE3 is low. When uP_MODE3 is high, this signal is only accessible through the CPLD. This signal is intended for external boot devices. Reference the IO controller specification for details on use of this signal.
13	ETHER_nLNK_LED	O	Active Low. This output drives low when a 100Mbps link is active, drives high when a 10MBps link is active. May be connected directly to an external LED.
14	nIOWR	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in. See the LH79524-10 IO Controller Specification for further details.
15	nSTANDBY	I	Active Low. CPU power mode signal. If supported by installed software, a low nSTANDBY signal is meant to cause the Card Engine to enter standby mode (hardware power down), where the contents of the SDRAM are placed in self-refresh and will be maintained. From standby, run is entered in response to an exit from CLKSET or in response to an interrupt or fast interrupt falling edge (IRQ/FIQ – assuming interrupts are enabled). Software must be implemented in order for this signal to operate properly. This signal is pulled up to 3.3V through a 10K resistor.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the LH79524-10 IO Controller Specification for further details.
17	DGND	I	Digital Ground (0V)
18	2.5V	O	Power Supply (2.5V). To maintain scalability between multiple Logic Product Development Card Engines, This signal should be used to power the impedance matching resistor network on the Ethernet’s TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid or the processor data bus is in use. See the LH79524-10 IO Controller Specification for further details.
21		NC	No internal connection (not implemented on the LH79524-10)
22	nCHRDY	I	Active Low. The I/O channel ready signal line serves to drive the asynchronous ready signal on the Compact Flash circuit low when additional cycle time is required. Push/Pull or open drain assertion of this signal are acceptable. This signal is pulled up to 3.3V through a 1K resistor.
23	CPLD_nIRQD	I	Active Low. Dedicated hardware interrupt on LH79524-10. This interrupt is readable and maskable in the CPLD. See the IO controller specification for detailed information on accessing CPLD interrupts. This signal is pulled up to 3.3V through a 10K resistor.

Pin #	Signal Name	I/O	Description
24	uP_TEST1	I	This is connected to TEST1 pin on the LH79524 processor. A high state on this signal is required for normal processor operation. Tying this signal low enables JTAG / ICE mode. This signal is pulled up to 3.3V through a 10K resistor.
25	uP_nIRQC	I	Active Low. Dedicated hardware interrupt on LH79524-10. This interrupt is readable and maskable in the CPLD. See the IO controller specification for detailed information on accessing CPLD interrupts. This signal is pulled up to 3.3V through a 10K resistor.
26	uP_TEST2	I	This is connected to TEST2 pin on the LH79524 processor. For normal mode leave open. For more information, please see the section on Operating Modes in the LH79524 technical datasheet for detailed operation. This signal is pulled up to 3.3V through a 10K resistor to put the processor in normal operation mode.
27	uP_nIRQB	I	Active Low. Dedicated hardware interrupt on LH79524-10. This signal is pulled up to 3.3V through a 10K resistor.
28	uP_nTRST	I	Active Low. Used by JTAG tools to assert reset to the processor JTAG interface. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
29	uP_nIRQA	I	Active Low. Dedicated hardware interrupt on LH79524-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V through a 10K resistor.
30	uP_TMS	I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
31		NC	No internal connection (not implemented on the LH79524-10)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use. This signal is pulled up to 3.3V through a 10K resistor.
33		NC	No internal connection (not implemented on the LH79524-10)
34	uP_TDI	I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
35		NC	No internal connection (not implemented on the LH79524-10)
36	uP_TCK	I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
37	uP_nWAIT	I	Active low. This is the processor's wait signal. The CPLD ISA I/O Ready signal may drive this signal low. See the LH79524-10 IO Controller Specification for further details. This signal is pulled up to 3.3V through a 1K resistor.
38	uP_MODE3	I	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished in the CPLD. uP_MODE3 low at reset causes assertion of BOOT_nCS for external boot devices. See LH79524-10 IO controller specification for detailed information on boot device selection. This defaults to high (onboard flash) if left unconnected (pulled to 3.3V through a 10K pullup resistor).
39	uP_UARTA_RTS (UP_UARTA_RTS – DREQ)	O	The LH79524 UART0 RTS signal. Tied to 3.3V through a 10K resistor.
40	uP_MODE2	I	The LH79524 processor only supports Little Endian memory operations. On development kits by Logic Product Development, the generic use of this pin is an Endian setting (0 = big endian, 1 = little endian). This defaults to high (Little Endian) if left unconnected (pulled to 3.3V through a 10K pullup resistor). This pin can also be used as a General Purpose input and read from the CPLD register.
41	uP_UARTA_CTS (uP_UARTA_CTS – nDACK)	I	The LH79524 UART0 CTS signal. Tied to 3.3V through a 10K resistor.
42	uP_MODE1	I	Bus width setting. uP_MODE1/uP_MODE0 is tied - 0/x = 16 bit boot width. 1/x = 8 bit boot width. The card engine default is pulled to 16 bit boot width through 10K pull downs to ground. Alternate boot configurations are supported. Reference the LH79524 Users Guide for detailed boot time operation.

Pin #	Signal Name	I/O	Description
43	uP_UARTA_TX	O	UART0 transmit output signal. Internally pulled up on the LH79524 processor.
44	uP_MODE2	I	The LH79524 processor only supports Little Endian memory operations. On development kits by Logic Product Development, the generic use of this pin is an Endian setting (0 = big endian, 1 = little endian). This defaults to high (Little Endian) if left unconnected (pulled to 3.3V through a 10K pullup resistor). This pin can also be used as a General Purpose input and read from the CPLD register.
45	uP_UARTA_RX	I	Serial Communication Interface (UART0) data input. Has pullup to 3.3V through a 10K resistor.
46		NC	No internal connection (not implemented on the LH79524-10)
47		NC	No internal connection (not implemented on the LH79524-10)
48	DREQ0 (uP_UARTA_RTS – DREQ)	I/O	DMA request 0 signal. This signal is multiplexed with UARTA _RTS signal. This signal has a 10K pull up to 3.3V. This signal is only externally connected when R114 is populated. R114 is not populated by default.
49		NC	No internal connection (not implemented on the LH79524-10)
50		NC	No internal connection (not implemented on the LH79524-10)
51	nSUSPEND	I	Active low. This signal is one of the CPLD interrupts and is meant to activate software that will suspend LH79524 operations. This pin is connected directly to the CPLD and it is pulled up to 3.3V by a 10k resistor. Software is required for proper suspend operation.
52		NC	No internal connection (not implemented on the LH79524-10)
53	uP_AUX_CLK	O	This signal is a programmable auxiliary clock. Refer to processor documentation for available output frequencies.
54		NC	No internal connection (not implemented on the LH79524-10)
55	DGND	I	Digital Ground (0V)
56	nDACK0 (uP_UARTA_CTS – nDACK)	I/O	DMA acknowledge 0 signal. This signal is multiplexed with UARTA_CTS. This signal has a 10K pull up to 3.3V. This signal is only externally connected when R115 is populated. R115 is not populated by default.
57	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
58	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
59	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
60	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply and VCORE as the only powered supplies during Standby power down mode.
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply and VCORE as the only powered supplies during Standby power down mode.
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply and VCORE as the only powered supplies during Standby power down mode.
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply and VCORE as the only powered supplies during Standby power down mode.
65		NC	No internal connection (not implemented on the LH79524-10)
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 51.6MHz and is connected to the SDRAM as well as the CPLD.
67		NC	No internal connection (not implemented on the LH79524-10)
68	DGND	I	Digital Ground (0V)
69		NC	No internal connection (not implemented on the LH79524-10)
70	uP_nRAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into row addressing mode.
71		NC	No internal connection (not implemented on the LH79524-10)

Pin #	Signal Name	I/O	Description
72	uP_nCAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into column addressing mode.
73	uP_D0	I/O	Data Bus bit 0.
74	uP_nWE3	O	Active low. Byte lane enable for data bus bits 24->31.
75	uP_D1	I/O	Data Bus bit 1.
76	uP_nWE2	O	Active Low. Byte lane enable for data bus bits 16->23
77	uP_D2	I/O	Data Bus bit 2.
78	uP_nWE1	O	Active Low. Byte lane enable for data bus bits 8->15.
79	uP_D3	I/O	Data Bus bit 3.
80	uP_nWE0	O	Active low. Byte lane enable for data bus bits 0->7.
81	uP_D4	I/O	Data Bus bit 4.
82	uP_nWR	O	Active Low. When low, this signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal is asserted whenever the processor nWE signal is asserted so it can be used in both synchronous and asynchronous memory areas.
83	uP_D5	I/O	Data Bus bit 5.
84	uP_nRD	O	Active low. This signal is the read strobe that latches data output from external peripherals. This signal is asserted by the processor nOE signal.
85	uP_D6	I/O	Data Bus bit 6.
86		NC	No internal connection (not implemented on the LH79524-10)
87	uP_D7	I/O	Data Bus bit 7.
88		NC	No internal connection (not implemented on the LH79524-10)
89	DGND	I	Digital Ground (0V)
90	uP_A0	O	Address Bus bit 0.
91	uP_D8	I/O	Data Bus bit 8.
92	uP_A1	O	Address Bus bit 1.
93	uP_D9	I/O	Data Bus bit 9.
94	uP_A2	O	Address Bus bit 2.
95	uP_D10	I/O	Data Bus bit 10.
96	uP_A3	O	Address Bus bit 3.
97	uP_D11	I/O	Data Bus bit 11.
98	uP_A4	O	Address Bus bit 4.
99	uP_D12	I/O	Data Bus bit 12.
100	uP_A5	O	Address Bus bit 5.
101	uP_D13	I/O	Data Bus bit 13.
102	uP_A6	O	Address Bus bit 6.
103	uP_D14	I/O	Data Bus bit 14.
104	uP_A7	O	Address Bus bit 7.
105	uP_D15	I/O	Data Bus bit 15.
106	uP_A8	O	Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)
108	uP_A9	O	Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_A10	O	Address Bus bit 10.
111	uP_D16	I/O	Data Bus bit 16.
112	uP_A11	O	Address Bus bit 11.
113	uP_D17	I/O	Data Bus bit 17.
114	uP_A12	O	Address Bus bit 12.
115	uP_D18	I/O	Data Bus bit 18.
116	uP_A13	O	Address Bus bit 13.
117	uP_D19	I/O	Data Bus bit 19.
118	uP_A14	O	Address Bus bit 14.
119	uP_D20	I/O	Data Bus bit 20.
120	uP_A15	O	Address Bus bit 15.
121	uP_D21	I/O	Data Bus bit 21.

Pin #	Signal Name	I/O	Description
122	uP_A16	O	Address Bus bit 16.
123	uP_D22	I/O	Data Bus bit 22.
124	uP_A17	O	Address Bus bit 17.
125	uP_D23	I/O	Data Bus bit 23.
126	uP_A18	O	Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128		O	This signal is tied to ground through a 10K resistor.
129	uP_D24	I/O	Data Bus bit 24.
130	uP_A19	O	Address Bus bit 19.
131	uP_D25	I/O	Data Bus bit 25.
132	uP_A20	O	Address Bus bit 20.
133	uP_D26	I/O	Data Bus bit 26.
134	uP_A21	O	Address Bus bit 21.
135	uP_D27	I/O	Data Bus bit 27.
136	uP_A22	O	Address Bus bit 22.
137	uP_D28	I/O	Data Bus bit 28.
138		O	This signal is tied to ground through a 10K resistor.
139	uP_D29	I/O	Data Bus bit 29.
140	uP_A23	O	Address Bus bit 23.
141	uP_D30	I/O	Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_D31	I/O	Data Bus bit 31.
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC – SPS	O	LCD VSYNC (TFT Signal).
2	LCD_HSYNC – LP	O	LCD HSYNC (TFT Signal).
3	LCD_DCLK	O	LCD Panel Data Clock
4		NC	No internal connection (not implemented on the LH79524-10)
5	LCD_MDISP – SPL	O	LCD enable signal (TFT signal).
6	LCD_VEEEN - MOD	O	Active high. This signal is the enable for the LCD panel Vee.
7	LCD_VDDEN	O	Active high. This signal is the LCD panel Vcc enable.
8		NC	No internal connection (not implemented on the LH79524-10)
9	DGND	I	Digital Ground (0V)
10	LCD_CLS	O	LCDCLS Signal Output (Row Driver Clock)– This signal is only used with a HR-TFT interface.
11	LCD_VSYNC - SPS	O	LCDSPS Signal Output (Row Reset) – This signal is only used with a HR-TFT interface.
12	LCD_PSAVE	O	LCDPS Signal Output (Power Save)–This signal is only used with a HR-TFT interface.
13	LCD_MDISP - SPL	O	LCDSPL Signal Output (Start Pulse Left) – This signal is only used with the HR-TFT interface.
14	LCD_HSYNC - LP	O	LCD Horizontal Sync Pulse/ Line clock (Latch Pulse) – This signal is only used with the HR-TFT interface.
15	LCD_VEEEN - MOD	O	LCDMOD is only used with a HR-TFT interface
16	LCD_REV – DON	O	LCDREV Signal Output (Grey Scale Voltage Reverse) – This signal is only used with the HR-TFT interface.
17	uP_STATUS_1	O	GPIO pin on the I/O Controller. Logic Loader uses to drive a status LED on the SDK.
18	uP_STATUS_2	O	GPIO pin on the I/O Controller. Logic Loader uses to drive a status LED on the SDK.
19	uP_I2S_BCK	O	Clock output from the onboard I2S interface. If no CODEC is populated, an external CODEC or other device could use this signal.
20		NC	No internal connection (not implemented on the LH79524-10)
21	uP_I2S_SWS	O	This signal is the I2S sync output to an I2S compliant audio CODEC. The CODEC Frequency is set on the CODEC, while the default frequency for the sync is set up on the processor.
22	uP_I2S_RX – UARTC_RX	I	This signal is the I2S output from the CODEC to the processor.
23	uP_I2S_TX – UARTC_TX	O	This signal is the I2S output from the processor to the I2S compliant CODEC.
24	DGND	I	Digital Ground (0V)
25	A/D1	I	Analog input into the processor: 0 to 3.3V swing possible.
26	A/D2	I	Analog input into the processor: 0 to 3.3V swing possible
27	AGND	I	Analog Ground (0V)
28	HP_OUTL	O	Left headphone output from onboard CODEC.
29	HP_OUTR	O	Right headphone output from onboard CODEC.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio CODEC.
32	CODEC_INR	I	Right channel stereo line input of the audio CODEC.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Texas Instruments #TLV320AIC23GQE Stereo Audio CODEC Technical Datasheet for more details.

Pin #	Signal Name	I/O	Description
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Texas Instruments #TLV320AIC23GQE Stereo Audio CODEC Technical Datasheet for more details.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch panel controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch panel controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch panel controller.
39	TOUCH_TOP	I	This is the X- position input to the four-wire resistive touch panel controller.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. Note that R0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and G0, which are connected to LCD_D15 on the processor
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1 is connected to LCD_D0.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2 is connected to LCD_D1.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3 is connected to LCD_D2.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4 is connected to LCD_D3.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5 is connected to LCD_D4.
48	G0	O	The LCD data bus used to transmit data to the LCD module. Note that G0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and R0, which are connected to LCD_D15 on the processor
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1 is connected to LCD_D5.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2 is connected to LCD_D6.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3 is connected to LCD_D7.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4 is connected to LCD_D8.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5 is connected to LCD_D9.
54	B0	O	The LCD data bus used to transmit data to the LCD module. Note that B0 is an intensity bit for the LCD display and therefore is tied to the other intensity bits, G0 and R0, which are connected to LCD_D15 on the processor.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1 is connected to LCD_D10.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2 is connected to LCD_D11.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3 is connected to LCD_D12.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4 is connected to LCD_D13.

Pin #	Signal Name	I/O	Description
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5 is connected to LCD_D14.
61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. See the LH79524-10 IO Controller Specification for further details. This signal is pulled up to 3.3V through a 10K resistor.
62	RSVD_1	I	This signal is connected to the onboard CPLD and should not be interfaced to. This signal is pulled up to 3.3V through a 10K resistor.
63	CPLD_GPIO_1	I/O	This signal is a general purpose output (GPIO), which in this case, is used to drive the GPIO LED on the application board (such as the SDK). For more information on how this signal is driven, see the LH79524-10 IO Controller Specification.
64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O (GPIO). It is controlled by a memory-mapped address in the CPLD. See the LH79524-10 IO Controller Specification for further details.
65		NC	No internal connection (not implemented on the LH79524-10)
66	DGND	I	Digital Ground (0V)
67	uP_USB1_nOVR_CRNT - VBUS	I	Active HIGH. This is a detect signal used to determine whether or not the USB interface is currently in use. This signal is pulled down to GND through a 365K resistor. See SDK baseboard schematics for proper USB interfacing.
68		NC	No internal connection (not implemented on the LH79524-10)
69	uP_USB1_PWR_EN	O	Active high. Enables power supply for USB. See SDK baseboard schematics for proper USB interfacing.
70		NC	No internal connection (not implemented on the LH79524-10)
71		NC	No internal connection (not implemented on the LH79524-10).
72	uP_USB1_M	I/O	USB data I/O minus. Route as a differential pair with uP_USB1_P.
73	uP_USB1_P	I/O	USB data I/O plus. Route as a differential pair with uP_USB1_M.
74		NC	No internal connection (not implemented on the LH79524-10)
75	BUFF_DIR_ADDRESS	O	This signal is tied to through a 10K resistor to GND indicating the address bus is always driven from the Card Engine.
76	BUFF_DIR_DATA	O	Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). See the LH79524-10 IO Controller Specification for further details.
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the I2S compliant audio CODEC. Please see the Texas Instruments #TLV320AIC23GQE Stereo Audio CODEC Technical Datasheet for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different card engines.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different card engines.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled down through a 10K resistor to digital GND.
2	CPLD_TDO	O	This input transmits data out of the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
3	CPLD_TMS	I	This input indicates the mode of CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
4	CPLD_TDI	I	This input receives data on the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
5		NC	No internal connection (not implemented on the LH79524-10)
6		NC	No internal connection (not implemented on the LH79524-10)
7		NC	No internal connection (not implemented on the LH79524-10)
8		NC	No internal connection (not implemented on the LH79524-10)
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection (not implemented on the LH79524-10)
11		NC	No internal connection (not implemented on the LH79524-10)
12		NC	No internal connection (not implemented on the LH79524-10)
13		NC	No internal connection (not implemented on the LH79524-10)
14		NC	No internal connection (not implemented on the LH79524-10)
15		NC	No internal connection (not implemented on the LH79524-10)
16		NC	No internal connection (not implemented on the LH79524-10)
17		NC	No internal connection (not implemented on the LH79524-10)
18		NC	No internal connection (not implemented on the LH79524-10)
19		NC	No internal connection (not implemented on the LH79524-10)
20		NC	No internal connection (not implemented on the LH79524-10)
21	DGND	I	Digital Ground (0V)

Pin #	Signal Name	I/O	Description
22		NC	No internal connection (not implemented on the LH79524-10)
23		NC	No internal connection (not implemented on the LH79524-10)
24		NC	No internal connection (not implemented on the LH79524-10)
25		NC	No internal connection (not implemented on the LH79524-10)
26	uP_nDQM3	O	Active Low. This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[24:31].
27	uP_nDQM2	O	Active Low. This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[16:23].
28	uP_nDQM1	O	Active Low. This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[8:15].
29	uP_nDQM0	O	Active Low. This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[0:7].
30	uP_UARTB_TX - IRTX	O	This is the IrDA Transmit signal, which is used for the Infrared Mode on UARTC.
31	uP_UARTB_RX - IRRX	I	This is the IrDA Receive signal, which is used for the Infrared Mode on UARTC. This signal is pulled up to 3.3V through a 10K resistor.
32	DGND	I	Digital Ground (0V)
33		NC	No internal connection (not implemented on the LH79524-10)
34		NC	No internal connection (not implemented on the LH79524-10)
35		NC	No internal connection (not implemented on the LH79524-10)
36		NC	No internal connection (not implemented on the LH79524-10)
37		NC	No internal connection (not implemented on the LH79524-10)
38		NC	No internal connection (not implemented on the LH79524-10)
39		NC	No internal connection (not implemented on the LH79524-10)
40		NC	No internal connection (not implemented on the LH79524-10)
41	uP_UARTB_TX – IRTX	O	UART 2 transmit output signal on the LH79524. May also be configured as a LH79524 GPIO pin.
42	uP_UARTB_RX – IRRX	I	UART 2 receive input signal on the LH79524. May also be configured as a LH79524 GPIO pin. This signal is pulled up to 3.3V through a 10K resistor.
43		NC	No internal connection (not implemented on the LH79524-10)
44	DGND	I	Digital Ground (0V)
45		NC	No internal connection (not implemented on the LH79524-10)
46	uP_I2S_TX - UARTC_TX	O	UARTC transmit output signal on the LH79524.
47	uP_I2S_RX - UARTC_RX	I	UARTC receive input signal on the LH79524.
48		NC	No internal connection (not implemented on the LH79524-10)
49		NC	No internal connection (not implemented on the LH79524-10)

Pin #	Signal Name	I/O	Description
50	MFP11 – uP_PA3/CTCAP0B/CTCMP0B	I/O	GPIO pin, Port A bit 3 I/O
51		NC	No internal connection (not implemented on the LH79524-10)
52		NC	No internal connection (not implemented on the LH79524-10)
53		NC	No internal connection (not implemented on the LH79524-10)
54		NC	No internal connection (not implemented on the LH79524-10)
55	DGND	I	Digital Ground (0V)
56	MFP16 – uP_PJ4/AD3	I	Digital or Analog GPIO, Port J bit 4, A/D bit 3
57	MFP17 – uP_PJ2/AD4	I	Digital or Analog GPIO, Port J bit 2, A/D bit 4
58	MFP18 - uP_PA5/CTCAP1A/CTCMP1B	I/O	GPIO pin, Port A bit 5 I/O
59	MFP19 – uP_PA4/CTCAP1A/CTCMP1A	I/O	GPIO pin, Port A bit 4 I/O
60		NC	No internal connection (not implemented on the LH79524-10)
61		NC	No internal connection (not implemented on the LH79524-10)
62		NC	No internal connection (not implemented on the LH79524-10)
63	MFP23 - uP_PA7/CTCAP2B/CTCMP2B/SCL	I/O	GPIO pin, Port A bit 7 I/O
64	MFP24 - uP_PA6/CTCAP2A/CTCMP2A/SDA	I/O	GPIO pin, Port A bit 6 I/O
65		NC	No internal connection (not implemented on the LH79524-10)
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection (not implemented on the LH79524-10)
68		NC	No internal connection (not implemented on the LH79524-10)
69		NC	No internal connection (not implemented on the LH79524-10)
70	MFP29 - uP_SDCKE	O	LH79524 SDRAM controllers SDCKE signal. This signal is used to interface with external SDRAM Ics.
71		NC	No internal connection (not implemented on the LH79524-10)
72	MFP31 - uP_nSDCS1	O	Active low. This signal is the processor's Synchronous Memory Chip Select 1.
73	MFP32 - uP_nRESETOUT	O	Active low. This signal is asserted by the processor whenever it is in a reset state.
74		NC	No internal connection (not implemented on the LH79524-10)
75	MFP34 – CODEC_CLKOUT	O	The signal is the CODEC clock output.
76		NC	No internal connection (not implemented on the LH79524-10)
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection (not implemented on the LH79524-10)
79		NC	No internal connection (not implemented on the LH79524-10)
80		NC	This signal is tied to ground through a 10k ohm resistor for compatibility with other card engine processor products.

5.4 Multiplexed Signal Trade-Offs

5.4.1 GPIO vs Functionality Trade Offs

The LH79524 MUXCTL1 to MUXCTL25 registers control how the LH79524 processor pins are used. If a peripheral feature of the chip is not used, the MUXCTL registers can be used to enable GPIO or alternate functionality on each pin. The following tables indicate some signals that can be used as alternate functions including GPIO's.

5.4.2 J1C Connector SO-DIMM 144-Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
27	uP_nIRQB	INT1	Interrupt 1 Input	PJ6	Port J bit 6 (I only)
39	uP_UARTA_RTS – DREQ	UARTA RTS	UARTA RTS	PB1	Port B bit 1 I/O
41	uP_UARTA_CTS – nDACK	UARTA CTS	UARTA CTS	PB0	Port B bit 0 I/O
43	uP_UARTA_TX	UARTA TX	UARTA TX	PB7	Port B bit 7 I/O
45	uP_UARTA_RX	UARTA RX	UARTA RX	PB6	Port B bit 6 I/O

5.4.3 J1A Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1, 11	LCD_VSYNC - SPS	LCDVSYNC	TFT LCD Vertical Sync Pulse Output	LCDFP, PF7	STN LCD Frame Pulse Output, Port F bit 7 I/O
2, 14	LCD_HSYNC - LP	LCDHSYNC	TFT LCD Horizontal Sync Pulse Output	LCDLP, PE0	STN LCD Line Sync Pulse Output, Port E bit 0 I/O
3	LCD_DCLK	LCDDCLK	LCD Data Clock	PE1	Port E bit 1 I/O
5, 13	LCD_MDISP - SPL	LCDENAB	TFT LCD Data Enable	LCDSPL, PF6	ADTFT/HRTFT LCD SPL Signal Output (line start pulse left), Port F bit 6 I/O
7	LCD_ VDDEN	LCDVDDEN	LCDVDDEN (Digital supply enable)	PE5	Port E bit 5 I/O
10	LCD_CLS	LCDCLS	ADTFT/HRTFT LCD CLS Signal Output (Gate Driver Clock)	PE3	Port E bit 3 I/O
12	LCD_PSAVE	LCDPS	ADTFT/HRTFT LCD PS (power save)	PE2	Port E bit 2 I/O
15	LCD_VEEEN - MOD	LCDVEEEN	LCDVEEEN (VEE enable)	LCDMOD, PE6	LCD MOD signal, Port E bit 6 I/O
16	LCD_REV - DON	LCDREV	ADTFT/HRTFT LCD REV Signal Output (AC bias)	LCDDON, PE4	LCD SPLEN signal, Port E bit 4 I/O
19	uP_I2S_BCK	I2S_BCK	I2S Clock	PB3	Port B bit 3 I/O
21	uP_I2S_SWS	I2S_SWS	I2S Sync	PB2	Port B bit 2 I/O
22	uP_I2S_RX – UARTC_RX	UARTRX1	UART1 Receive	I2SRX, PB4	I2S Receive, Port B bit 4 I/O
23	uP_I2S_TX – UARTC_TX	UARTTX1	UART1 Transmit	I2STX, PB5	I2S Transmit, Port B bit 5 I/O
25	A/D1	A/D1	Analog input to processor	PJ1	Port J bit 1 (I only)

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
26	A/D2	A/D2	Analog input to processor	PJ5	Port J bit 5 (I only)
36	TOUCH_LEFT	TOUCHLEFT	Touch screen left	PJ3	Port J bit 3 (I only)
37	TOUCH_RIGHT	TOUCHRIGHT	Touch screen right	PJ0	Port J bit 0 (I only)
42	R1	LCDVD0	LCD Data 0	PG2	Port G bit 2 I/O
43	R2	LCDVD1	LCD Data 1	PG3	Port G bit 3 I/O
45	R3	LCDVD2	LCD Data 2	PG4	Port G bit 4 I/O
46	R4	LCDVD3	LCD Data 3	PG5	Port G bit 5 I/O
47	R5	LCDVD4	LCD Data 4	PG6	Port G bit 6 I/O
49	G1	LCDVD5	LCD Data 5	PG7	Port G bit 7 I/O
50	G2	LCDVD6	LCD Data 6	PF0	Port F bit 0 I/O
51	G3	LCDVD7	LCD Data 7	PF1	Port F bit 1 I/O
52	G4	LCDVD8	LCD Data 8	PF2	Port F bit 2 I/O
53	G5	LCDVD9	LCD Data 9	PF3	Port F bit 3 I/O
54, 48, 41	B0, R0, G0	LCDVD15	LCD Intensity (same signal on these pins)	PL1	Port L bit 7 I/O
56	B1	LCDVD10	LCD Data 10	PF4	Port F bit 4 I/O
57	B2	LCDVD11	LCD Data 11	PF5	Port F bit 5 I/O
58	B3	LCDVD12	LCD Data 12	PL2	Port L bit 2 I/O
59	B4	LCDVD13	LCD Data 13	PL3	Port L bit 3 I/O
60	B5	LCDVD14	LCD Data 14	PL0	Port L bit 0 I/O

5.4.4 J1B Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
30,41	uP_UARTB_TX - IRTX	UARTTX2	UART B TX Output Only	UARTIRTX2, PA1	IRDA TX2, Port A bit 1 I/O
31,42	uP_UARTB_RX – IRRX	UARTRX2	UART B RX Input Only	UARTIRRX2, PA0	IRDA RX2, Port A bit 0 I/O
46	uP_I2S_TX - UARTC_TX	UARTRX1	UART1 Receive	I2SRX, PB4	I2S Receive, Port B bit 4 I/O
47	uP_I2S_RX – UARTC_RX	UARTTX1	UART1 Transmit	I2STX, PB5	I2S Transmit, Port B bit 5 I/O
50	MFP11 – uP_PA3/CTCAP0B/ CTCMP0B	PA3	Port A bit 3 I/O	CTCAP0B	Capture Register B
56	MFP16 – uP_PJ4/AD3	AD3	Analog pin 3	PJ4	Port J bit 4 (I only)
57	MFP17 – uP_PJ2/AD4	AD4	Analog pin 4	PJ2	Port J bit 2 (I only)
58	MFP18 - uP_PA5/CTCAP1A/ CTCMP1B	PA5	Port A bit 5 I/O	CTCAP1A	Capture Register A
59	MFP19 – uP_PA4/CTCAP1A/ CTCMP1A	PA4	Port A bit 4 I/O	CTCAP1A	Capture Register A
63	MFP23 - uP_PA7/CTCAP2B/ CTCMP2B/SCL	PA7	Port A bit 7 I/O	CTCAP2B	Capture Register B

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
64	MFP24 - uP_PA6/CTCAP2A/ CTCMP2A/SDA	PA6	Port A bit 6 I/O	CTCAP2A	Capture Register A

6 Unused Pin Treatments

6.1 J1C Connector SODIMM 144-Pin Unused Pin Treatments

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	Leave floating.
2	MSTR_nRST	I/O	Leave floating. Internal pull up.
3	ETHER_RX(+)	I	Leave floating.
4	uP_SW_nRESET	I	Leave floating.
5	ETHER_TX(-)	O	Leave floating.
6	FAST_nMCS	O	Leave floating.
7	ETHER_TX(+)	O	Leave floating.
8	SLOW_nMCS	O	Leave floating.
9	DGND	I	Required. Digital Ground (0V)
10	VIDEO_nCS	O	Leave floating.
11	ETHER_nACT_LED	O	Leave floating.
12	BOOT_nCS	O	Leave floating.
13	ETHER_nLNK_LED	O	Leave floating.
14	nIOWR	O	Leave floating.
15	nSTANDBY	I	Leave floating.
16	nIORD	O	Leave floating.
17	DGND	I	Required. Digital Ground (0V)
18	2.5V	O	Leave floating.
19	3.3V	I	Required. Power Supply (3.3V)
20	BALE	O	Leave floating.
21		NC	Leave floating. No internal connection
22	nCHRDY	I	Leave floating.
23	CPLD_nIRQD	I	Leave floating.
24	uP_TEST1	I	Leave floating. Internal pull up.
25	CPLD_nIRQC	I	Leave floating.
26	uP_TEST2	I	Leave floating. Internal pull up.
27	uP_nIRQB	I	Leave floating.
28	uP_nTRST	I	Leave floating. Internal pull up.
29	uP_nIRQA	I	Leave floating. Internal pull up.
30	uP_TMS	I	Leave floating. Internal pull up.
31		NC	Leave floating. No internal connection
32	uP_TDO	O	Leave floating.
33		NC	Leave floating. No internal connection
34	uP_TDI	I	Leave floating. Internal pull up.
35		NC	Leave floating. No internal connection
36	uP_TCK	I	Leave floating. Internal pull up.
37	uP_nWAIT	I	Leave floating. Internal pull up.
38	uP_MODE3	I	Leave floating.
39	uP_UARTA_RTS (uP_UARTA_RTS – DREQ)	O	Leave floating. Internal pull up.
40	uP_MODE2	I	Leave floating. Internal pull down.

Pin #	Signal Name	I/O	Description
41	uP_UARTA_CTS (uP_UARTA_CTS – nDACK)	I	Leave floating. Internal pull up.
42	uP_MODE1	I	Leave floating. Internal pull down.
43	uP_UARTA_TX	O	Leave floating. Internal pull down.
44	uP_MODE2	I	Leave floating. Internal pull down.
45	uP_UARTA_RX	I	Leave floating. Internal pull up.
46		NC	Leave floating. No internal connection
47		NC	Leave floating. No internal connection
48	DREQ0 (UP_UARTA_RTS – DREQ)	NC	Leave floating. No internal connection If external DMA functionality is required, please contact Logic Product Development for production boards with R114, R115 populated.
49		NC	Leave floating. No internal connection
50		NC	Leave floating. No internal connection
51	nSUSPEND	I	Leave floating.
52		NC	Leave floating. No internal connection
53	uP_AUX_CLK	O	Recommend termination load near connector. 75ohm resistor in series with 10pF capacitor to DGND.
54		NC	Leave floating. No internal connection
55	DGND	I	Required. Digital Ground (0V)
56	nDACK0 (uP_UARTA_CTS – nDACK)	NC	Leave floating. No internal connection If external DMA functionality is required, please contact Logic Product Development for production boards with R114, R115 populated.
57	VCORE	I	Required. VCORE is fixed at 1.8V.
58	VCORE	I	Required. VCORE is fixed at 1.8V.
59	VCORE	I	Required. VCORE is fixed at 1.8V.
60	VCORE	I	Required. VCORE is fixed at 1.8V.
61	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
62	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
63	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
64	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
65		NC	Leave floating. No internal connection
66	uP_BUS_CLK	O	Recommend termination load near connector. 75ohm resistor in series with 10pF capacitor to DGND.
67		NC	Leave floating. No internal connection
68	DGND	I	Required. Digital Ground (0V)
69		NC	Leave floating. No internal connection
70	uP_nRAS	O	Leave floating.
71		NC	Leave floating. No internal connection
72	uP_nCAS	O	Leave floating.
73	uP_D0	I/O	Leave floating. Internal pull down.
74	uP_nWE3	O	Leave floating.
75	uP_D1	I/O	Leave floating. Internal pull down.
76	uP_nWE2	O	Leave floating.
77	uP_D2	I/O	Leave floating. Internal pull down.
78	uP_nWE1	O	Leave floating.
79	uP_D3	I/O	Leave floating. Internal pull down.
80	uP_nWE0	O	Leave floating.

Pin #	Signal Name	I/O	Description
81	uP_D4	I/O	Leave floating. Internal pull down.
82	uP_nWR	O	Leave floating.
83	uP_D5	I/O	Leave floating. Internal pull down.
84	uP_nRD	O	Leave floating.
85	uP_D6	I/O	Leave floating. Internal pull down.
86		NC	Leave floating. No internal connection
87	uP_D7	I/O	Leave floating. Internal pull down.
88		NC	Leave floating. No internal connection
89	DGND	I	Required. Digital Ground (0V)
90	uP_A0	O	Leave floating.
91	uP_D8	I/O	Leave floating. Internal pull down.
92	uP_A1	O	Leave floating.
93	uP_D9	I/O	Leave floating. Internal pull down.
94	uP_A2	O	Leave floating.
95	uP_D10	I/O	Leave floating. Internal pull down.
96	uP_A3	O	Leave floating.
97	uP_D11	I/O	Leave floating. Internal pull down.
98	uP_A4	O	Leave floating.
99	uP_D12	I/O	Leave floating. Internal pull down.
100	uP_A5	O	Leave floating.
101	uP_D13	I/O	Leave floating. Internal pull down.
102	uP_A6	O	Leave floating.
103	uP_D14	I/O	Leave floating. Internal pull down.
104	uP_A7	O	Leave floating.
105	uP_D15	I/O	Leave floating. Internal pull down.
106	uP_A8	O	Leave floating.
107	3.3V	I	Leave floating.
108	uP_A9	O	Leave floating.
109	DGND	I	Required. Digital Ground (0V)
110	uP_A10	O	Leave floating.
111	uP_D16	I/O	Leave floating. Internal pull down.
112	uP_A11	O	Leave floating.
113	uP_D17	I/O	Leave floating. Internal pull down.
114	uP_A12	O	Leave floating.
115	uP_D18	I/O	Leave floating. Internal pull down.
116	uP_A13	O	Leave floating.
117	uP_D19	I/O	Leave floating. Internal pull down.
118	uP_A14	O	Leave floating.
119	uP_D20	I/O	Leave floating. Internal pull down.
120	uP_A15	O	Leave floating.
121	uP_D21	I/O	Leave floating. Internal pull down.
122	uP_A16	O	Leave floating. Internal pull down.
123	uP_D22	I/O	Leave floating. Internal pull down.
124	uP_A17	O	Leave floating. Internal pull down.
125	uP_D23	I/O	Leave floating. Internal pull down.
126	uP_A18	O	Leave floating. Internal pull down.

Pin #	Signal Name	I/O	Description
127	DGND	I	Required. Digital Ground (0V)
128		O	Leave floating. Internal pull down.
129	uP_D24	I/O	Leave floating. Internal pull down.
130	uP_A19	O	Leave floating. Internal pull down.
131	uP_D25	I/O	Leave floating. Internal pull down.
132	uP_A20	O	Leave floating. Internal pull down.
133	uP_D26	I/O	Leave floating. Internal pull down.
134	uP_A21	O	Leave floating. Internal pull down.
135	uP_D27	I/O	Leave floating. Internal pull down.
136	uP_A22	O	Leave floating. Internal pull down.
137	uP_D28	I/O	Leave floating. Internal pull down.
138		O	Leave floating. Internal pull down.
139	uP_D29	I/O	Leave floating. Internal pull down.
140	uP_A23	O	Leave floating. Internal pull down.
141	uP_D30	I/O	Leave floating. Internal pull down.
142	nAEN	O	Leave floating.
143	uP_D31	I/O	Leave floating. Internal pull down.
144	3.3V	I	Required. Power Supply (3.3V)

6.2 J1A Expansion Connector Unused Pin Treatments

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC - SPS	O	Leave floating. Internal pull down.
2	LCD_HSYNC – LP	O	Leave floating. Internal pull down.
3	LCD_DCLK	O	Leave floating. Internal pull down.
4		NC	Leave floating. No internal connection
5	LCD_MDISP - SPL	O	Leave floating. Internal pull down.
6	LCD_VEEEN – MOD	O	Leave floating. Internal pull down.
7	LCD_VDDEN	O	Leave floating. Internal pull down.
8		NC	Leave floating. No internal connection
9	DGND	I	Required. Digital Ground (0V)
10	LCD_CLS	O	Leave floating. Internal pull down.
11	LCD_VSYNC - SPS	O	Leave floating. Internal pull down.
12	LCD_PSAVE	O	Leave floating. Internal pull down.
13	LCD_MDISP - SPL	O	Leave floating. Internal pull down.
14	LCD_HSYNC - LP	O	Leave floating. Internal pull down.
15	LCD_VEEEN - MOD	O	Leave floating. Internal pull down.
16	LCD_REV – DON	O	Leave floating. Internal pull down.
17	uP_STATUS_1	I/O	Leave floating.
18	uP_STATUS_2	I/O	Leave floating.
19	uP_I2S_BCK	O	Leave floating. Internal pull down.
20		NC	Leave floating. No internal connection
21	uP_I2S_SWS	O	Leave floating. Internal pull up.
22	uP_I2S_RX – UARTC_RX	I	Leave floating. Internal pull up.
23	uP_I2S_TX – UARTC_TX	O	Leave floating. Internal pull down.
24	DGND	I	Required. Digital Ground (0V)
25	A/D1	I	Leave floating.
26	A/D2	I	Leave floating.
27	AGND	I	Required. Analog Ground (0V)
28	HP_OUTL	O	Leave floating.
29	HP_OUTR	O	Leave floating.
30	3.3VA	I	Required. Analog Power Supply (3.3V)
31	CODEC_INL	I	Leave floating.
32	CODEC_INR	I	Leave floating.
33	CODEC_OUTL	O	Leave floating.
34	CODEC_OUTR	O	Leave floating.
35	AGND	I	Required. Analog Ground (0V)
36	TOUCH_LEFT	I	Leave floating.
37	TOUCH_RIGHT	I	Leave floating.
38	TOUCH_BOTTOM	I	Leave floating.
39	TOUCH_TOP	I	Leave floating.
40	3.3VA	I	Required. Analog Power Supply (3.3V)
41	R0	O	Leave floating. Internal pull down.
42	R1	O	Leave floating. Internal pull down.
43	R2	O	Leave floating. Internal pull down.
44	DGND	I	Required. Digital Ground (0V)
45	R3	O	Leave floating. Internal pull down.

Pin #	Signal Name	I/O	Description
46	R4	O	Leave floating. Internal pull down.
47	R5	O	Leave floating. Internal pull down.
48	G0	O	Leave floating. Internal pull down.
49	G1	O	Leave floating. Internal pull down.
50	G2	O	Leave floating. Internal pull down.
51	G3	O	Leave floating. Internal pull down.
52	G4	O	Leave floating. Internal pull up.
53	G5	O	Leave floating. Internal pull up.
54	B0	O	Leave floating. Internal pull down.
55	DGND	I	Required. Digital Ground (0V)
56	B1	O	Leave floating. Internal pull up.
57	B2	O	Leave floating. Internal pull up.
58	B3	O	Leave floating. Internal pull down.
59	B4	O	Leave floating. Internal pull down.
60	B5	O	Leave floating. Internal pull down.
61	CF_nCE	O	Leave floating.
62	RSVD_1	I	Leave floating.
63	CPLD_GPIO_1	I/O	Leave floating.
64	CPLD_GPIO_2	I/O	Leave floating.
65		NC	Leave floating. No internal connection
66	DGND	I	Required. Digital Ground (0V)
67	uP_USB1_nOVR_CRNT - VBUS	I	Leave floating.
68		NC	Leave floating. No internal connection
69	uP_USB1_PWR_EN	O	Leave floating.
70		NC	Leave floating. No internal connection
71		NC	Leave floating. No internal connection
72	uP_USB1_M	I/O	Leave floating.
73	uP_USB1_P	I/O	Leave floating.
74		NC	Leave floating. No internal connection
75	BUFF_DIR_ADDRESS	O	Leave floating. Internal pull down.
76	BUFF_DIR_DATA	O	Leave floating.
77	DGND	I	Required. Digital Ground (0V)
78	MIC_IN	I	Leave floating.
79	POWER_SENSE1	O	Leave floating.
80	POWER_SENSE2	O	Leave floating.

6.3 J1B Expansion Connector Unused Pin Treatments

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	Leave floating.
2	CPLD_TDO	O	Leave floating.
3	CPLD_TMS	I	Leave floating.
4	CPLD_TDI	I	Leave floating.
5		NC	Leave floating. No internal connection
6		NC	Leave floating. No internal connection
7		NC	Leave floating. No internal connection
8		NC	Leave floating. No internal connection
9	DGND	I	Required. Digital Ground (0V)
10		NC	Leave floating. No internal connection
11		NC	Leave floating. No internal connection
12		NC	Leave floating. No internal connection
13		NC	Leave floating. No internal connection
14		NC	Leave floating. No internal connection
15		NC	Leave floating. No internal connection
16		NC	Leave floating. No internal connection
17		NC	Leave floating. No internal connection
18		NC	Leave floating. No internal connection
19		NC	Leave floating. No internal connection
20		NC	Leave floating. No internal connection
21	DGND	I	Required. Digital Ground (0V)
22		NC	Leave floating. No internal connection
23		NC	Leave floating. No internal connection
24		NC	Leave floating. No internal connection
25		NC	Leave floating. No internal connection
26	uP_nDQM3	O	Leave floating.
27	uP_nDQM2	O	Leave floating.
28	uP_nDQM1	O	Leave floating.
29	uP_nDQM0	O	Leave floating.
30	uP_UARTB_TX - IRTX	O	Leave floating. Internal pull down.
31	uP_UARTB_RX - IRRX	I	Leave floating. Internal pull up.
32	DGND	I	Required. Digital Ground (0V)
33		NC	Leave floating. No internal connection
34		NC	Leave floating. No internal connection
35		NC	Leave floating. No internal connection
36		NC	Leave floating. No internal connection
37		NC	Leave floating. No internal connection
38		NC	Leave floating. No internal connection
39		NC	Leave floating. No internal connection
40		NC	Leave floating. No internal connection
41	uP_UARTB_TX - IRTX	O	Leave floating. Internal pull down.
42	uP_UARTB_RX – IRRX	I	Leave floating. Internal pull up.
43		NC	Leave floating. No internal connection
44	DGND	I	Required. Digital Ground (0V)
45		NC	Leave floating. No internal connection
46	uP_I2S_TX - UARTC_TX	O	Leave floating. Internal pull down.
47	uP_I2S_RX - UARTC_RX	I	Leave floating. Internal pull up.
48		NC	Leave floating. No internal connection
49		NC	Leave floating. No internal connection
50	MFP11 – uP_PA3/CTCAP0B/CTCMP0B	I/O	Leave floating. Internal pull down.
51		NC	Leave floating. No internal connection
52		NC	Leave floating. No internal connection
53		NC	Leave floating. No internal connection
54		NC	Leave floating. No internal connection

Pin #	Signal Name	I/O	Description
55	DGND	I	Required. Digital Ground (0V)
56	MFP16 – uP_PJ4/AD3	I	Leave floating.
57	MFP17 – uP_PJ2/AD4	I	Leave floating.
58	MFP18 - uP_PA5/CTCAP1A/CTCMP1B	I/O	Leave floating. Internal pull down.
59	MFP19 – uP_PA4/CTCAP1A/CTCMP1A	I/O	Leave floating. Internal pull down.
60		NC	Leave floating. No internal connection
61		NC	Leave floating. No internal connection
62		NC	Leave floating. No internal connection
63	MFP23 - uP_PA7/CTCAP2B/CTCMP2B/SCL	I/O	Leave floating. Internal pull up.
64	MFP24 - uP_PA6/CTCAP2A/CTCMP2A/SDA	I/O	Leave floating. Internal pull up.
65		NC	Leave floating. No internal connection
66	DGND	I	Required. Digital Ground (0V)
67		NC	Leave floating. No internal connection
68		NC	Leave floating. No internal connection
69		NC	Leave floating. No internal connection
70	MFP29 - uP_SDCKE	I/O	Leave floating.
71		NC	Leave floating. No internal connection
72	MFP31 - uP_nSDCS1	I/O	Leave floating.
73	MFP32 - uP_nRESETOUT	I/O	Leave floating.
74		NC	Leave floating. No internal connection
75	MFP34 – CODEC_CLKOUT	I/O	Leave floating.
76		NC	Leave floating. No internal connection
77	DGND	I	Required. Digital Ground (0V)
78		NC	Leave floating. No internal connection
79		NC	Leave floating. No internal connection
80		NC	Leave floating. Internal pull down.

7 Mechanical Specifications

7.1 Interface Connectors

The LH79524-10 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM Connector must be 3.7mm mating height.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

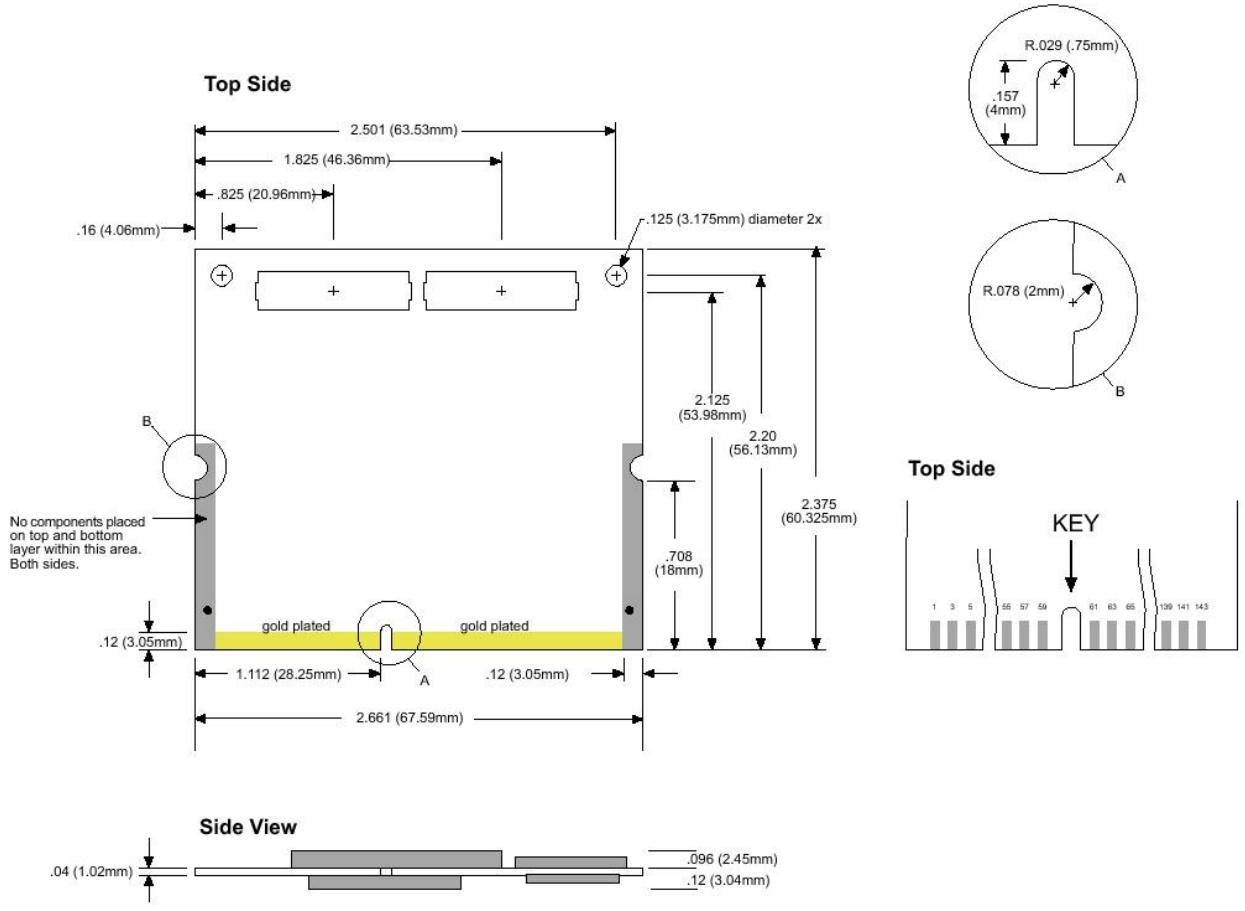

Figure 7.1: Card Engine Mechanical Drawing

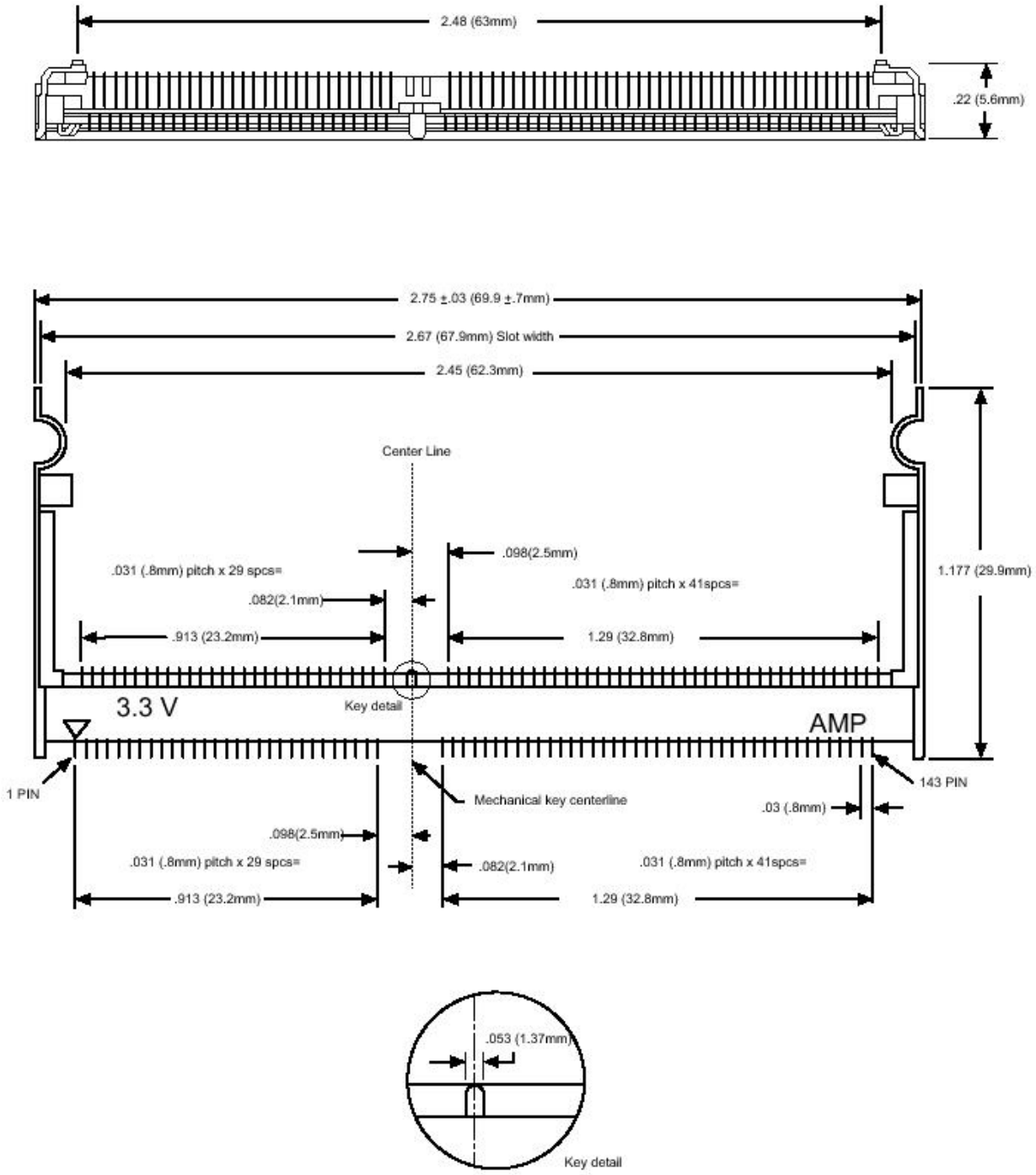

Figure 7.2: SODIMM Connector Specification

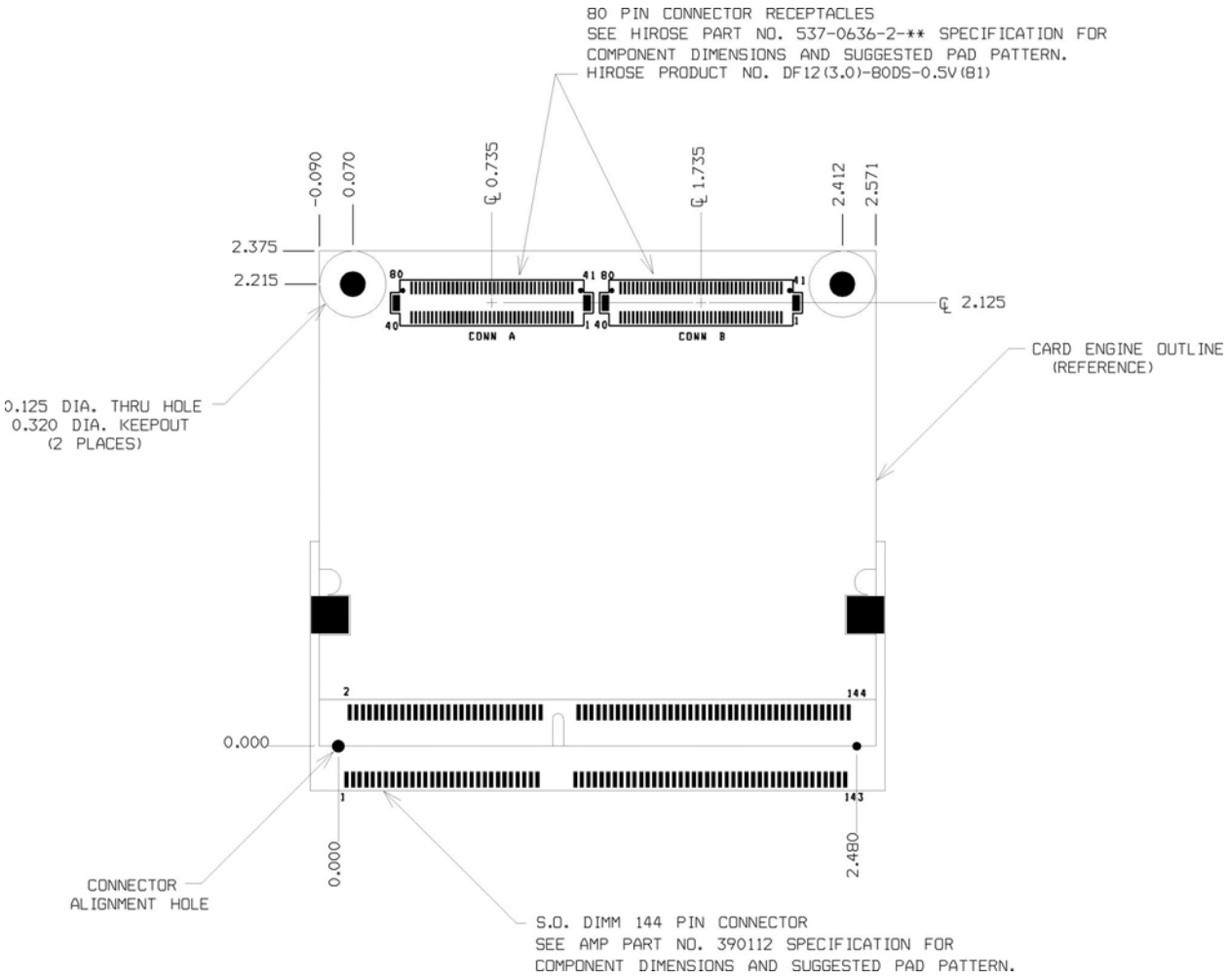

Figure 7.3: Recommended PCB Layout

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