LH79520-10
Card Engine

NANO

LOGIC

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	APPROVAL	DATE
1	Nate Kemp	First Draft Version	TDK	12/17/02
A	Troy Kopischke	Release	TDK	01/27/03
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F	Kurt Larson, Michael Anderson	Signal characteristics update, Product Brief Section update	KTL	12/22/03
G	Kurt Larson James Wicks	Corrected SODIMM Pin Descriptions: 76, 78, 80; added bookmark feature to .pdf	JAW	09/30/04

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H	Jed Anderson	Updated Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes	80000113 Rev F01	JCA	11/03/06

Please check www.logicpd.com for the latest revision of this manual, errata's, and additional application notes.

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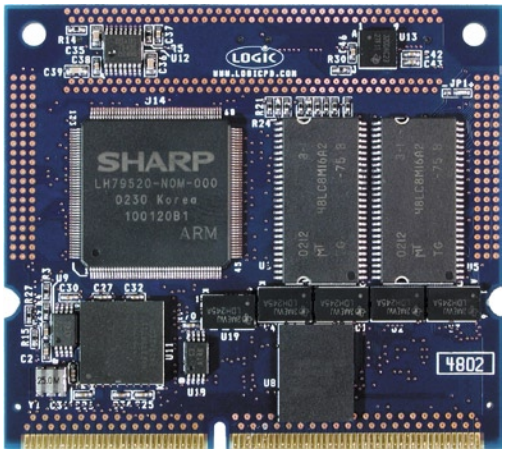
LH79520 CARD ENGINE

The LH79520 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

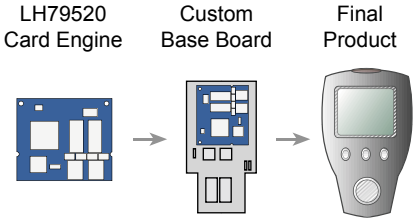
CARD ENGINE ADVANTAGE

- Reduce TIme to Market
  - ⟶ 6 to 9 month savings typical
- Product-Ready Hardware Platform
- Production Quality Software
  - Bootloader/Monitor
  - Board Support Packages
  - Supports other operating systems
- Engineering Support

The LH79520 Card Engine is a complete single board computer offering essential features for handheld and embedded networking applications in the industrial, consumer, and medical markets. The use of custom base boards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation microcontroller Card Engines when new functionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Sharp LH79520 32 bit ARM720T RISC processor running up to 77.414 MHz
- **SDRAM Memory** Up to 64 Mbytes
- **Flash Memory** Up to 16 Mbytes on board
- **Display** Programmable color LCD controller
  - Built in driver supports up to 800 x 600 x 16 bit color
  - Supports STN, Color STN, HR-TFT, AD-TFT, TFT
- **Touch Screen** Four wire resistive touch controller
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN91C111 (MAC & PHY)
- **Audio** Stereo Output Audio CODEC (TI TLV320DAC23)
- **PC Card Expansion** Compact Flash type 1 card (memory mode only)
- **Serial Ports** 2 X 16C550 like, standard UARTS
- **IrDA** SIR supports up to 115.2 Kbps
- **GPIO** Programmable depending on peripheral requirements
- **SSP** Supports either Motorola SPI™, National Semiconductor MICROWIRE™, TI SSI
- **USB 2.0 Full Speed** One Device
- **Software**
  - Linux BSP
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37"(60.2 mm) long x 2.67"(67.8 mm) wide x 0.17"(4.4 mm) high
  - 144 pin SODIMM connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

For more information on our EmbeddedProduct Solutions, please contact Logic Sales at www.logicpd.com or 612.672.9495.

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1.2 Acronyms

ADC	Analog to Digital Converter
AHB	Advanced Hardware Bus
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
IO	Input Output
LCD	Liquid Crystal Display
LOLO	LogicLoader™
NC	No Connect
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SSP	Synchronous Serial Port
TTL	Transistor Transistor Logic
UART	Universal Asynchronous Receive Transmit
VIC	Vectored Interrupt Controller

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

LH79520-10 IO Controller Interface Specification
LogicLoader™ User's Manual
LH79520 Universal Microcontroller User's Guide
Altera MAX 7000A CPLD data sheet (EPM7128A)
Altera Device Package Information data sheet
Altera Ordering Information
Texas Instruments TLV320DAC23 data manual
Texas Instruments (Burr-Brown) ADS7843 data sheet

1.4 Card Engine Advantages

Logic's Card Engines accelerate your products time to market. In addition, the Card Engines provide the following advantages:

- Product Ready Hardware & Software solutions allow immediate application development which results in embedded product development cycle with less time, less cost, less risk, with more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost

  - Less risk – complex portion of design product ready
  - More Innovation – Allows you to focus on your IP
- Common Card Engine Footprint (See Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

1.5 Card Engine Interface

The Card Engine's common interface allows you to easily migrate to new processors and technology. Logic is in constant research and development of new technologies to improve performance, lower cost and increase feature capabilities. By using the common footprint, you can leverage Logic's work without having to re-spin your product. Contact Logic sales for more information.

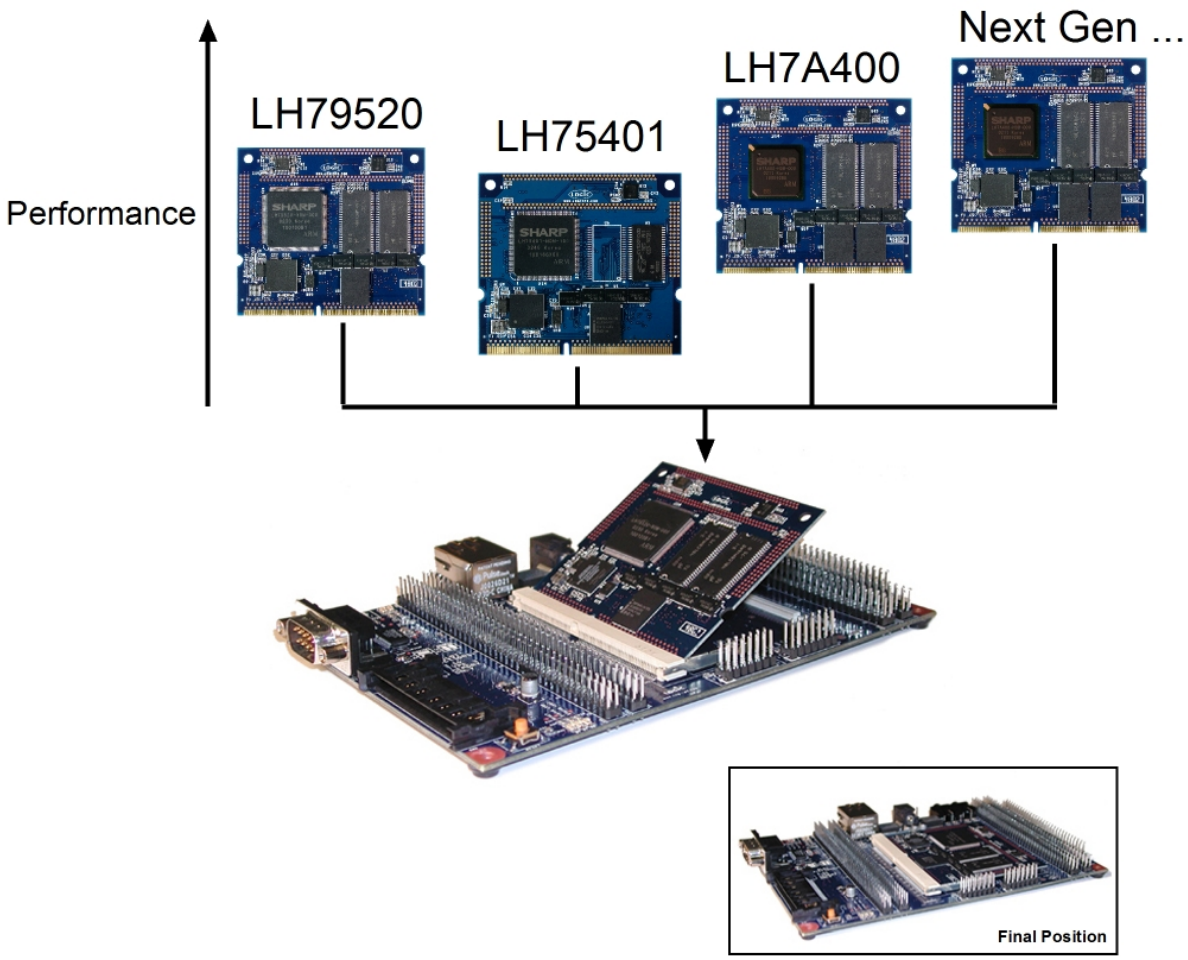


Figure 1.1: Card Engine Advantages

Encapsulating a significant amount of your design onto the Card Engine reduces risk of obsolescence issues. If a component on the Card Engine design becomes obsolete you don't have to re-spin your board, Logic will design for alternative part that is transparent to your product. Manufacturing also becomes much easier. Card Engines are delivered to you fully tested, making your manufacturing process simpler and less costly.

1.6 LH79520-10 Card Engine Block Diagram

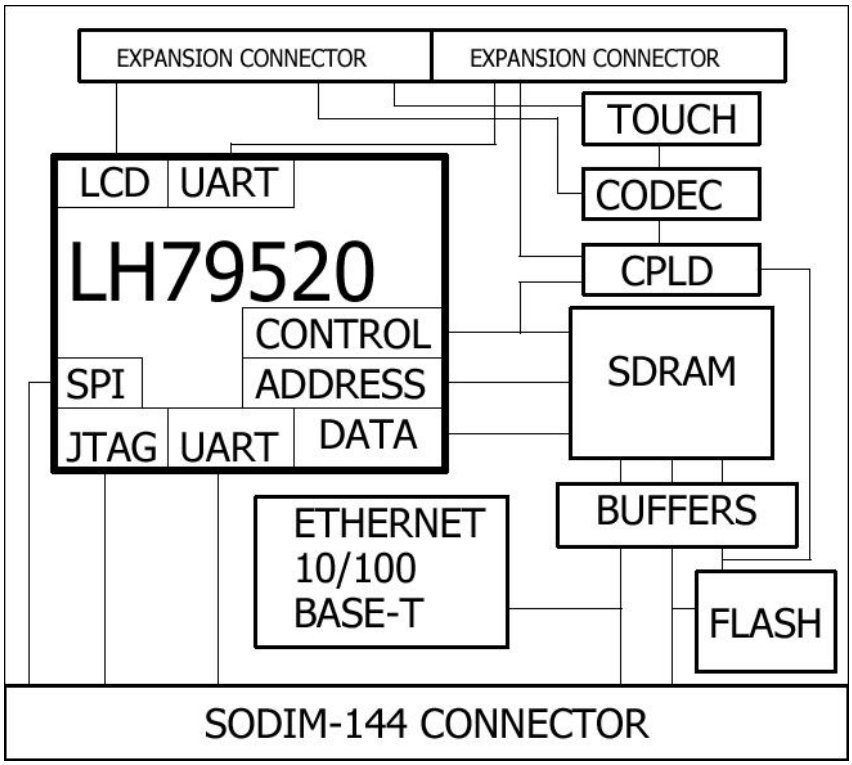


Figure 1.2: LH79520-10 Card Engine Block Diagram

1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	unit
DC IO and Peripheral Supply Voltage	3.3V	-0.3 to 4.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.4	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.7.2 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	TBD	240	TBD	mA	2
DC IO Supply Standby Current	TBD	180	TBD	mA	2
DC IO Supply Sleep Current	TBD	130	TBD	mA	2
DC Core Supply Voltage	1.62	1.8	1.98	V	1
DC Core Supply Active Current	TBD	40	TBD	mA	2
DC Core Supply Standby Current	TBD	30	TBD	mA	2
DC Core Supply Sleep Current	TBD	0	TBD	mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.6		VIO	V	
Output Signal Low Voltage	GND		0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. This test was performed with the 91C111 chip power disabled.
3. Contact Logic for more information on an industrial temperature LH79520-10 Card Engine
4. May vary depending on Card Engine configuration.

2 Electrical Specification

2.1 MicroController

2.1.1 LH79520 Microcontroller

The LH79520-10 Card Engine uses Sharp's highly integrated system on a chip LH79520 microcontroller. Sharp's LH79520 has a 32-bit ARM720T RISC core. Sharp's LH79520 microcontroller is a system on a chip providing many integrated on-chip peripherals including:

- Integrated ARM720T™ Core
  - 2 bit ARM7TDMI™ RISC Core
  - 8 KB Cache
  - MMU
- 32 KB on-chip SRAM
- Integrated LCD Controller
  - Up to 800 x 600 Resolution
  - Supports STN, TFT, HR-TFT
  - 64 k Colors
- Three UART's
- IrDA SIR up to 115.2 Kbps (UART0)
- SPI (UART2)
- Up to 64 General Purpose I/O Signals
- Two 16-bit Pulse Width Modulators
- Four DMA Channels (2 External)
- Four Counter/Timers
- RTC
- Low Power Modes
- 5 Volt Tolerant Inputs

See Sharp's LH79520 Universal Microcontroller User's Guide for additional information.
http://www.sharpsma.com/

IMPORTANT NOTE: Please see http://www.sharpsma.com/ for any errata on the LH79520.

2.1.2 LH79520 Microcontroller Block Diagram

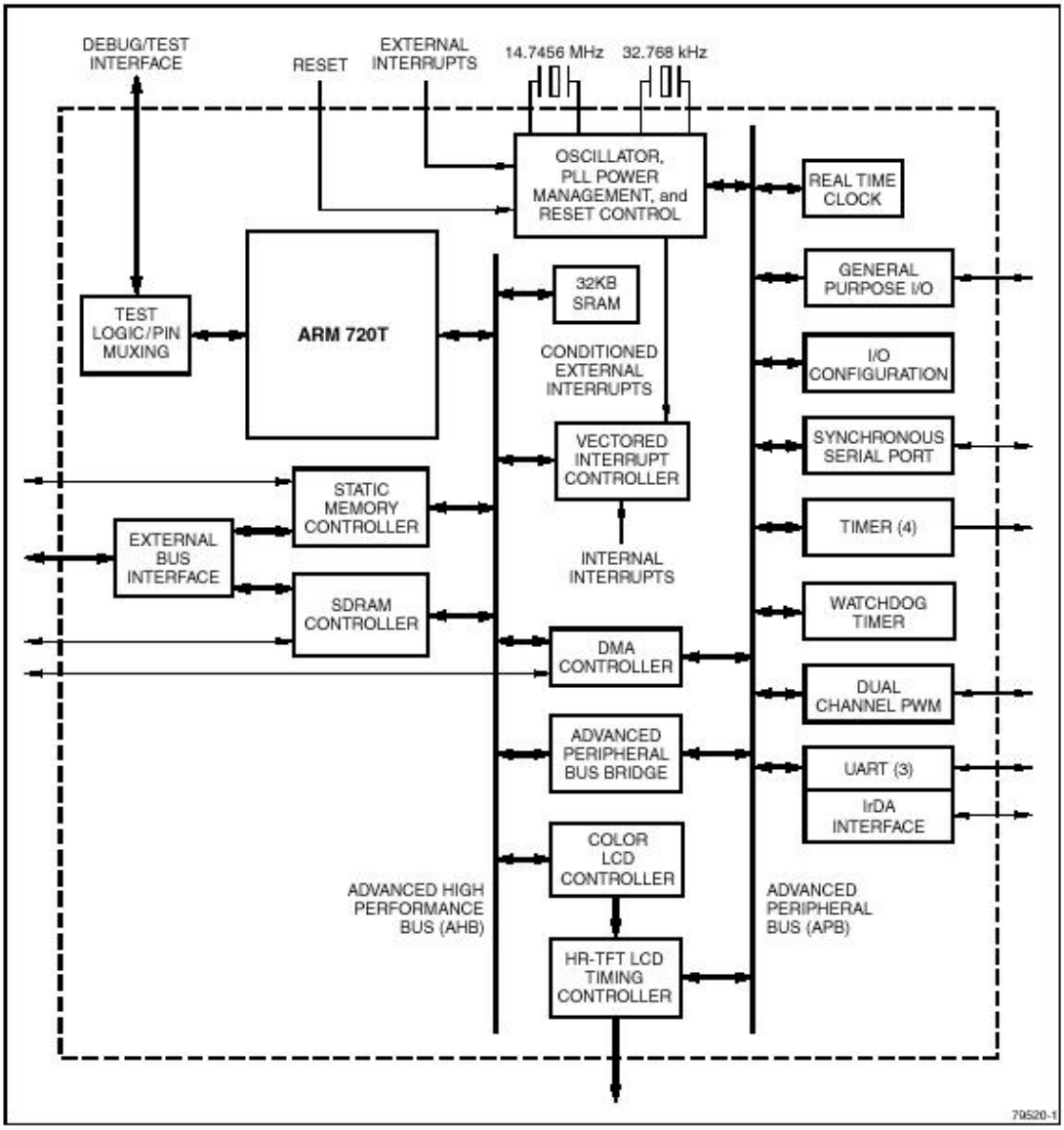


Figure 2.1: LH79520 Microcontroller Block Diagram

2.2 Clocks

The LH79520 uses a 14.7456 MHz crystal, which is scaleable in software to generate FCLK signal. FCLK is used internally for the ARM720T core and cache. The 14.7456 MHz crystal is also used to generate HCLK that is used to generate other bus and peripheral clocks. The 32.768 kHz crystal is used for the RTC interface.

The LH79520 is software configurable to select between asynchronous, synchronous, and FastBus extension clocking mode. The microcontroller has a sophisticated clocking architecture and can be software programmable tailored to an application to vary the microcontroller performance, power consumption, and bus throughput. See the LH79520 Universal Microcontroller User's Guide for more details.

The LH79520's microcontroller core clock speed is initialized to 51.6096 MHz on the Card Engine and the Bus speed is 51.6096 MHz in the LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH79520-10 Card Engine provides an external Bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector. The uP_BUS_CLK, the LH79520 Bus clock – SDCLK, is set to a default of 51.6096 MHz. The uP_BUS_CLK signal is programmable via the LH79520 clock registers.

The LH79520-10 Card Engine provides an external auxiliary clock, uP_AUX_CLK, on the 144-pin SO-DIMM connector. The uP_AUX_CLK, the LH79520 CLKOUT, is set to a default of 51.6096 MHz. The uP_AUX_CLK signal is programmable via the LH79520 clock registers.

LH79520 Microcontroller Signal Name	LH79520-10 Card Engine Net Name	Default Software Value in LogicLoader™
FCLK	NA	51.6096 MHz
HCLK	NA	51.6096 MHz
SDCLK	uP_BUS_CLK	51.6096 MHz
CLKOUT	uP_AUX_CLK	51.6096 MHz

2.3 Memory

2.3.1 Synchronous Dynamic Random Access Memory (DRAM)

The LH79520-10 Card Engine uses a 32-bit memory bus to interface to Synchronous DRAM. The memory can be configured as 16, 32 or 64 Mbytes to meet the user's memory requirements and cost constraints. The default memory configuration is a 32 Mbyte configuration.

2.3.2 Direct Memory Access (DMA)

The Sharp LH79520 microcontroller has an internal DMA controller and 2 external DMA channels. The standard LH79520-10 Card Engine uses DMA Channel 0 to interface with the onboard audio CODEC - Texas Instruments TLV320DAC23. The DMA channel 1 DREQ signal is multiplexed with the LH79520 nWAIT signal. By default, the nWAIT signal is used to interface with the onboard Ethernet controller - SMSC 91C111. DMA Channel 1 is available to the user through the expansion connectors if the user chooses to not use the nWAIT signal in the SMSC 91C111 Ethernet controller. The SMSC 91C111 can be configured in software to exclude the nWAIT signal functionality, providing DMA Channel 1 to the user. If an external DMA channel is required, please contact Logic Product Development.

2.3.3 NOR Flash

The LH79520-10 Card Engine uses a 16-bit memory bus to interface to Strataflash. The on board Card Engine memory can be configured as 8 or 16 Mbytes to meet the user's flash requirements and cost constraints. A user should consult Logic when specifying flash size because it is one of the most expensive components in the LH79520-10 Card Engine.

A user can expand their non-volatile storage capability using the LH79520-10 Card Engine Application Kit as a design reference. User's can expand their non-volatile storage capability by external flash ICs, CompactFlash, or NAND Flash. See the LH79520-10 Application Kit for reference designs or contact Logic for other reference designs of peripheral interfaces.

2.3.4 CompactFlash (memory-mapped mode only)

The LH79520 microcontroller does not have an on chip integrated CompactFlash controller. However, for applications requiring larger non-volatile storage, the LH79520-10 Card Engine provides the necessary signals using the IO Controller for a CompactFlash card interface in memory-mapped mode only. The Zoom™ Starter Kit reference design includes a CompactFlash

connector for memory-mapped mode, but does not support the hot-swappable capability. See the LH79520-10 IO Controller Interface Specification for further details.

IMPORTANT NOTE: Additional hardware is required on the user's daughter board to provide hot-swapping capability.

IMPORTANT NOTE: The IO Controller CompactFlash interface supports memory-mapped mode only. Designs requiring other CompactFlash modes should use an external controller or select a microcontroller with an integrated CompactFlash interface.

2.4 10/100 Ethernet Controller

The LH79520-10 Card Engine uses the SMSC 91C111 10/100 Ethernet single chip solution. The Card Engine Ethernet interface provides an easy to use interface. The Card Engine provides six signals from the 91C111: TPO+, TPO-, TPI+, TPI-, ACT_LED, and LNK_LED. The four analog PHY interface signals (TPO+, TPO-, TPI+, TPI-) require an external impedence matching circuit. Logic provides an example circuit schematics in the LH79520-10 Application Kit for reference.

IMPORTANT NOTE: Eneep signal on the SMSC 91C111 is connected to npR15 (zero ohm resistor) that is not populated. Eneep signal has an internal weak pull up in the SMSC 91C111. If Eneep signal is tied low it will disable the serial EEPROM interface.

2.5 Audio CODEC

The LH79520-10 Card Engine uses the TI TLV320DAC23GQE high performance low cost stereo audio CODEC. The TLV320DAC23GQE audio CODEC has a single channel stereo input and single channel stereo output, but the LH79520-10 Card Engine does not support stereo input on its standard card engine.

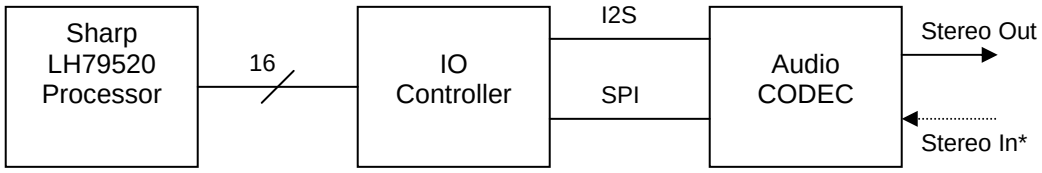


Figure 2.2: Audio CODEC Block Diagram

***IMPORTANT NOTE: Stereo In not supported in default LH79520-10 Card Engine**

The LH79520-10 Card Engine supports a 10-bit stereo out. The audio CODEC uses a 5.6448 MHz crystal. The audio CODEC is software programmable via the SPI interface in the IO Controller. See the IO Controller Interface Specification for programming information. The audio CODEC provides software programmable sample rates, volume control, mute, and power management. See the TI Audio CODEC specification for programmable register settings.

Logic has interfaced other high performance audio CODECs to the Card Engines. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

2.6 Video Interface

Sharp's LH79520 microcontroller has a built in LCD controller supporting STN, TFT, HR-TFT panels at 800 x 600 x 16 bit color max resolution. See the LH79520 Universal Microcontroller User's Guide for further information on the integrated LCD controller. The LCD controller signals from the LH79520 are located on one of the Card Engine's 80-pin expansion connectors. Logic

has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will effect processor performance. Selecting display resolutions and color bits per pixel will vary processor bus load.

2.7 Serial Interface

The LH79520-10 Card Engine comes with the following serial channels: UARTA, UARTB, and SPI. If additional serial channels are required, please contact Logic for reference designs. UARTB includes a Serial InfraRed (SIR) ENDEC (Encoder/Decoder), and is capable of generating two interrupts not available from UARTA or the SPI.

2.7.1 UARTA

UARTA has been configured to be the LH79520 main serial port. It is an asynchronous 16C550 compatible UART. This SCIF interface is a high-speed serial interface with a FIFO (asynchronous or synchronous) and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Zoom™ Starter Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2K bits/sec, though it supports all common serial baud rates from 110bps to 460.8K bits/sec. UART A is available off the 144-pin SO-DIMM connector. Please see the LH79520 Universal Microcontroller User's Guide for further information.

2.7.2 UARTB

Serial Port UARTB has dual functionality, its primary function is as an asynchronous 16C550 compatible UART. This SCIF interface is also a high-speed serial interface with a FIFO (asynchronous or synchronous) and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTB's baud rate can also be set to all common serial baud rates from 110bps to 460.8K bits/sec.

UARTB's secondary function is as an IrDA-compatible Serial InfraRed (SIR) Encoder/Decoder (ENDEC) block that supports serial infrared communications. The SIR ENDEC can be enabled for serial IR communication through pins uP_UARTB_TX - IR and uP_UARTB_RX - IR. The SIR ENDEC is half-duplex only, so it cannot receive while transmitting, or transmit while receiving. UART B/IrDA port is available off one of the 80 pin expansion connectors. Please see the LH79520 Universal Microcontroller User's Guide for further information.

2.7.3 SPI

The SPI interface on the LH79520 is a SSP (synchronous serial port) used to facilitate synchronous serial communications with slave peripheral devices. This serial port is a Master-only device, with programmable clock bit-rate and prescale factors. It supports three data frame formats:

- Texas Instruments' SSI
- Motorola SPI™
- National Semiconductor Microwire™

The SPI interface signals are available off the 144-pin SO-DIMM connector. Please see the LH79520 Universal Microcontroller User's Guide for further information.

2.8 Touch Interface

Touch interface is supported on the LH79520-10 Card Engine for standard 4-wire resistive touch panels. The LH79520-10 Card Engine implements the popular TI ADS7843 12-bit sampling ADC touch controller. See the ADS7843 specification for more detailed information. The touch controller interfaces to the LH79520 microcontroller through the IO Controller, which provides a parallel to SPI interface. Why not use the SPI interface provided on the LH79520 microcontroller? Many of Logic's customers use the on-chip (microcontroller) SPI port for their applications, therefore Logic designs their Card Engines to keep the serial channels free for user applications.

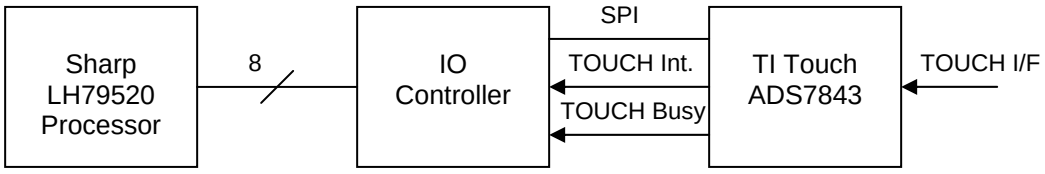


Figure 2.3: Touch Controller Block Diagram

The IO Controller Interface Specification provides the necessary information to interface to the touch controller. Please see the LH79520-10 Card Engine IO Controller Interface Specification for more information.

2.9 General Purpose Analog & Digital I/O

Logic designed the LH79520-10 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO on the Card Engine that interface to the LH79520, and the IO Controller. Some of these GPIO are interrupt capable while other signals are input or output only. Please see the Pin Descriptions section of this data sheet. The LH79520 microcontroller does not contain an internal Analog to Digital Converter (ADC), however, the ADS7843 Touch Chip (U12) provides 2 analog inputs available to the user. The IO Controller Interface Specification provides a user with the necessary information to interface to the touch controller. Please see the IO Controller Interface Specification for more information. If certain peripherals are not used, such as the LCD Controller, Chip Selects, IRQs, UARTs, or SPI port multiple GPIO pins become available. Please see the table in section 5 entitled "Multiplexed Signal Trade-Offs." This table lists the available GPIO trade-offs that are available when certain peripheral functions are not used.

2.10 IO Controller

Please see the LH79520-10 Card Engine IO Controller Interface Specification for more information.

2.11 Serial EEPROM Interface

Logic designed the LH79520-10 Card Engine to have a low cost 1 kbit serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the LH79520 microcontroller via the IO Controller through an SPI interface. See Figure 2.4 below. Please see the LH79520-10 Card Engine IO Controller Interface Specification for more information.

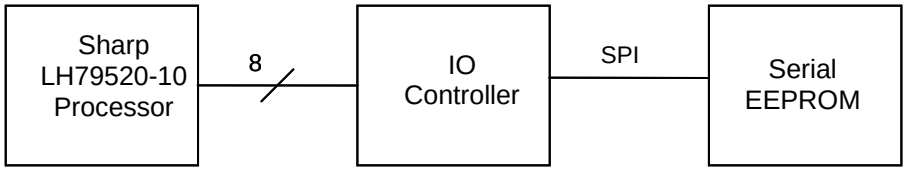


Figure 2.4: Serial EEPROM Block Diagram

2.12 Expansion Options

The LH79520-10 Card Engine was designed for expansion and provides all the necessary control signals and bus signals to expand the user's design. Many of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80 pin expansion connectors. See the LH79520-10 Card Engine schematics for more detail. A user can expand the Card Engine's functionality such as PCI, CompactFlash, PCMCIA, ISA devices, PCI devices, etc.. Logic has expanded the Card Engine to other audio CODECs, Ethernet IC's, UARTs, Co-processors, etc. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The LH79520-10 Card Engine was designed to be configurable to meet user's applications and budget needs. The Card Engine supports a variety of embedded operating systems and comes in the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64 Mbytes Synchronous DRAM
- Flexible flash footprint: 8 or 16 Mbytes StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional TI TLV320DAC23GQE Audio CODEC
- Optional Touch Controller

Please contact Logic for additional hardware configurations to meet your application.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

Any microcontroller or peripheral having a hardware-reset signal is reset by the MSTR_nRST or RESET_HIGH signal. MSTR_nRST should be the "pin hole" reset used for commercial embedded systems implemented with the LH79520-10 Card Engine. If MSTR_nRST is asserted, the user can expect to lose information stored in SDRAM.

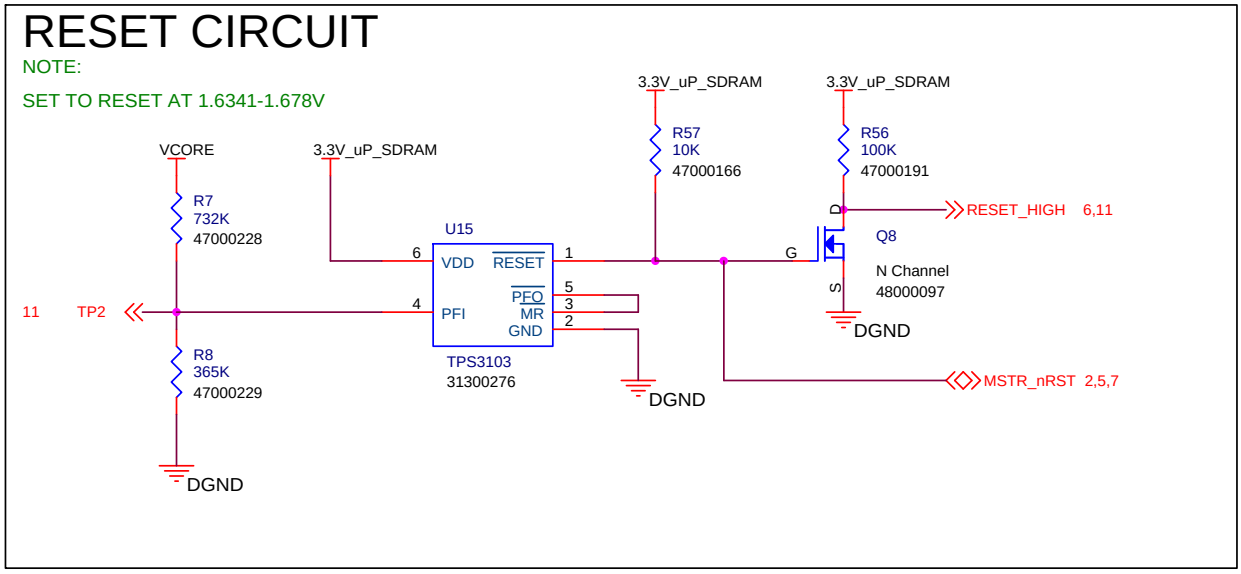


Figure 3.1: Reset Circuit

The MSTR_nRST signal is an active low output of the reset chip, located on the card engine. The RESET_HIGH signal is an active high signal.

IMPORTANT NOTE: The user should guard the assertion of the reset lines during a low power state so the microcontroller cannot be reset and powered up with bad power (will cause data corruption and possible temporary system lockup). See section entitled "Power Management" for further details.The timing diagrams for the reset chip are shown in Figure 3.2.

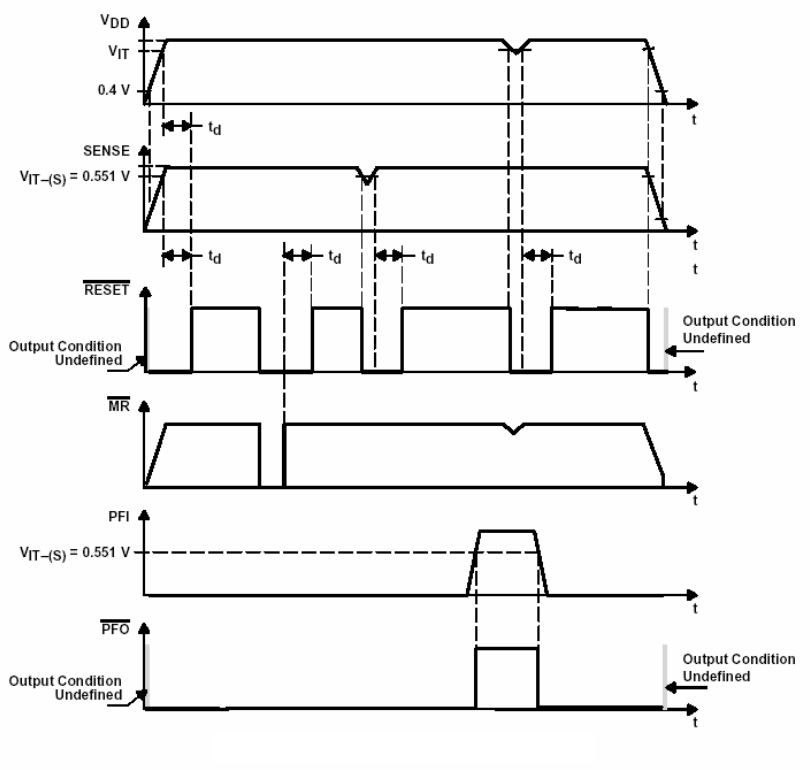


Figure 3.2: Reset IC Timing Diagram

There are three conditions that will generate a low on the output reset pin of the reset chip (the MSTR_nRST signal): power-on condition, a low pulse on the MSTR_nRST signal, and the power fail comparator input (PFI pin) falling below the internal comparator threshold.

Power On:
At power on, MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip becomes higher than 1.1V. Once VDD signal becomes higher than 2.93V, an internal timer will delay the rising edge of MSTR_nRST for 200 ms (typical).

Low Pulse on MSTR_RST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by a push button located on the application board, will bring MSTR_nRST low. MSTR_nRST will return high as soon as it is deasserted offboard.

Power Fail:
If the power fail comparator input pin (PFI pin) falls below the internal comparator threshold of 1.25V, it will create a low pulse on the MR input pin of the reset chip (after a delay of 0.5 uS). The MSTR_nRST pin will then follow the above stated procedure for a low pulse on the MR pin.

IMPORTANT NOTE: It is critical that a user is careful in selecting cross-parts for the reset IC. The current reset chip in the BOM has an open drain output for output pin RESET. Other cross-parts may not have an open drain on this pin and will fail when MSTR_nRST signal is asserted to GND.

3.2.2 Soft Reset

Logic has created a soft reset signal named uP_SW_nRESET that can be used to reset the LH79520 internal registers, without affecting the peripherals on the rest of the board and without losing data stored in SDRAM or other volatile storage. The uP_SW_nRESET signal is an input to

the IO Controller. When a low pulse is detected, the IO Controller generates an interrupt to the microcontroller. The microcontroller then reads the interrupt/mask register of the IO Controller, which indicates a soft reset has been administered.

3.3 Interrupts

The LH79520 responds to ARM exceptions and vectored interrupts generated by the onboard-vectored interrupt controller (VIC). The LH79520 accepts inputs from 32 interrupt sources--24 are from internal sources, and 8 are from external sources. All interrupts are routed to the VIC where priorities are determined by hardware and the appropriate interrupt signal is dispatched to the ARM720T exception-handling hardware. Lower numbered interrupts have higher priority than higher-numbered interrupts. Each external interrupt has rising edge, falling edge, HIGH level, or LOW-level trigger options. The LH79520-10 Card Engine interrupts are set to trigger on a LOW level by default. The LH79520-10 Card Engine provides 7 available interrupt sources. Each of the interrupts can be separately setup as FIQs via software. Refer to Sharp's LH79520 Universal Microcontroller User's Guide for further information.

LPD Signal	LH79520 Signal	External User Availability	Default Use
uP_NMI	INT0	Available	
uP_IRQA	INT1	Available	
uP_IRQB	INT2	Available	
uP_IRQC	INT3	Available	
uP_IRQ4	INT4	Not Available	Onboard IO Controller (U11)
uP_nWAIT	INT5	Available if uP_WAIT# is not used	Onboard Ethernet (U10)
G4	INT6	Available if LCD signal is not used	Offboard LCD Display
G5	INT7	Available if LCD signal is not used	Offboard LCD Display

IMPORTANT NOTE: See LH79520-10 Card Engine IO Controller Interface Specification for detailed information on the use of the uP_IRQ4 interrupt.

3.4 JTAG Debugger Interface

There are many different third party JTAG debuggers available for Sharp ARM microcontrollers. The JTAG connection enables a user to recover a board that has corrupted flash memory and to debug real time applications. The following signals make up the JTAG interface to the LH79520, for connection to an JTAG emulator: uP_TRST, uP_TDI, uP_TMS, uP_TCK, uP_TDO. These signals should interface directly to a 20-pin or 14-pin 0.1" through-hole connector as demonstrated in the Sharp LH79520 Universal Microcontroller User's Guide, or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20-pin or 14-pin connector out, realize it may not be numbered as a standard 20-pin or 14-pin 0.1" IDC through-hole connector. See LH79520-10 Card Engine Application Kit reference design for further details. Different IC manufacturers define the 20-pin or 14-pin IDC connector pin-out differently.

3.5 Power Management

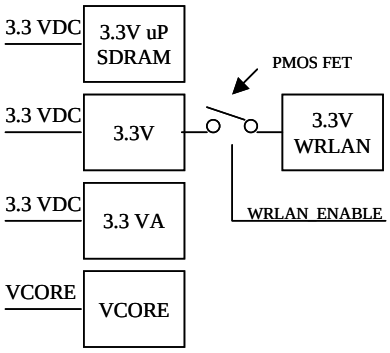
3.5.1 System Power Management

Good power management design happens in the hardware and software of any system. Typically, the power management design of any embedded system can be one of the most complicated parts and has a dramatic effect on the overall product cost, performance, usability, and customer satisfaction. Many factors effect good power management design in the hardware including: power supply selection (efficiency), clocking design, IC and component selection, etc.

The LH79520-10 Card Engine electronics were designed to provide maximum flexibility to the software and system integrator.

There are many different software configurations which drastically effect the power consumption of the LH79520-10 Card Engine including: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes (asynchronous, synchronous, FastBus), microcontroller power management states (active, standby, sleep, stop1, stop2), peripheral power states and modes, product user scenarios, interrupt handling, display settings (resolution, backlight, refresh, bits per pixel, etc..) These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. These items are covered in the appropriate documents such as the LogicLoader™ User's Manual or appropriate BSP manual.

The LH79520-10 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, and VCORE for a flexible hardware design. See Figure 3.3 below.



Logic Net Name	Required Input VDC	Notes
3.3V_uP_SDRAM	3.3 VDC	Connects to the processor 3.3 volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and SDRAM to refresh.
3.3V	3.3 VDC	Connects to the digital peripherals on the Card Engine
3.3VA	3.3 VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may chose not to provide a clean analog plane depending on their audio performance requirements.
3.3V_WRLAN	NA	The 3.3V_WRLAN is located on the Card Engine only and provides power the the SMSC 91C111 processor. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the CPLD Interface Specification for controlling the WRLAN_E
VCORE	See Note	Connects to the processor core voltage. See specific processor for VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperature,etc..

Figure 3.3: Power Plane Diagram

IMPORTANT NOTE: The purpose of the PMOS FET to control the power to the SMSC 91C111 is because the software power management in the 91C111 is not suitable for many applications.

IMPORTANT NOTE: The 3.3V_WRLAN signal is an output from the card engine and is used to power off board Wired Lan related circuitry. Typically this signal is used to power Activity and Link status LEDs.

IMPORTANT NOTE: The LH79520-10 Card Engine hardware architecture was designed for low power battery operated applications. However, the Altera CPLD on the LH79520-10 Card Engine is not an ideal part for low power battery operated designs. This specific component was chosen for cost. If one is using the LH79520-10 Card Engine as a reference design, one can consider other programmable logic devices that are optimized for power, not cost.

3.5.2 Peripherals

Most peripherals provide software programmable power states. The audio CODEC and touch controller have programmable power states. Please see the appropriate data sheet for more information and the IO Controller Interface Specification for details. The SMSC 91C111 controller has software programmable power states but may not be sufficient for some applications. Logic has provided hardware to cut power to the 91C111 IC.

3.5.3 Microcontroller

The LH79520-10 Card Engine power management's scheme was designed to be easy to use. There are five power management states provided in the LH79520 microcontroller: ACTIVE, STANDBY, SLEEP, STOP1, and STOP2. Sharp's LH79520 provides complex power management features. Please see the LH79520 Universal Microcontroller User's Guide for more details.

IMPORTANT NOTE: The BSPs available from Logic for the different operating systems supported on the LH79520 may not support all five of the power management states. Please see the appropriate BSP documentation for power management modes for more detail.

3.5.3.1 Active Mode

The LH79520-10 Card Engine normal operating state is ACTIVE. The LH79520 system on a chip enters this mode on reset and returns to this mode when any interrupt is received, if operating in any other power mode. The LH79520 cannot transition directly between the other power modes; it will always return to active mode before entering any other power mode.

3.5.3.2 Standby Mode

The Standby mode halts the clocks to the CPU while leaving the remainder of the chip active. The LH79520 transitions from the Standby mode to the Active mode when an interrupt is received.

3.5.3.3 Sleep Mode

The Sleep mode halts all system clocks. Only the PLL and the internal oscillators remain active. If the 32.768 kHz internal oscillator is in use, it will also remain active. The LH79520 transitions from the Sleep mode to the Active mode when an interrupt is received.

When transitioning from the Active mode to the Sleep mode, the LH7920 Power Management system automatically performs the following sequence:

- Acquires control of the AHB, to ensure that all transactions are completed.
- Ensures that all SDRAM devices are placed in the self-refresh mode of operation.
- Halts all output clocks that are driven by HCLK, HCLK_CPU, and PCLK
- Waits for IRQ or FIQ to be asserted (which will return the LH79520 to the Active mode).

When an IRQ or FIQ occurs, the LH79520 returns to the Active mode, restarts the output clocks, resumes SDRAM refresh and then cedes control of the AHB.

3.5.3.4 Stop1 Mode

The Stop1 mode halts all system clocks and disables the PLL but keeps the internal oscillators active. If the 32.768 kHz internal oscillator is in use, it will remain active. The LH79520 transitions from the Stop1 mode to the Active mode when an interrupt is received.
When transitioning from the Active mode to the Stop1 mode, the LH79520 Power Management system automatically performs the following sequence:

- Acquire control of the AHB, to ensure that all transactions are completed.
- Ensure that all SDRAM devices are placed in the self-refresh mode of operation.
- Halts all clocks, disable the PLL and deassert the CLKEN output signal.
- Wait for IRQ or FIQ to be asserted (which will return the LH79520 to the Active mode).

When an IRQ or FIQ occurs, the LH79520 returns to the Active mode, restarts the output clocks (which may require a delay for the PLL to reacquire lock, if the PLL is in use), resumes SDRAM refresh and then cedes control of the AHB.

3.5.3.5 Stop2 Mode

The Stop2 mode halts all system clocks and disables both the PLL and the internal oscillators that feed it. If the 32.768 kHz internal oscillator is in use, it will remain active. The LH79520 transitions from the Stop2 mode to the Active mode when an interrupt is received.

When transitioning from the Active mode to the Stop2 mode, the LH79520 Power Management system automatically performs the following sequence:

- Acquire control of the AHB, to ensure that all transactions are completed.
- Ensure that all SDRAM devices are placed in the self-refresh mode of operation.
- Halts all clocks, disable the PLL, disable the 14.7456 MHz oscillator, and de-assert the CLKEN output signal.
- Wait for IRQ or FIQ to be asserted (which will return the LH79520 to the Active mode).

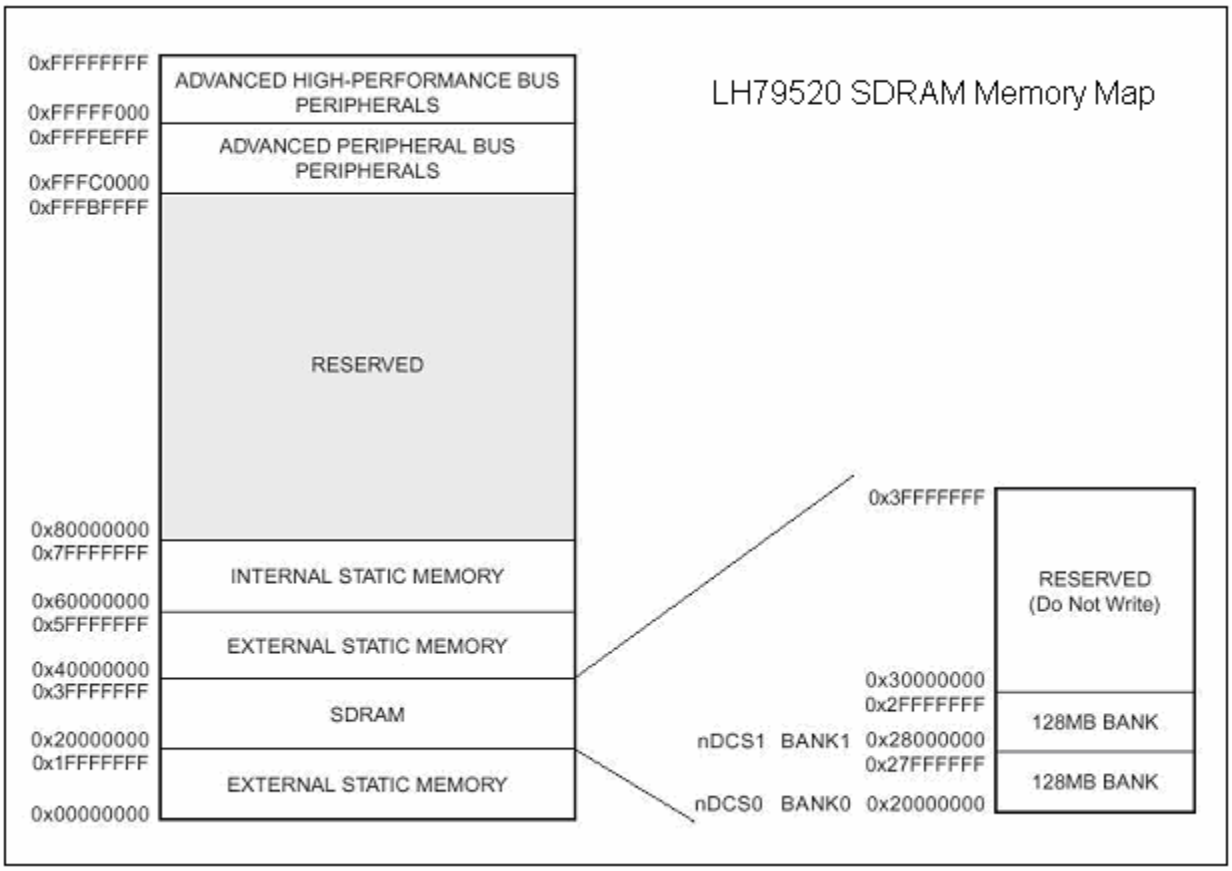
When an IRQ or FIQ occurs, the LH79520 returns to the Active mode, restarts the output clocks (which may require a delay for the PLL to reacquire lock, if the PLL is in use), resumes SDRAM refresh and then cedes control of the AHB.

3.6 ESD Considerations

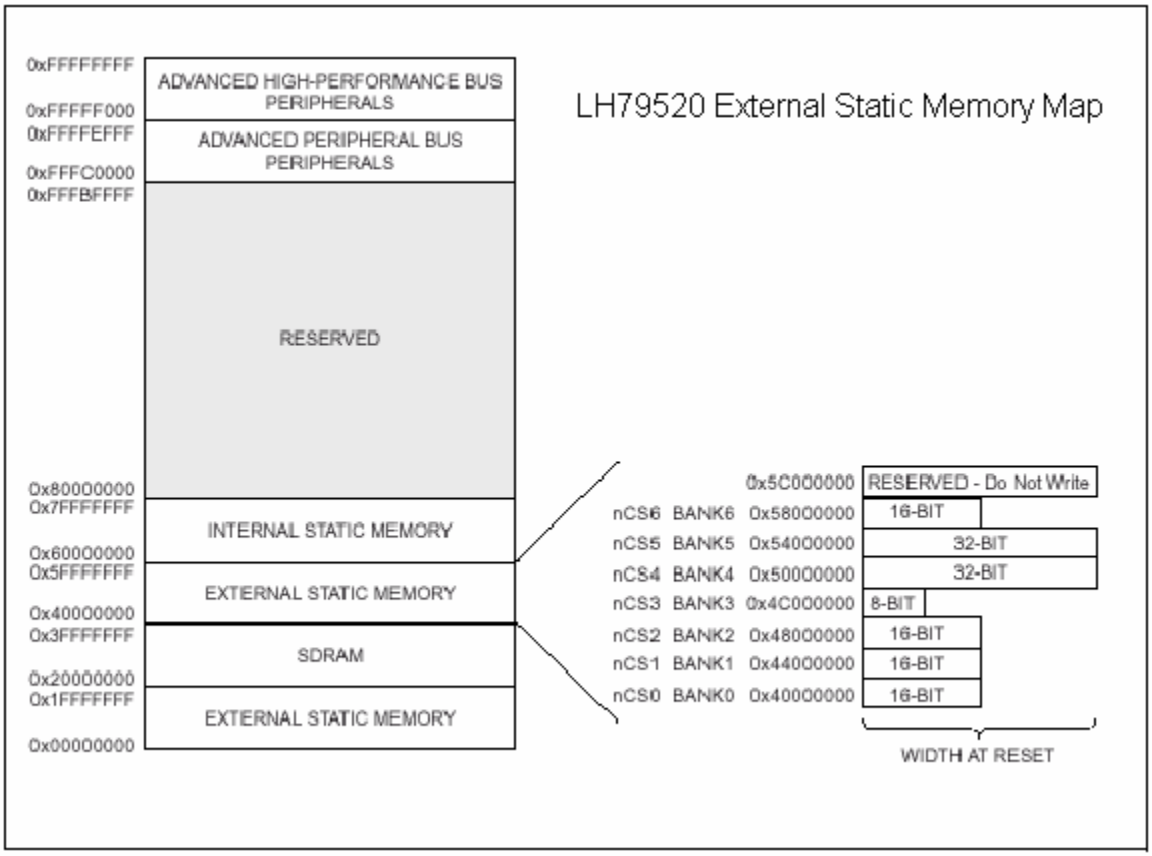
The LH79520-10 Card Engine was designed to interface to a customer's peripheral board. The Card Engine was designed to be low cost and adaptable to many different applications. The LH79520-10 Card Engine does not provide any ESD protection circuitry on the card and must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SDRAM Memory Map



4.2 External Static Memory Map



4.2.1 Card Engine Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the card engine.

Chip Select	Bank	Start Address	Memory Description
nCS6	6	0x5800 0000	N/A[1]
nCS5	5	0x5400 0000	IO Controller Peripherals (fast[2])
nCS4	4	0x5000 0000	IO Controller Peripherals (slow[2])
nCS3	3	0x4C00 0000	Boot Device (flash or EEPROM[3])
nCS2	2	0x4800 0000	open
nCS1	1	0x4400 0000	Video[3]
nCS0	0	0x4000 0000	Boot Device (flash or EEPROM[3])

Notes:
1. Pin nCS6 is used as an alternate pin function.
2. IO Controller peripherals are those components that get a decoded chip select from the IO Controller. (i.e. CPLD memory mapped registers, onboard SMSC 91C111 Ethernet controller, etc... Please see the LH79520-10 IO Controller Specification document for details.) These

peripherals are separated into two different chip select banks, due to difference in timing: slow and fast.
3. Components planned for future applications.

4.2.2 Chip Select 4 (nCS4) – IO Controller Peripherals (slow timing)

The table below indicates how the IO Controller decodes chip select 4. For more detailed information see the IO Controller Interface Specification.

Chip Select	Address Range	Memory Description	Size
nCS4	0x5000 0000 – 0x501F FFFF	open	2MB
nCS4	0x5020 0000 – 0x503F FFFF	CF Chip Select	2MB
nCS4	0x5040 0000 – 0x505F FFFF	ISA-like Bus Chip Select	2MB
nCS4	0x5060 0000 – 0x51FF FFFF	open	2MB (X13)
nCS4	0x5200 0000 – 0x53FF FFFF	reserved	1MB (X32)

4.2.3 Chip Select 5 (nCS5) – IO Controller Peripherals (fast timing)

The table below indicates how the IO Controller decodes chip select 5. For more detailed information see the IO Controller Interface Specification.

Chip Select	Address Range	Mem Block Description	Size
nCS5	0x5400 0000 – 0x541F FFFF	Wired LAN Chip Select	2MB
nCS5	0x5420 0000 – 0x543F FFFF	Wired LAN Control Reg	2MB
nCS5	0x5440 0000 – 0x545F FFFF	CODEC I2S Audio	2MB
nCS5	0x5460 0000 – 0x547F FFFF	SPI Data Reg	2MB
nCS5	0x5480 0000 – 0x549F FFFF	SPI Control Reg	2MB
nCS5	0x54A0 0000 – 0x54BF FFFF	EEPROM SPI Reg	2MB
nCS5	0x54C0 0000 – 0x54DF FFFF	Interrupt/Mask Reg	2MB
nCS5	0x54E0 0000 – 0x54FF FFFF	Mode Reg	2MB
nCS5	0x5500 0000 – 0x551F FFFF	Flash Reg	2MB
nCS5	0x5520 0000 – 0x553F FFFF	SDRAM Reg	2MB
nCS5	0x5540 0000 – 0x555F FFFF	IO Controller Revision Reg	2MB
nCS5	0x5560 0000 – 0x557F FFFF	Extended GPIO Reg	2MB
nCS5	0x5580 0000 – 0x55FF FFFF	open	2MB (X5)
nCS5	0x5600 0000 – 0x57FF FFFF	reserved	1MB (X32)

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the card engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines.
2	MSTR_nRST	I/O	This signal initiates a hard reset – external memory contents are lost during reset. This signal is active low. A low on this signal resets the Card Engine. This signal has a 10k pull up located on the Card Engine.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines.
4	uP_SW_nRESET	I	This signal initiates a soft reset – external memory contents are retained during reset. This signal is active low. The uP_SW_RESET signal is an input to the IO Controller. When a low pulse is detected, the IO Controller generates an interrupt to the microcontroller. The microcontroller then reads the interrupt/mask register of the IO Controller, which indicates a soft reset has been administered. See the IO Controller Interface Specification. This signal has a 10k pull up located on the Card Engine.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines.
6	FAST_nMCS	O	Chip select for area 5 of LH79520 memory.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines.
8	SLOW_nMCS	O	Chip select for area 4 of LH79520 memory.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nMCS	O	Chip select for area 1 of LH79520 memory (active low).
11	ETHER_nACT_LED	O	This output indicates transmission or reception of frames or detection of a collision. This signal may be connected to an external LED.
12	BOOT_nMCS	O	This signal is the chip select for boot ROM.
13	ETHER_nLNK_LED	O	This output indicates valid link pulses. May be connected to an external LED.
14	nIOWR	O	This signal is driven by the ISA bus master or DMA controller to request an I/O resource to accept data from data lines.
15	nSTANDBY	I	CPU power mode signal. This signal is connected to the LH79520 on pin #99 (PF1/CLKEN). This signal has a 10k pull up located on the Card Engine.
16	nIORD	O	This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	I	This pin outputs power for use with external Wired Lan circuitry. Please refer to Logic Product Development SDK and IDK kits for reference designs for Wired Lan connector implementations. Typically this power output would be used to supply power to the Wired Lan Activity and Link LEDs.
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	This signal is driven to a logical one to indicate when the MA<19:0> signal lines are valid.

Pin #	Signal Name	I/O	Description
21	uP_NMI	I	The NMI (non-maskable interrupt – highest priority) and IRQ[3:0] signals generate a request to the CPU for service (interrupt service routine). The NMI signal is active low. The uP_NMI has a 10k pull up located on the Card Engine.
22	nCHRDY	I	The I/O channel ready signal line allows the resources to indicate to the ISA bus master that additional cycle time is required. This signal has a 1k pull up located on the Card Engine.
23		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
24	uP_TEST1	I	Reserved for Production Test: This signal is tied low internally by the processor. No external connection is necessary. LOW indicates NORMAL operation.
25	uP_IRQC	I	Hardware interrupt on LH79520 (active low). Optionally configured as LH79520 general-purpose input. The uP_IRQC signal has a 10k pull up located on the Card Engine.
26	uP_TEST2	I	Reserved for Production Test: This signal is tied low in the processor. LOW indicates NORMAL operation, pull up to enable the use of a JTAG emulator.
27	uP_IRQB	I	Hardware interrupt on LH79520 (active low). Optionally configured as LH79520 general-purpose input. The uP_IRQB signal has a 10k pull up located on the Card Engine.
28	uP_nTRST	I	JTAG Test Reset Input. This signal has a 10k pull up located on the card engine.
29	uP_IRQA	I	Hardware interrupt on LH79520 (active low). Optionally configured as LH79520 general-purpose input. The uP_IRQA signal has a 10k pull up located on the Card Engine.
30	uP_TMS	I	JTAG Test Mode Select Input. This signal has a 10k pull up located on the card engine.
31		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
32	uP_TDO	O	JTAG Test Data Serial Output. This signal has a 10k pull up located on the card engine.
33		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
34	uP_TDI	I	JTAG Test Serial Data Input. This signal has a 10k pull up located on the card engine.
35		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
36	uP_TCK	I	JTAG Test Clock Input. This signal has a 10k pull up located on the card engine.
37	uP_nWAIT	I	The WAIT signal requests the current bus cycle be extended by one or more wait states (active low). The uP_nWAIT signal has a 10k pull up located on the Card Engine.
38	uP_MODE3	I	Boot select signal (0 = external boot PROM, 1 = onboard flash) This signal has a 10k pull up located on the Card Engine.
39		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
40	uP_MODE2	I	This signal has a 10k pull up located on the Card Engine.
41		NC	No internal connection. DO NOT TIE TO GND. LEAVE FLOATING.
42	uP_MODE1	I	This signal has a 10k pull up located on the Card Engine.
43	uP_UARTA_TX - PA4	O	Transmitter serial data output.
44	uP_MODE0	I	This signal has a 10k pull up located on the Card Engine.
45	uP_UARTA_RX - PA3	I	Receiver serial data input. This signal has a 10k pull up located on the Card Engine.
46		NC	No internal connection.
47		NC	No internal connection.
48		NC	No internal connection.
49		NC	No internal connection.
50		NC	No internal connection.

Pin #	Signal Name	I/O	Description
51	nSUSPEND	I	CPU power mode signal. This signal is connected to the LH79520 on pin #99 (PH5/nCS6) This signal has a 10k pull up located on the Card Engine.
52		NC	No internal connection.
53	uP_AUX_CLK	O	This auxiliary clock is controlled in the CPU and can be used by the peripherals.
54	uP_DACK1	O	This handshake signal is output by the CPU to acknowledge DMA requests.
55	DGND	I	Digital Ground (0V)
56		NC	No internal connection.
57	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
58	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
59	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
60	VCORE	I	CPU core voltage supply (on during low power, SW_Reset).
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset)
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset)
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset)
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset)
65	uP_SPI_FRM	O	Serial Frame Output.
66	uP_BUS_CLK	O	51.6 MHz clock.
67	uP_SPI_MOSI_TX	O	This output transmits SPI data.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_MISO_RX	I	This input receives SPI data. This signal has a 10k pull up located on the Card Engine.
70	uP_nRAS	I/O	This signal is sent to a random access memory to tell that an associated address is a row address.
71	uP_SPI_SCK	O	SPI transmit/receive data is shifted/sampled on the rising or falling edge of this clock.
72	uP_nCAS	I/O	This signal is sent to a random access memory to tell that an associated address is a column address.
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74		NC	No internal connection.
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2	O	Buffered data bus bits 23-16 Byte lane enable (active low output)signal from the LH79520.
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMWE1	O	Buffered data bus bits 15-8 Byte lane enable (active low output) signal from the LH79520.
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0	O	Buffered data bus bits 7-0 Byte lane enable (active low output) signal from the LH79520.
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	When asserted, the write signal instructs an I/O device to store the data present on the data bus, during a write instruction.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	The read signal instructs an I/O device to drive its data onto the data bus.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection.
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection.
89	DGND	I	Digital Ground (0V)
90	uP_MA0	I/O	Buffered Address Bus bit 0.

Pin #	Signal Name	I/O	Description
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	I/O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	I/O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	I/O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	I/O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	I/O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	I/O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	I/O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	I/O	Buffered Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)
108	uP_MA9	I/O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	I/O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	I/O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	I/O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.
116	uP_MA13	I/O	Buffered Address Bus bit 13.
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	I/O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	I/O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	I/O	Buffered Address Bus bit 16.
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	I/O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	I/O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	I/O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	I/O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	I/O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	I/O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.
136	uP_MA23	I/O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	I/O	Buffered Address Bus bit 24.

Pin #	Signal Name	I/O	Description
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	I/O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Address Enable, this ISA signal is used to degate the uP and other devices from the bus during DMA transfers.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC - SPS	O	Vertical synchronization pulse for TFT displays. / LCD reset signal for row display on HR-TFT displays.
2	LCD_HSYNC - LP	O	Horizontal synchronization pulse for TFT displays. / LCD line synchronization pulse for STN displays.
3	LCD_DCLK	O	LCD data clock.
4		NC	No internal connection.
5	LCD_MDISP - SPL - PC0	O	LCD Display Enable signal. / LCD Line Start Pulse.
6		NC	No internal connection.
7	LCD_CLS - VDDEN - PC1	O	LCD clock signal for gate driver / LCD digital supply enable.
8	LCD_CLK_RETURN	I	High Resolution clock input. This signal has a 10k pull down located on the Card Engine.
9	DGND	I	Digital Ground (0V)
10	LCD_CLS - VDDEN - PC1	O	LCD clock signal for gate driver / LCD digital supply enable.
11	LCD_VSYNC – SPS	O	Vertical synchronization pulse for TFT displays. / LCD reset signal for row display on HR-TFT displays.
12	G0	O	High Resolution Rev (AC bias) Signal.
13	LCD_MDISP - SPL - PC0	O	LCD Display Enable signal. / LCD Line Start Pulse.
14	LCD_HSYNC - LP	O	Horizontal synchronization pulse for TFT displays. / LCD line synchronization pulse for STN displays.
15		NC	No internal connection.
16	B0	O	High Resolution Power Save Signal.
17	Up_STATUS_1	O	Status Pin.
18	UP_STATUS_2	O	Status Pin
19		NC	No internal connection.
20		NC	No internal connection.
21		NC	No internal connection.
22		NC	No internal connection.
23		NC	No internal connection.
24	DGND	I	Digital Ground (0V)
25	A/D1	I	This can be programmed as an auxiliary ADC input on the touch controller. If not used, tie to GND w/ 10k pull down.
26	A/D2	I	This can be programmed as an auxiliary ADC input on the touch controller. If not used, tie to GND w/ 10k pull down.
27	AGND	I	Analog Ground (0V)
28	HP_OUTL	O	Left stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1.0 Vrms. Gain of -73dB to 6dB is provided in 1-dB steps.
29	HP_OUTR	O	Right stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1.0 Vrms. Gain of -73dB to 6dB is provided in 1-dB steps.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo-line in input of the audio CODEC. If not used, tie to GND w/ 10k pull down.
32	CODEC_INR	I	Right channel stereo-line in input of the audio CODEC. If not used, tie to GND w/ 10k pull down.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Nominal output level is 1.0 Vrms.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Nominal output level is 1.0 Vrms.

Pin #	Signal Name	I/O	Description
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	Y+ Position Input. If not used, tie to GND w/ 10k pull down. This signal has a .01uF capacitor tied to ground.
37	TOUCH_RIGHT	I	Y- Position Input. If not used, tie to GND w/ 10k pull down. This signal has a .01uF capacitor tied to ground.
38	TOUCHX_BOTTOM	I	X+ Position Input. If not used, tie to GND w/ 10k pull down. This signal has a .01uF capacitor tied to ground.
39	TOUCH_TOP	I	X- Position Input. If not used, tie to GND w/ 10k pull down. This signal has a .01uF capacitor tied to ground.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. RED 0. This is an intensity bit.
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5.
48	R0	O	The LCD data bus used to transmit data to the LCD module. GREEN 0. This is an intensity bit.
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5
54	R0	O	The LCD data bus used to transmit data to the LCD module. BLUE 0. This is an intensity bit.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5.
61	CF_nCE	O	This signal is used to select the CF card and indicates a word operation to the CF storage card.
62	RSVD_1	I	This pin is a no connect, but is kept as reserved. This signal has a 10k pull up located on the Card Engine.
63	CPLD_GPIO_1	O	This signal is a general-purpose output it is controlled by a memory mapped address in the IO Controller. See IO Controller Interface Specification.
64		NC	No internal connection.
65		NC	No internal connection.
66	DGND	I	Digital Ground (0V)
67		NC	No internal connection.
68		NC	No internal connection.
69		NC	No internal connection.

Pin #	Signal Name	I/O	Description
70		NC	No internal connection.
71		NC	No internal connection.
72		NC	No internal connection.
73		NC	No internal connection.
74	BUFF_nOE	O	Controls the outputs of the buffers present on the Card Engine, the states are active or tri-state.
75	BUFF_DIR_ADDRESS	O	Controls the direction of the address lines through the buffers.
76	BUFF_DIR_DATA	O	Controls the direction of the data through the buffers.
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection.
79	POWER_SENSE1	I	These two pins are used to set the core voltage of the Card Engine. For use with Logic Application Boards only.
80	POWER_SENSE2	I	These two pins are used to set the core voltage of the Card Engine. For use with Logic Application Boards only.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the JTAG device. This signal has a 10k pull down located on the Card Engine.
2	CPLD_TDO	O	This output transmits data out of the JTAG device. This signal has a 10k pull up located on the Card Engine.
3	CPLD_TMS	I	This input indicates the mode of JTAG device. This signal has a 10k pull up located on the Card Engine.
4	CPLD_TDI	I	This input receives data on the JTAG device. This signal has a 10k pull up located on the Card Engine.
5		NC	No internal connection.
6		NC	No internal connection.
7		NC	No internal connection.
8		NC	No internal connection.
9	DGND	I	Digital Ground (0V)
10		NC	No internal connection.
11		NC	No internal connection.
12		NC	No internal connection.
13		NC	No internal connection.
14		NC	No internal connection.
15		NC	No internal connection.
16		NC	No internal connection.
17		NC	No internal connection.
18		NC	No internal connection.
19		NC	No internal connection.
20		NC	No internal connection.
21	DGND	I	Digital Ground (0V)
22		NC	No internal connection.
23		NC	No internal connection.
24		NC	No internal connection.
25		NC	No internal connection.
26	uP_nDQM3	O	Data mask output to SDRAM.
27	uP_nDQM2	O	Data mask output to SDRAM.
28	uP_nDQM1	O	Data mask output to SDRAM.
29	uP_nDQM0	O	Data mask output to SDRAM.
30	UP_UARTB_TX - IR	O	UARTB Transmitted serial data input / UARTB Infrared Transmit.
31	UP_UARTB_RX - IR	I	UARTB Received serial data input / UARTB Infrared Receive. This signal has a 10k pull up located on the Card Engine.
32	DGND	I	Digital Ground (0V)
33		NC	No internal connection.
34		NC	No internal connection.
35		NC	No internal connection.
36		NC	No internal connection.
37		NC	No internal connection.
38		NC	No internal connection.
39		NC	No internal connection.
40		NC	No internal connection.
41	UP_UARTB_TX - IR	O	UARTB Transmitted serial data input / UARTB Infrared Transmit.

Pin #	Signal Name	I/O	Description
42	uP_UARTB_RX - IR	I	UARTB Received serial data input / UARTB Infrared Receive. This signal has a 10k pull up located on the Card Engine.
43		NC	No internal connection.
44	DGND	I	Digital Ground (0V)
45		NC	No internal connection.
46		NC	No internal connection.
47		NC	No internal connection.
48	MFP9 - CLKIN/UARTCLK	I	External Clock Input (if CLKINSEL = high at reset) This signal has a 10k pull up located on the Card Engine.
49	MFP10 - CLKINSEL	I	External Clock Select. This signal has a 10k pull down located on the Card Engine. The processor also has an internal pull down. The card engine derives its clock from the 14.7456 crystal onboard when this signal is LOW.
50		NC	No internal connection.
51		NC	No internal connection.
52		NC	No internal connection.
53		NC	No internal connection.
54		NC	No internal connection.
55	DGND	I	Digital Ground (0V)
56		NC	No internal connection.
57		NC	No internal connection.
58		NC	No internal connection.
59		NC	No internal connection.
60		NC	No internal connection.
61		NC	No internal connection.
62	MFP22 - PWM1/DEOT1	O	PWM Output
63	MFP23 – CPLD_GPI_3	O	This signal is a general-purpose input. This signal has a 10K pull up.
64		NC	No internal connection.
65		NC	No internal connection.
66	DGND	I	Digital Ground (0V)
67	MFP26 - uP_PH7	I	Port H bit 7
68	MFP27 - uP_MCS2	O	Chip select for area 2 of LH79520 memory
69	MFP28 – nTSTA	O	Reserved for production test.
70	MFP29 - SDCKE	O	SDRAM Clock Enable
71	MFP30 - uP_nSDWE	O	SDRAM Write Enable.
72	MFP31 - uP_nMCS3	O	Chip select for area 3 of LH79520 memory.
73	MFP32 - nRESETOUT	O	Reset Output
74		NC	No internal connection.
75	MFP34 - CODEC_CLKOUT	O	CODEC Clock Output
76		NC	No internal connection.
77	DGND	I	Digital Ground (0V)
78		NC	No internal connection.
79		NC	No internal connection.
80		NC	This signal has a 10k pull down. It is reserved for the RTCK signal out of card engines requiring RTCK for JTAG interfacing.

5.4 Multiplexed Signal Trade-Offs

5.4.1 J1C Connector SODIMM 144-Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
6	FAST_nMCS	nCS5	Chip Select 5 Output	PH7	Port H bit 7 Output Only
8	SLOW_nMCS	nCS4	Chip Select 4 Output	PH3	Port H bit 3 Output Only
15	nSTANDBY	PF1	Port F1 I/O	CLKEN	Clock Enable Output
21	uP_NMI	INT0	Interrupt 0 Input	PA6	Port A bit 6 I/O
25	uP_IRQC	INT3	Interrupt 3 Input Only	PWMSYNC0	PWM 0 Sync Input Only
27	uP_IRQB	INT2	Interrupt 2 Input	PB0	Port B bit 0 I/O
29	uP_IRQA	INT1	Interrupt 1 Input	PA7	Port A bit 7 I/O
43	uP_UARTA_TX - PA4	UARTTX1	Debug UART Output	PA4	Port A bit 4 I/O
45	uP_UARTA_RX - PA3	UARTRX1	Debug UART Input	PA3	Port A bit 3 I/O
53	uP_AUX_CLK	CLKOUT	Output Clock from Microcontroller Output	PA5	Port A bit 5 I/O
54	uP_DACK1	DACK1	DMA acknowledge Output Only	CTOUT1B	Counter Timer Output Only
65	uP_SPI_FRM	SSPFRM	SPI Frame I/O	PA2	Port A bit 2 I/O
67	uP_SPI_MOSI_TX	SSPTX	SPI TX Output Only	UARTTX2	UART TX 2 Output Only
69	uP_SPI_MISO_RX	SSPRX	SPI RX Input Only	UARTRX2	UART RX 2 Input Only
71	uP_SPI_SCK	SSPCLK	SPI Clock Output	PA1	Port A bit 1 I/O
76	uP_nMWE2	nBLE2	Byte Lane Enable 2 Output Only	PH6	Port H bit 6 Output Only

5.4.2 J1A Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1	LCD_VSYNC - SPS	LCDFP	LCDFP Signal Output	PC7 or LCDSPS	Port C bit 7 I/O or LCDSPS Signal Output
2	LCD_HSYNC - LP	LCDLP	LCDLP Signal Output	PC5	Port C bit 5 I/O
3	LCD_DCLK	LCDDCLK	LCD Clock Output	PC3	Port C bit 3 I/O
5	LCD_MDISP - SPL - PC0	LCDSPL	LCDSPL Signal Output	PC0 or LCDENAB	Port C bit 0 I/O or LCDENAB Signal Output
7	LCD_CLS - VDDEN - PC1	LCDCLS	LCDCLS Signal Output	PC1 or LCDVDDEN	Port C bit 1 I/O or LCDVDDEN Signal Output
8	LCD_CLK_RETURN	PC2	Port C bit 2 I/O	LCDCLKIN	LCD Input Clock Input
10	LCD_CLS - VDDEN - PC1	LCDCLS	LCDCLS Signal Output	PC1 or LCDVDDEN	Port C bit 1 I/O or LCDVDDEN Signal Output
11	LCD_VSYNC – SPS	LCDFP	LCDFP Signal Output	PC7 or LCDSPS	Port C bit 7 I/O or LCDSPS Signal Output
12	G0	LCDVD6	LCD Data 6 I/O	PD4 or LCDPS	Port D bit 4 I/O or LCD Power Save Output
13	LCD_MDISP - SPL - PC0	LCDSPL	LCDSPL Signal Output	PC0 or LCDENAB	Port C bit 0 I/O or LCDENAB Signal Output
14	LCD_HSYNC - LP	LCDLP	LCDLP Signal Output	PC5	Port C bit 5 I/O
16	B0	LCDVD12	LCD Data 12 I/O	PB4 or LCDREV	Port B bit 4 I/O or LCDREV Signal Output

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
17	uP_STATUS_1	PB1	Port B bit 1 I/O	DEOT0	DMA End Of Transfer Output
43	R2	LCDVD2	LCD Data 2 I/O	PD0	Port D bit 0 I/O
45	R3	LCDVD3	LCD Data 3 I/O	PD1	Port D bit 1 I/O
46	R4	LCDVD4	LCD Data 4 I/O	PD2	Port D bit 2 I/O
47	R5	LCDVD5	LCD Data 5 I/O	PD3	Port D bit 3 I/O
49	G1	LCDVD7	LCD Data 7 I/O	PD5	Port D bit 5 I/O
50	G2	LCDVD8	LCD Data 8 I/O	PD6	Port D bit 6 I/O
51	G3	LCDVD9	LCD Data 9 I/O	PD7	Port D bit 7 I/O
52	G4	LCDVD10	LCD Data 10 I/O	INT6	Interrupt 6 Input
53	G5	LCDVD11	LCD Data 11 I/O	INT7	Interrupt 7 Input
56	B1	LCDVD13	LCD Data 13 I/O	PB5	Port B bit 5 I/O
57	B2	LCDVD14	LCD Data 14 I/O	PB6	Port B bit 6 I/O
58	B3	LCDVD15	LCD Data 15 I/O	PB7 or LCDDSPLEN	Port B bit 7 I/O or LCDDSPLEN Signal Output
59	B4	LCDVD16	LCD Data 16 I/O	PC4	Port C bit 4 I/O
60	B5	LCDVD17	LCD Data 17 I/O	PC6	Port C bit 6 I/O

5.4.3 J1B Expansion Connector Pin Multiplexing

Pin #	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
30	uP_UARTB_TX - IR	UARTTX0	UART B TX Output Only	UARTIRTX0	IRDA TX Output Only
31	uP_UARTB_RX - IR	UARTRX0	UART B RX Input Only	UARTIRRX0	IRDA RX Input Only
41	uP_UARTB_TX - IR	UARTTX0	UART B TX Output Only	UARTIRTX0	IRDA TX Output Only
42	uP_UARTB_RX - IR	UARTRX0	UART B RX Input Only	UARTIRRX0	IRDA RX Input Only
48	MFP9 - CLKIN/UARTCLK	CLKIN	External Clock Input Input Only	UARTCLK	UART Input Clock Input Only
62	MFP22 - PWM1/DEOT1	PWM1	PWM Channel 1 Output Only	DEOT1	DMA End Of Transfer Output Only
72	MFP31 - uP_nMCS3	nCS3	Chip Select 3 Output Only	PH2	Port H bit 2 Output Only

6 Mechanical Specifications

6.1 Interface Connectors

The LH79520-10 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM Connector must be 3.7mm mating height.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

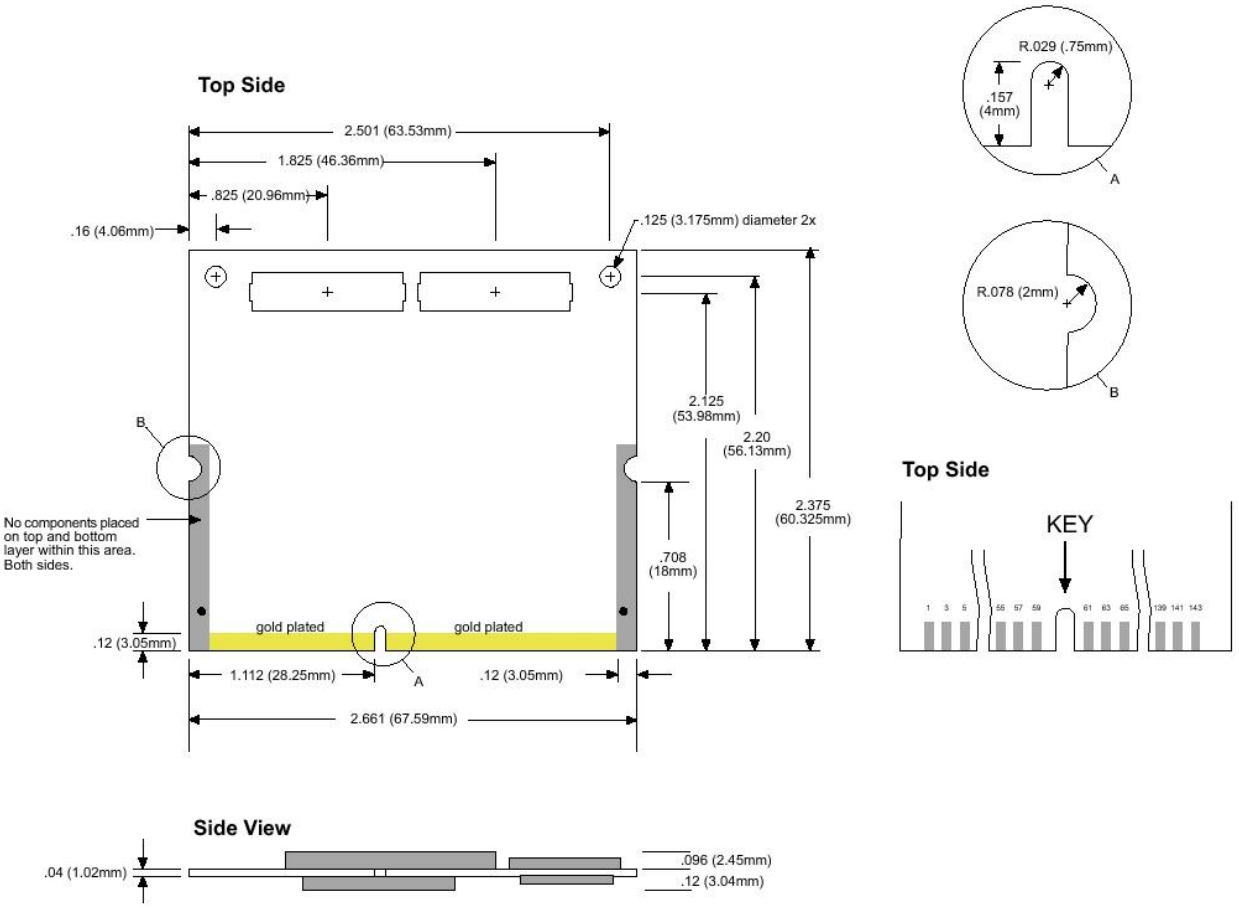


Figure 6.1: Card Engine Mechanical Drawing

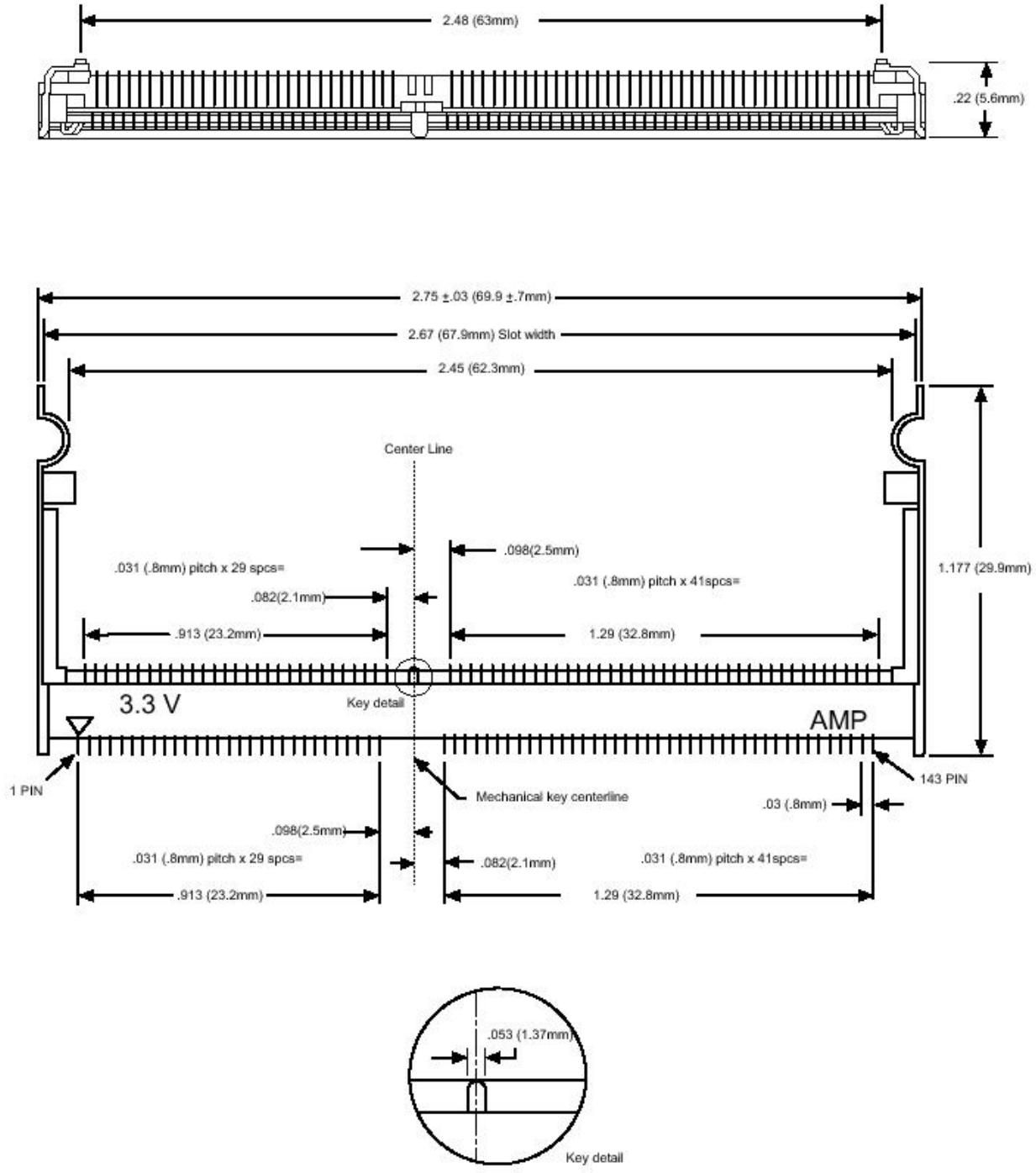


Figure 6.2: SODIMM Connector Specification

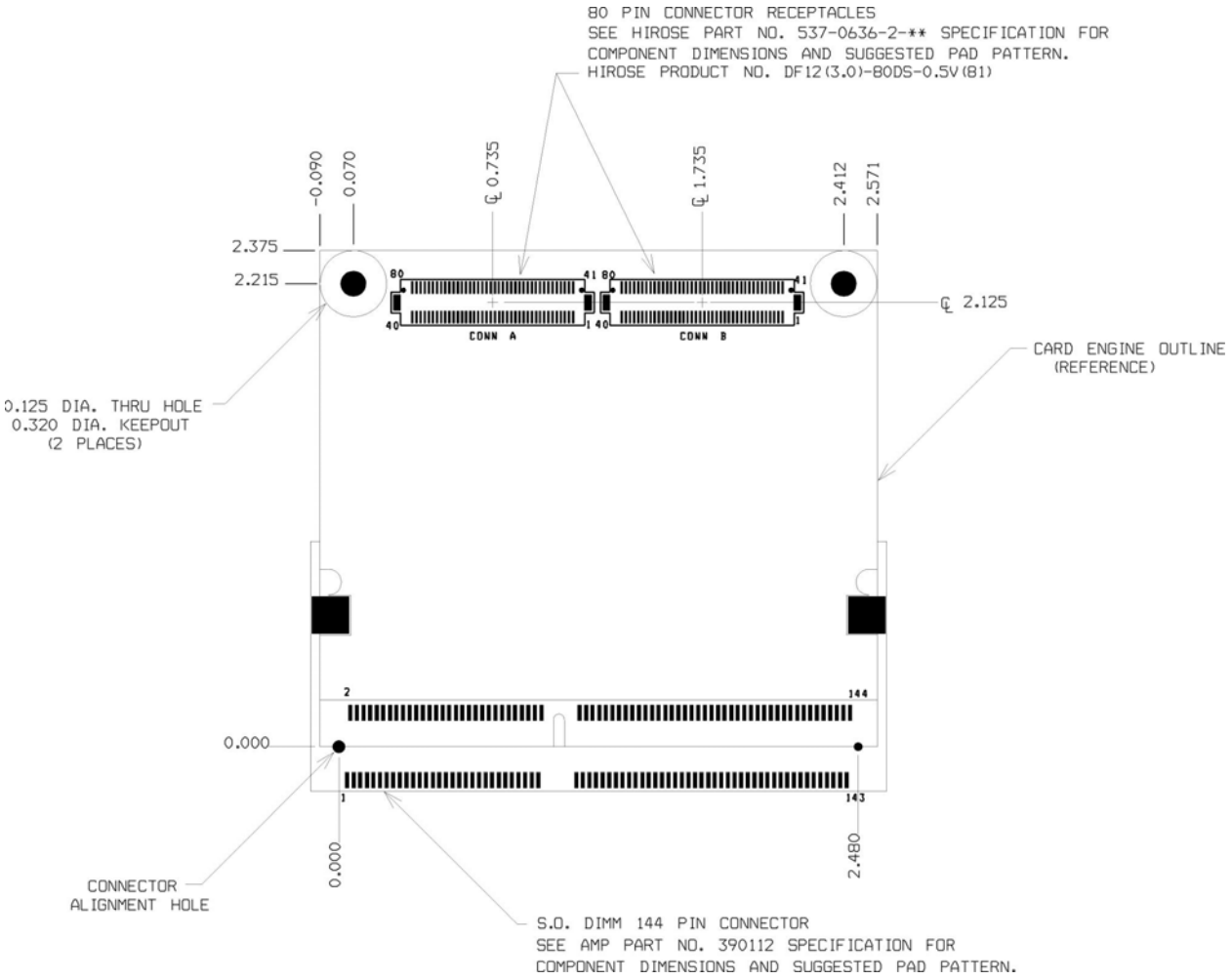


Figure 6.3: Recommended PCB Layout

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