LH7A404-10 to LH7A404-11 Card Engine Migration

Application Note 238

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Abstract

This application note is for developers who are presently using the LH7A404-10 card engine with the intention of migrating to the LH7A404-11 card engine.

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REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
A	Erik Reynolds	Release	HAR	6/21/2004
B	James Wicks	Correction, Section 2.2	JAW	7/14/2004

1 Introduction

This document applies to customer intending to migrate from the LH7A404-10 card engine (Logic PN: 80000127-xxxx) to the LH7A404-11 card engine (Logic PN: 80000258-xxxx).

The LH7A404-10 card engine is being phased out and is replaced by the LH7A404-11 card engine. The newer "-11" model has numerous changes and added features. They include changing the processor package, replacing the original on-board CPLD with a different part to reduce power consumption, and the addition of NAND Flash and EEPROM population options. Multiple hardware modifications were made to adjust for the changes.

This document details 1) the hardware changes that have been made and 2) describes software changes that may need to be made to accommodate the hardware changes for full product functionality.

2 Migrating to the LH7A404-11

The LH7A404-10 card engine uses the PBGA microprocessor package from Sharp Microelectronics which has been obsoleted and replaced by a CABGA package. The LH7A404-11 card engine utilizes the new CABGA package. Customers that have or are in the process of designing their product with the LH7A404-10 card engine will need to migrate to the -11 card engine so that the processor type will be supported.

The following sections detail hardware, software, and firmware changes between the LH7A404-10 and the -11 models so that customers can best determine if their implementation of the card engine base board needs to change to facilitate the migration.

2.1 General Hardware Changes

- The signal for the Address Buffer direction control on the engine has been removed from the expansion connector J1A.
- The default population of the jumper block JP1 – JP22 has changed – see associated schematic page for new default population.
- Added net uP_UARTB_RTS to A404 processor pin C3 (PE5/SCCLKEN) this replaces net uP_PER.
- The SDRAM chip select, uP_nSDCS0 is no longer routed off the card engine.
- Added NAND Flash footprint (not populated), added EPROM footprint (not populated)
- Added signal uP_UARTB_RTS, in place of A404 GPIO signal PE5/SCCLKEN
- Changed how the signal nPWRFL is controlled on the A404, it is now controlled by the CPLD

2.2 CPLD Changes

- Changed CPLD part from an Altera MAX7000 part to a Xilinx Coolrunner II part.
- Removed signals: uP_nWE3, BUFF_DIR_ADDRESS, uP_AUX_CLK_INT, MFP30-uP_nSDCS2, MFP31 – uP_nSDCS1, WRLAN_25, uP_WAKEUP
- Added signals: uP_PCC_BVD1, uP_PCC_BVD2, NAND_RDnBY, NAND_nRE, NAND_nWE, NAND_nCE, uP_STANDBY, uP_nPWFL

2.3 PCMCIA Interface Changes

- Removed PCMCIA status signals uP_PCC_BVD1, uP_PCC_BVD2 from the processor, they are now inputs to the CPLD and are read from the mode register.
- Swapped nets uP_PCC_RDYA and uP_PCC_RDYB on the two expansion connectors J1A and J1B.

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2.4 NOR Flash Interface Changes:

- Moved the signal FLASH_STS1 from processor port PC6 to PA6.

2.5 Software Changes:

2.5.1 CPLD Changes (no register address changes) see LH7A404-11 IO Controller Spec for details:

- Card Engine Control Register 0x7020 0000: added software settable interrupt source bit(7).
- Interrupt/Mask Register 0x70C0 0000: removed PCMCIA card detect signals and masks, CD2 MSK bit(6), CD1 MSK bit(5), nCD2 bit(4), and nCD1 bit(4). The PCMCIA card detects are no longer interruptible and were moved to the Mode Register (see below) and must be polled.
- Mode Register 0x70E0 0000: added PCMCIA Status bits BVD2 bit(7), CD2 bit(6), BVD1 bit(5), CD1 bit(4).
- Power Management Register 0x7120 0000: added signal nSTANDBY, STBY bit(4).
- GPIO Data Register 0x7180 0000: removed signal CPLD_GPIO_3 bit(1). This is no longer available to the user.
- GPIO Direction Register 0x71A0 0000: changed functionality of bit(1). This bit used to control the direction of the signal CPLD_GPIO_3, this signal does not exist anymore. Bit(1) is now used as the GPIO active bit. Its function is allow users who choose to use the A404's PCMCIA signals as GPIO. The CPLD uses some of these signals in its buffer control logic. This bit is used to either enable or disable the PCMCIA signals from the buffer control logic equation, thus allowing someone to use them as GPIO.

3 Summary

Logic Product Development Windows CE and LogicLoader BSP's have implemented the changes described in this document in order to provide the most updated functionality of the new LH7A404 CABGA processor package to our customers. The majority of the changes will not require a customer base board change, but the details have been listed so that customers can evaluate the ramifications of the migration. Please consider all changes when migrating from the LH7A404-10 to the LH7A404-11 card engine products.

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