LH7A400-10
Card Engine

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IO Controller Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CPLD Version	APPROVAL	DATE
A	Colette O'Brien	Document Created	--	CO	06/16/03
B	Erik Reynolds	Updated GPIO information; Applicable for CPLD Code Update	--	ER	08/21/03
C	Kurt Larson, James Wicks	SPI Interface Section Edit; Release: Rev. A to B	3.4	KTL	02/09/04
D	Kurt Larson	Interrupt Source Section Edit; Release: Rev C and D	3.4	KTL	03/08/04
E	Hans Rempel	Document Update: Added required wait state control registers for ISA and CF; SWINT, SCACT, and GPACT bit details	3.7	HAR	07/30/04
F	Hans Rempel, Nathan Kro	Document update: PDRV bit explanation, updated ISA-Like Bus diagrams	3.E	HAR	04/12/05
G	Jed Anderson	Added note to reference App Note 303 in Section 4	3.E	BR	09/16/05
H	Jed Anderson	Corrected signal name "uP_USB1_nOVR_CRNT" which was mistakenly listed as "uP_USB1_OVR_CRNT"	4.0	SJS	05/07/07

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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LH7A400 I/O CONTROLLER

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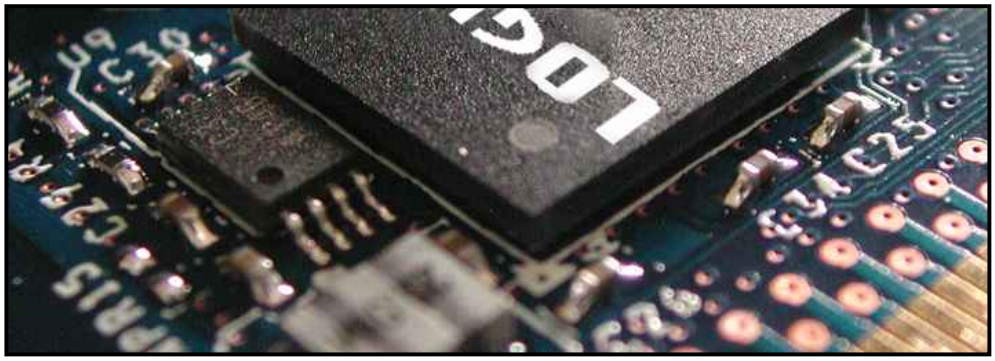
Logic offers production-ready I/O controller devices and design packages for customers creating custom Card Engine designs and CPLD code for Logic's Card Engines. Logic has optimized the VHDL code to fit in the smallest possible programmable logic device. This results in an embedded product development cycle with **less time, less cost, less risk ... more innovation.**



- **I/O Controller was written in VHDL and contains the following:**
  - SPI (parallel to SPI interface)
  - ISA-like bus interface
  - SMSC LAN91C111 wired LAN bus interface and power control logic
  - Buffer control logic
  - Chip select decoder logic
  - Interrupt encoder logic
  - Flash program control logic
  - Processor mode control logic
  - IC code revision register

- **I/O Controller Device**
  - 100-pin FBGA package (Logic Part No. 31300181-P01-0110)

- **Source Code**
  - Includes all VHDL code (licensable .vhd source code files)

- **Support**
  - VHDL IP Core Source Code Design Package includes the Bronze level support package

** Some controllers do not require I2S*

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

For more information on our Embedded Platform Solutions, please contact Logic Sales at www.logicpd.com or 612.672.9495.

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1.2 Acronyms

BALE	Buffered Address Latch Enable
CF	CompactFlash
CS	Chip Select
GPIO	General Purpose Input Output
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Electrically Programmable Read Only Memory
IO	Input Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LAN	Local Area Network
LED	Light Emitting Diode
MB	Megabyte (2^20 bytes)
SPI	Serial Peripheral Interface

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Altera MAX 7000A PLD data sheet (EPM7128AFC100-10)
- Altera Device Package Information data sheet
- Altera Ordering Information
- Texas Instruments (Burr-Brown) ADS7843 data sheet

1.4 IO Controller Advantages

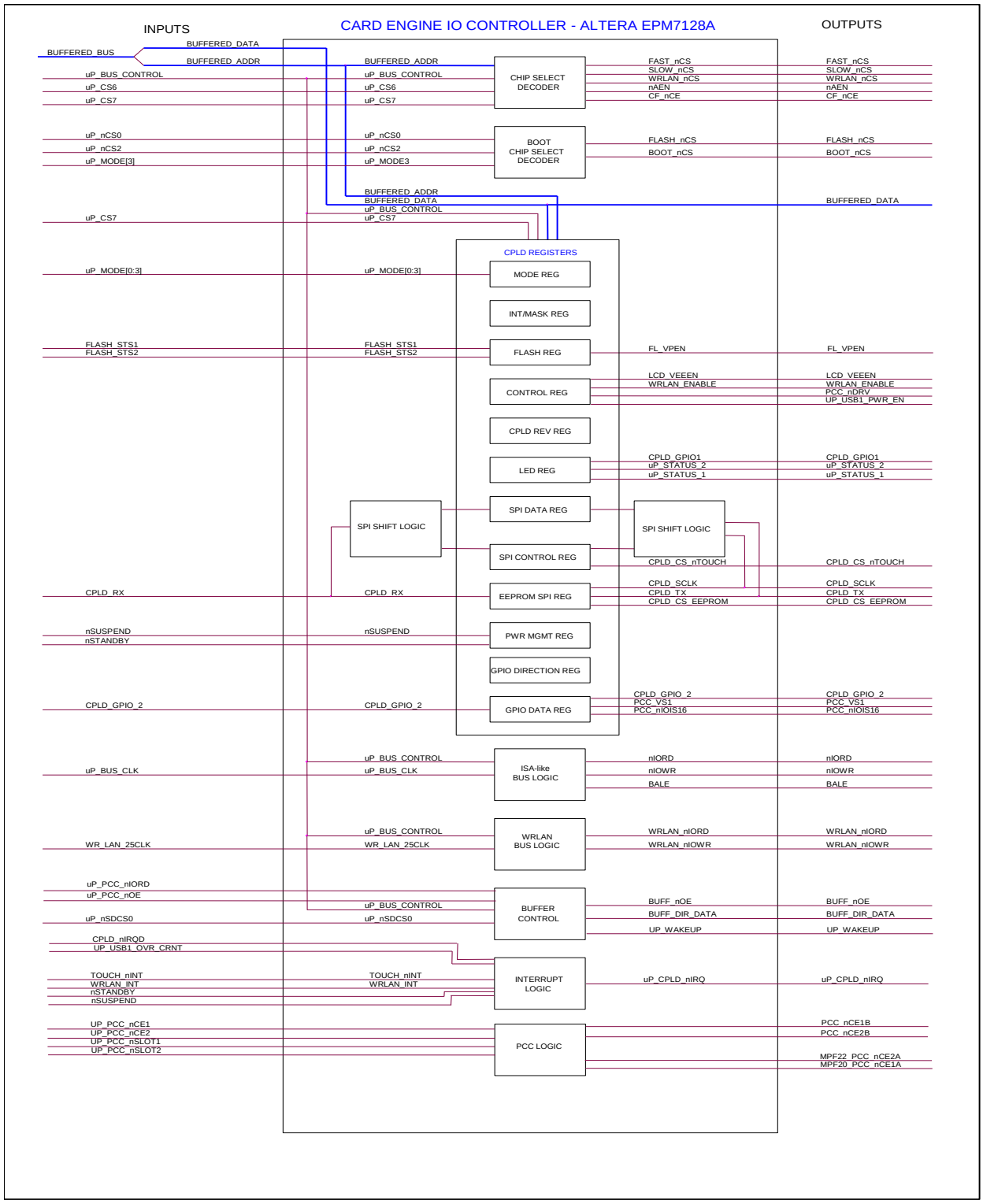
Some of the key features in the IO Controller include:

- Multiple Parallel to SPI Interface
- Chip Select Decoder
- Interrupt Decoder
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player

The IO Controller VHDL source code is available for purchase. Contact Logic for more information.

2 IO Controller Block Diagram

Figure 2.1: IO Controller Block Diagram



3 IO Controller Address and Register Definitions

Address Range	Memory Block Description	Size
0x7000 0000 – 0x7FFF FFFF	Fast Peripherals Chip Select 7 (CS7)	64MB
0x6000 0000 – 0x6FFF FFFF	Slow Peripherals Chip Select 6 (CS6)	64MB

3.1 Fast Peripherals Chip Select 7 (CS7)

Address Range	Memory Block Description	Size
0x7000 0000 – 0x701F FFFF	Wired LAN Chip Select	2MB
0x7020 0000 – 0x703F FFFF	Card Engine Control Reg	2MB
0x7040 0000 – 0x705F FFFF	Reserved	2MB
0x7060 0000 – 0x707F FFFF	SPI Data Reg	2MB
0x7080 0000 – 0x709F FFFF	SPI Control Reg	2MB
0x70A0 0000 – 0x70BF FFFF	EEPROM SPI Reg	2MB
0x70C0 0000 – 0x70DF FFFF	Interrupt/Mask Reg	2MB
0x70E0 0000 – 0x70FF FFFF	Mode Reg	2MB
0x7100 0000 – 0x711F FFFF	Flash Reg	2MB
0x7120 0000 – 0x713F FFFF	Power Management Reg	2MB
0x7140 0000 – 0x715F FFFF	IO Controller Code Revision Reg	2MB
0x7160 0000 – 0x717F FFFF	Extended GPIO Reg	2MB
0x7180 0000 – 0x719F FFFF	GPIO Data Reg	2MB
0x71A0 0000 – 0x71BF FFFF	GPIO Direction Reg	2MB
0x71C0 0000 – 0x71FF FFFF	Reserved - On-Board Expansion	2MB (X2)
0x7200 0000 – 0x72FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x7300 0000 – 0x73FF FFFF	Open – Available for User	1MB (X16)

Each memory block for chip select 7 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.1.1 Wired LAN Chip Select

Address Range: 0x7000 0000 – 0x701F FFFF

- This area of memory is used when accessing the Wired LAN chip (internal registers/memory).

3.1.2 Card Engine Control Register

Address Range: 0x7020 0000

- This register holds control bits for the Card Engine.

7	6	5	4	3	2	1	0	
SWINT	OCMSK	PDRV	USB1OC	USB1P	AWKP	LCDV	WLPE	
1	0	1	-	1	0	0	0	reset
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

SWINT: Software settable interrupt source – setting this bit to '0' forces an interrupt on the CPLD interrupt bit (uP_CPLD_nIRQ) back to the processor. It must be set back to a '1' to clear the interrupt condition (this is usually done within the interrupt service routine).

0 = generate an interrupt on uP_CPLD_nIRQ
1 = do not generate an interrupt on uP_CPLD_nIRQ

OCMSK: USB1 connection interrupt mask. This signal masks the interrupt caused by the uP_USB1_nOVR_CRNT.

0 = interrupt not masked
1 = interrupt masked

PDRV: PCC_nDRV output. This bit controls the level of the PCC_nDRV Card Engine interface signal meant for PCMCIA buffer and/or power enable control. This bit is valid and active at all times (regardless of the state of the GPACT bit in the GPIO Direction Register).

0 = PCC_nDRV signal outputs low
1 = PCC_nDRV signal outputs high

USB1C: USB1 connection interrupt. The Card Engine signal is uP_USB1_nOVR_CRNT but is used as a VBUS connection interrupt. When uP_USB1_nOVR_CRNT is high, the USB1C bit will read low. When uP_USB1_nOVR_CRNT signal is low, the USB1C bit will read high.

0 = USB1 connection interrupt active
1 = USB1 connection interrupt inactive

USB1P: Power enable for USB1. A USB driver should drive this bit low during initialization. It will allow a connection interrupt to be generated on the USB1C bit when a USB cable is plugged into the adapter board and another powered device.

0 = USB1 power enabled
1 = USB1 power disabled

AWKP: Auto-Wakeup enable signal. This bit enables/disables the uP_WAKEUP signal which is used at power up to automatically bring the processor out of the standby state.

0 = Auto-Wakeup feature enabled
1 = Auto-Wakeup feature disabled

LCDV: LCD_VEEEN signal. This bit enables/disables the LCD VEE signal which can be used for backlight control and STN display power sequencing.

0 = Disable LCD VEE (set pin low)
1 = Enable LCD VEE (set pin high)

WLPE: Wired LAN power enable signal. This bit enables/disables power to the on-board Wired LAN chip.

0 = Wired LAN enabled
1 = Wired LAN disabled

3.1.3 Reserved

Address Range: 0x7040 0000 – 0x705F FFFF

- This memory block is reserved.

3.1.4 SPI Data Register

Address Range: 0x7060 0000

- This register holds the SPI data for transmit or receive. This SPI register is used in the interface to the touch chip. See Section 4.3 for a detailed description of the SPI interface and how to use it.

7	6	5	4	3	2	1	0	
8-bit SPI data								
0	0	0	0	0	0	0	0	reset
R/W								R/W

3.1.5 SPI Control Register

Address Range: 0x7080 0000

- This register controls the transmission and reception of SPI data, to/from the 8-bit SPI data register (Section 3.1.4).

7	6	5	4	3	2	1	0	
-	-	SPLD	SPST	SPDN	SPRW	STCS	SCCS	
		0	0	0	0	0	0	reset
-	-	R	R/W	R	R/W	R/W	R/W	R/W

SPLD: SPI load.
0 = SPI data register has not been loaded and shift count has not been reset
1 = SPI data register has been loaded and shift count has been reset

SPST: SPI start.
0 = don't load SPI data register and reset shift count
1 = ready to load SPI data register and reset shift count

SPDN: SPI done.
0 = not done
1 = SPI access done

SPRW: SPI read/write.
0 = SPI write access
1 = SPI read access

STCS: SPI touch chip select.
0 = not selected
1 = touch chip selected

SCCS: SPI CODEC chip select (not used).

0 = not selected
1 = CODEC chip selected

3.1.6 EEPROM SPI Interface Register

Address Range: 0x70A0 0000

- This register holds SPI data during a read/write between the processor and on-board EEPROM. This SPI interface used for the EEPROM is directly controlled by the processor, and is not timed by the IO Controller.

7	6	5	4	3	2	1	0	
-	-	-	-	EECS	EECK	EETX	EERX	
-	-	-	-	0	0	0	0	reset
-	-	-	-	R/W	R/W	R/W	R	R/W

EECS: EEPROM chip select.
0 = not selected
1 = EEPROM chip selected

EECK: EEPROM spi clock.

EETX: EEPROM spi data transmit.

EERX: EEPROM spi data receive.

3.1.7 Interrupt/Mask Register

Address Range: 0x70C0 0000

- This register contains the bits used by the IO Controller to generate an interrupt to the processor via net uP_CPLD_nIRQ. The bits in this register are not latched and will return the actual state of the corresponding interrupt upon a read of this register.

7	6	5	4	3	2	1	0	
CMSK	CIRQ	-	PIRQ	TMSK	WMSK	TIRQ	WIRQ	
0	-	-	1	0	0	1	1	reset
R/W	R	-	R/W	R/W	R/W	R	R	R/W

CMSK: CPLD_nIRQD interrupt mask.
0 = interrupt not masked
1 = interrupt masked

CIRQ: interrupt signal to CPLD.
0 = interrupt is active
1 = no interrupt

PIRQ: Bit exists for legacy software, but is not required for touch functionality. Setting this bit to 0 or 1 does nothing. This bit can be ignored.

TMSK: touch chip interrupt mask.
0 = interrupt not masked
1 = interrupt masked

WMSK: Wired LAN chip interrupt mask.

0 = interrupt not masked
1 = interrupt masked

TIRQ: touch chip interrupt request (IRQ).
0 = interrupt is active
1 = no interrupt

WIRQ: Wired LAN chip interrupt request (IRQ).
0 = interrupt is active
1 = no interrupt

* Other interrupt sources include the USB1C and SWINT bits in the Card Engine Control Register and the STBY and SPND bits in the Power Management Register.

3.1.8 Mode Register

Address Range: 0x70E0 0000

- Reading this register will return the current state of the mode pins.

7	6	5	4	
VS1	CD2	IOIS16	CD1	
0	-	0	-	reset
R	R	R	R	R

3	2	1	0	
uP_MODE3	uP_MODE2	uP_MODE1	uP_MODE0	
-	-	-	-	reset
R	R	R	R	R

VS1: PCMCIA Voltage Sense 1 input. Signal name PCC_VS1.
0 = Active slot VS1 pin is low
1 = Active slot VS1 pin is high

CD2: PCMCIA Card Detect 2 input. Signal name PCC_nCD2.
0 = Active slot Card Detect 2 is low
1 = Active slot Card Detect 2 is high

IOIS16: PCMCIA IOIS16 input. Signal name PCC_nIOIS16.
0 = indicates a 16 bit access area
1 = indicates a 8 bit access area

CD1: PCMCIA Card Detect 1 input. Signal name PCC_nCD1.
0 = Active slot Card Detect 1 is low
1 = Active slot Card Detect 1 is high

uP_MODE3: mode pin 3. Mode pin 3 selects between on-board and off-board boot device. See Section 4.2 for detailed information on mode pin 3.
0 = off-board boot device
1 = on-board boot device (flash memory)

uP_MODE2: mode pin 2. Mode pin 2 represents the endian setting for the processor. (The LH7A400 supports little endian only. The value of this bit is ignored.)

0 = big endian
1 = little endian

uP_MODE1, uP_MODE0: mode pin 1 and mode pin2. These mode pins represent the bus width at boot. Bit MDP0 controls processor pin BOOTWIDTH0 and bit MDP1 controls processor pin BOOTWIDTH1.

(Note: See LH7A400 datasheet for specific setting options for pins BOOTWIDTH0 and BOOTWIDTH1.)

3.1.9 Flash Register

Address Range: 0x7100 0000

- This register holds status information for the Flash.

7	6	5	4	3	2	1	0	
-	-	-	-	FPOP	FST2	FST1	FPEN	
-	-	-	-	1	-	-	0	reset
-	-	-	-	R/W	R	R	R/W	R/W

FPOP: Flash populated bit.
0 = Flash populated
1 = Flash not populated

Note: This bit is used to generate the Flash chip select, when mode pin 3 is low. This bit is ignored when mode pin 3 is high. See Section 4.2 for detailed information on mode pin 3.

FST2: Flash status pin. This is the RY/BY# pin for the upper 16 bit Flash chip.
0 = Flash busy
1 = Flash ready

FST1: Flash status pin. This is the RY/BY# pin for the lower 16 bit Flash chip.
0 = Flash busy
1 = Flash ready

FPEN: Flash program enable.
0 = normal Flash operations
1 = program Flash enabled

3.1.10 Power Management Register

Address: 0x7120 0000

- Reading this register will return the current value of the nSUSPEND and nSTANDBY input signals to the cpld.

7	6	5	4	3	2	1	0	
-	-	-	STBY	-	SPND	-	-	
-	-	-	-	-	-	-	-	reset
-	-	-	R	-	R	-	-	R

STBY: value of the nSTANDBY input signal to the cpld. The nSTANDBY signal has a pull-up resistor on the card engine.
0 = nSTANDBY signal is low
1 = nSTANDBY signal is high

SPND: value of the nSUSPEND input signal to the cpld. The nSUSPEND signal has a pull-up resistor on the card engine.
0 = nSUSPEND signal is low
1 = nSUSPEND signal is high

Note: When nSUSPEND or nSTANDBY is low, an interrupt to the processor will be generated. There are no interrupt mask bits for the nSUSPEND or nSTANDBY signals.

3.1.11 IO Controller Code Revision Register

Address Range: 0x7140 0000

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								reset
R								R

3.1.12 Extended GPIO Register

Address Range: 0x7160 0000

- This register controls extended general-purpose signals.

7	6	5	4	3	2	1	0	
-	-	-	-	-	uP_STATUS_1	uP_STATUS_2	CPLD_GPIO_1	
-	-	-	-	-	1	1	1	reset
-	-	-	-	-	R/W	R/W	R/W	R/W

uP_STATUS_1 : Status 1 output bit (net uP_STATUS_1). Can be used as a general purpose output.
0 = Set pin low
1 = Set pin high

uP_STATUS_2 : Status 2 output bit (net uP_STATUS_2). Can be used as a general purpose output.
0 = Set pin low
1 = Set pin high

CPLD_GPIO_1 : General purpose output bit (net CPLD_GPIO_1).
0 = Set pin low
1 = Set pin high

3.1.13 GPIO Data Register

Address: 0x7180 0000

- This register controls the state of the CPLD general-purpose input/output pins. Note: The direction (input or output) of the CPLD pins are set in the GPIO Direction Register in Section 3.1.14.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	CPLD_GPIO_2	
-	-	-	-	-	-	-	0	reset
-	-	-	-	-	-	-	R/W	R/W

CPLD_GPIO_2: Controls state of general purpose input/output bit CPLD_GPIO_2. Outputs register value when configured as output, reads pin state when configured as input.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output. read pin state high if configured as input

3.1.14 GPIO Direction Register

Address: 0x71A0 0000

- This register controls the direction for the CPLD general purpose input/output pins. Note: The value (high or low) of the CPLD pins are read/written in the GPIO Data Register in Section 3.1.13.

7	6	5	4	3	2	1	0	
-	-	-	-	-	SCACT	GPACT	GPDR0	
-	-	-	-	-	1	0	0	reset
-	-	-	-	-	R/W	R/W	R/W	R/W

GPDR0: GPIO direction bit 0.
0 = external CPLD signal CPLD_GPIO_2 is an output.
1 = external CPLD signal CPLD_GPIO_2 is an input.

GPACT: GPIO active – this bit enables or disables buffer control based on the PCMCIA slot signals. If this bit is 0, the card engine buffers and PCMCIA CE signals will be controlled via the PCMCIA control signals. If this bit is a 1, the buffer control equations will ignore the PCMCIA signals because the user intends to use them as GPIO and not as PCMCIA control signals.
0 = input PCMCIA control signals to CPLD enabled (GPIO disabled).
1 = input PCMCIA control signals to CPLD disabled (GPIO enabled).

SCACT: Smart Card active – this bit enables or disables the use of address line 25 in buffer control and address decoding. If this bit is a 0, address line 25 (A25) is given the value of '0' in all of the address decode and buffer control equations. If this bit is a 1, the true value of address line 25 (A25) is used in the address decode and buffer control equations. This was done because the LH7A400 processor multiplexes the smart card I/O signal with A25, requiring the detachment of the state of the signal value in buffer and address decode equations when the smart card interface is in use.
0 = Smart Card enabled.
1 = Smart Card disabled.

3.1.15 Reserved On-Board Memory Blocks

Address Range: 0x71C0 0000 – 0x71FF FFFF

- These two memory blocks are reserved for future on-board expansion.

3.1.16 Reserved Off-Board Memory Blocks

Address Range: 0x7200 0000 – 0x72FF FFFF

- These sixteen memory blocks are reserved for off-board IO controller expansion.

3.1.17 Open Memory Blocks – Available for User

Address Range: 0x7300 0000 – 0x73FF FFFF

- These sixteen memory blocks are open and available for the user to utilize.

3.2 Slow Peripherals Chip Select 6 (CS6)

Address Range	Memory Block Description	Size
0x6000 0000 – 0x601F FFFF	Reserved	2MB
0x6020 0000 – 0x603F FFFF	CF Chip Select	2MB
0x6040 0000 – 0x605F FFFF	ISA-like Bus Chip Select	2MB
0x6060 0000 – 0x61FF FFFF	Reserved - On-Board Expansion	2MB (X13)
0x6200 0000 – 0x62FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x6300 0000 – 0x63FF FFFF	Open – Available for User	1MB (X16)

Each memory block for chip select 6 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.2.1 CompactFlash (CF) Chip Select

Address Range: 0x6020 0000 – 0x603F FFFF

- This area of memory is used when accessing the off-board memory mapped CompactFlash Type 1 Memory Only slot. Accesses to this address range assert the external card enable net “CF_nCE.”

3.2.2 ISA-like Bus Chip Select

Address Range: 0x6040 0000 – 0x605F FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 5 for read and write timing diagrams.

3.2.3 Reserved On-Board Memory Blocks

Address Range: 0x6060 0000 – 0x61FF FFFF

- These memory blocks are reserved for future on-board expansion.

3.2.4 Reserved Off-Board Memory Blocks

Address Range: 0x6200 0000 – 0x62FF FFFF

- These memory blocks are reserved for off-board IO controller expansion.

3.2.5 Open Memory Blocks – Available for User

Address Range: 0x6300 0000 – 0x63FF FFFF

- These memory blocks are open and available for the user to utilize.

4 IO Controller Functions

This section describes in detail the different IO Controller function blocks. See Section 2 for the IO Controller block diagram.

Note: A specific software protocol must be followed to access IO devices on Sharp Card Engines. Please see Logic's Application Note 303: *Interfacing to IO Devices via the Static Memory Controller on LH7xxxx Card Engines* for examples of the protocol when accessing registers within the CPLD. This document can be found at: http://www.logicpd.com/auth/default.php.

4.1 Chip Select Decoder Logic

This logic decodes processor chip selects 6 and 7 into smaller segments of memory. See Section 3.1 for the chip select 7 memory map, and Section 3.2 for the chip select 6 memory map.

CPLD signal FAST_nCS is output when uP_CS7 is low and uP_MA25 is high. CPLD signal SLOW_nCS is output when uP_CS6 is low and uP_MA25 is high. Signals FAST_nCS and SLOW_nCS are brought off the card engine through the expansion bus connectors.

4.2 Boot Chip Select Decoder Logic

Note: Mode pin 3 selects between on-board and off-board boot device.

The card engine can boot from a on-board Flash or an off-board memory device. The boot device selection is determined by a jumper setting (mode pin 3) on the application board. The boot device is always located in area 0 (CS0). When mode pin 3 is high, the on-board Flash is selected for boot, and when mode pin 3 is low, the off-board memory device is selected for boot. This logic implements the following table.

Flash register bit (3) is used to generate the Flash chip select, when mode pin 3 is low. This bit is ignored when mode pin 3 is high. See Section 3.1.9 for more information on the Flash register.

Flash (on-board)	Off-board memory	Mode Pin 3	Flash Reg (3)	Function
CS0 (area 0)	CS2 (area 2)	1	ignored	boot from Flash in area 0, off-board memory device is in area 2
CS2 (area 2)	CS0 (area 0)	0	0	boot from off-board memory device in area 0, Flash is in area 2
CS2 (area 2)	CS0 (area 0)	0	1	boot from off-board memory device in area 0, (Flash not populated) area 2 is open

The chip selects for area 0 and 2 are routed to the flash and off-board memory device by signals FLASH_nCS and BOOT_nCS.

4.3 SPI Interface

4.3.1 Usage Notes

The SPI interface usage flow is as follows:

SPI Read Cycle:
1) set SPST and SPRW to 1
2) poll SPLD bit until it equals 1
3) clear SPST bit to 0
4) poll SPDN bit until it equals 1
5) read the SPI data register for received data
6) repeat…

SPI Write Cycle:
1) write 8 bit data to SPI data register
2) set SPST to 1
3) poll SPLD bit until it equals 1
4) clear SPST to 0
5) poll SPDN bit until it equals 1
6) repeat…

4.3.2 Touch SPI Interface

See Texas Instruments (Burr-Brown) ADS7843 data sheet for the complete command set and registers. See sections 3.1.4 and 3.1.5 for the SPI Data and SPI Control Register bit definitions.

4.4 ISA-like Bus Logic (CompactFlash and ISA peripherals in area 6)

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic outputs the ISA chip select, CompactFlash chip select, BALE, read (nIORD), and write (nIOWR) signals. It also creates two timing delays in the ISA-like bus timing: first, the delay between the falling edge of the chip select (CompactFlash or ISA) and falling edge of read (nIORD) or write (nIOWR) signal, and second, the delay between the rising edge of the read or write signal and rising edge of the chip select.

The first delay is created by shifting the falling edge of the read (nIORD) or write (nIOWR) signal to create a delay from the chip select. The rising edge of the read and write signals are not delayed from the rising edge of the processor read and write signals. See Section 5 for sample read and write ISA-like timing diagrams.

The ISA device chip select is output by the CPLD when an access to address range 0x6040 0000 – 0x605F FFFF is made, and the CompactFlash chip select is output when an access to address range 0x6020 0000 – 0x603F FFFF is made. To create a timing delay between the rising edge of the read or write signal and the rising edge of the chip select, the chip select rising edge is delayed from the processor's area 6 chip select by a single bus clock cycle. The card engine buffers are turned off during this chip select extension, to retain the data on the bus while the chip select is still valid. See Section 5 for sample read and write ISA-like timing diagrams.

The ISA-like bus timing is shown with the maximum number of internal wait states programmed for the processor. This is implemented in order to accommodate for a CompactFlash card or ISA device that uses the nCHRDY signal, since the LH7A400 has no external wait state signal to connect to the nCHRDY signal. Not all CompactFlash cards or ISA devices will assert the nCHRDY signal. The user can change the programmed wait state values by modifying the WST1 and WST2 fields in the processor's Static Memory Controller Bus Configuration Register, for area 6.

4.5 Wired LAN Bus Logic

This logic creates read and write output signals to the Wired LAN chip by shifting the falling edge of the read and write signals from the processor, to meet the required Wired LAN timing. The rising edge of the Wired LAN read and write signals are not shifted.

An interrupt to the processor is generated when an interrupt from the Wired LAN is seen at the CPLD.

4.6 Buffer Control Logic

This logic controls the output enable and direction of the on-board buffers.

4.7 Interrupt Logic

This logic generates the processor's uP_CPLD_nIRQ, from information in the Interrupt/Mask register, Section 3.1.7, and the Power Management register, Section 3.1.10

5 ISA Timing Diagrams

5.1 ISA-like Bus, Read Cycle Timing Diagrams

The internal wait state timing registers on the LH7A400 processor must be setup properly in order to yield the bus timing figures below. For example, the “min 300nS” value associated with the nAEN and CF_nCE assertion during a read cycle is generated by the appropriate setting of the BCR6 register that controls the generated wait states for the SLOW_nCS region. These register settings are initialized for proper wait state control by Logic’s standard software offerings on the LH7A400-10 Card Engine.

Figure 5.1: ISA-like Bus, Compact Flash Read Cycle Timing

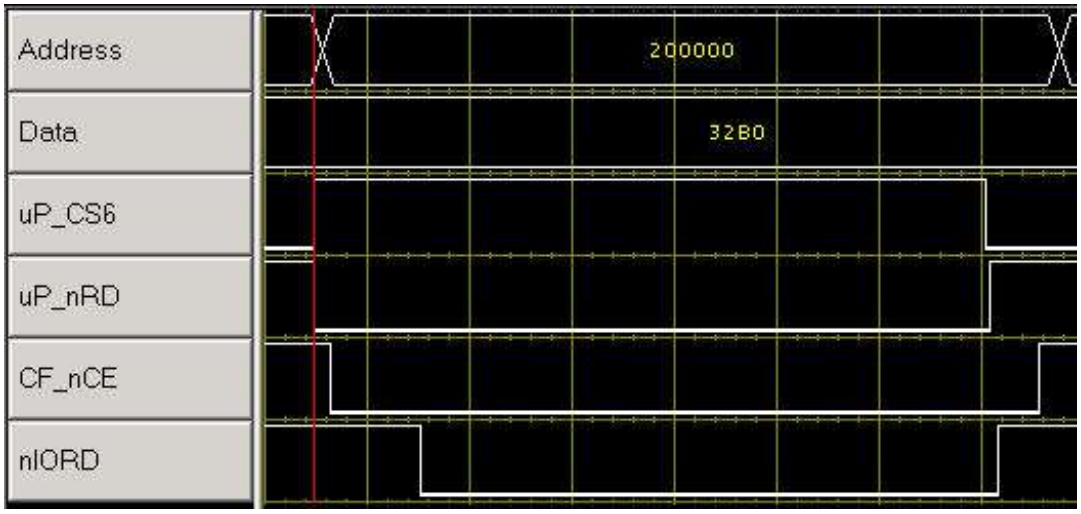


Figure 5.2: ISA-like Bus, ISA Read Cycle Timing

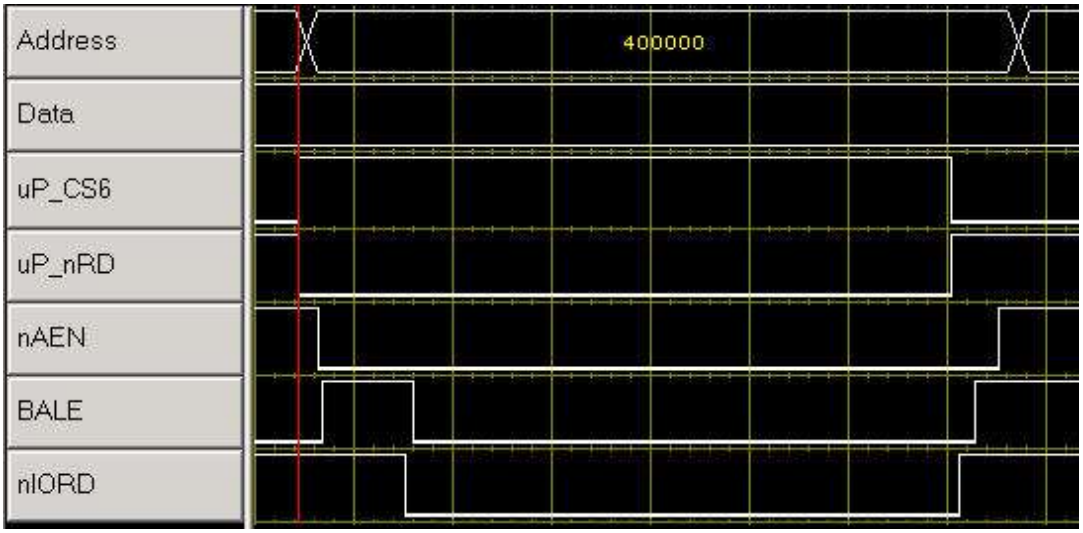
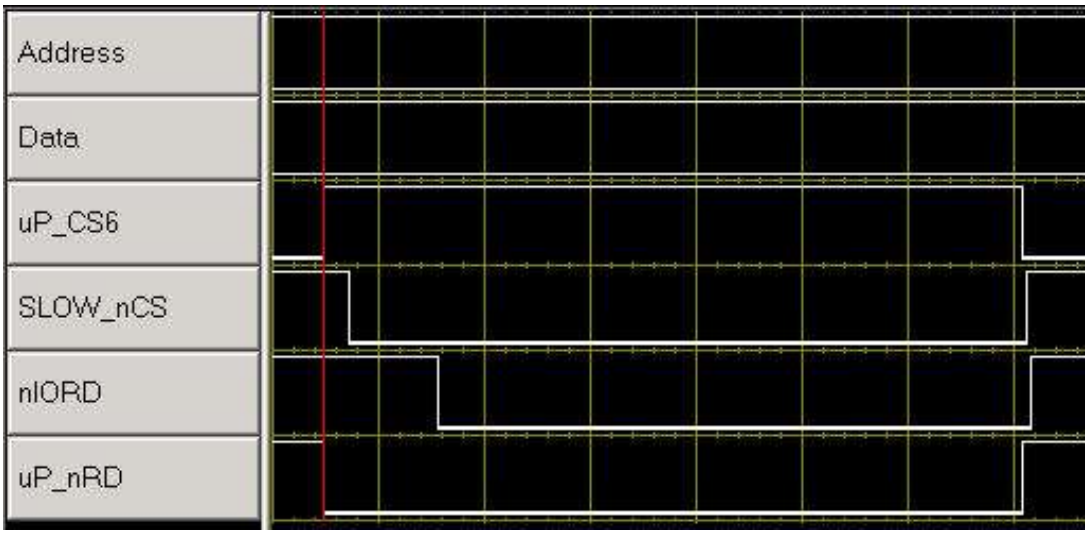


Figure 5.3: ISA-like Bus, SLOW_nCS Read Cycle Timing



Note: All timing parameters shown in 50 nanosecond (ns) divisions.

5.2 ISA-like Bus, Write Cycle Timing Diagrams

Figure 5.4: ISA-like Bus, Compact Flash Write Cycle Timing

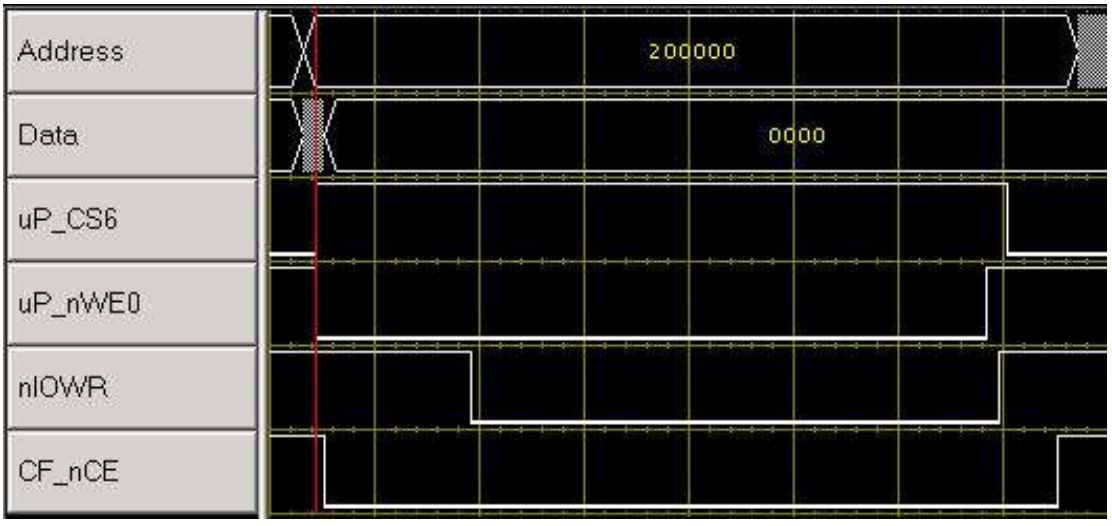


Figure 5.5: ISA-like Bus, ISA Write Cycle Timing

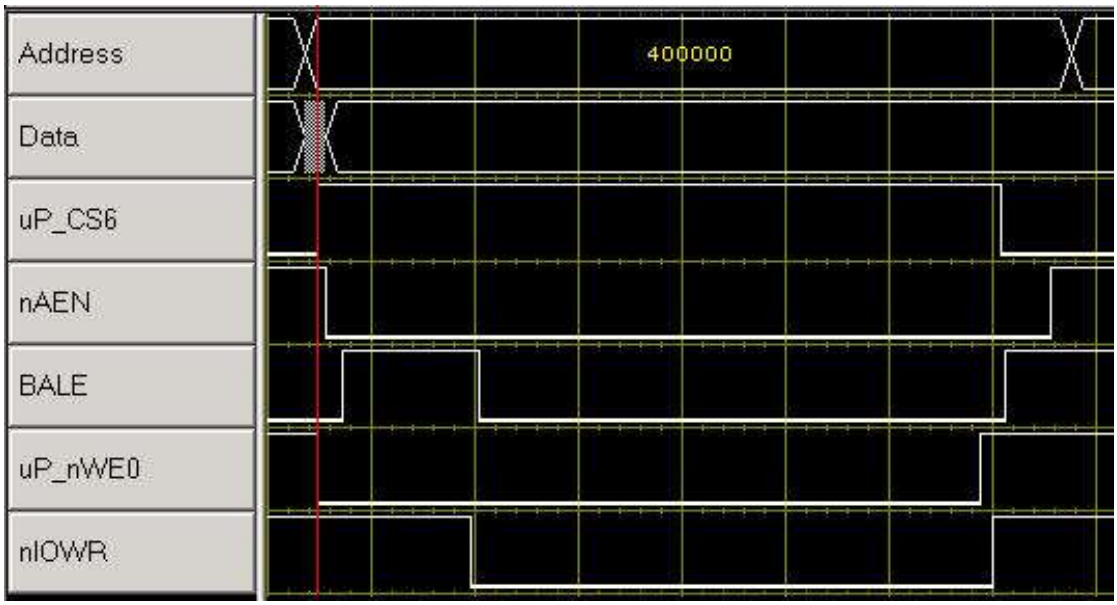
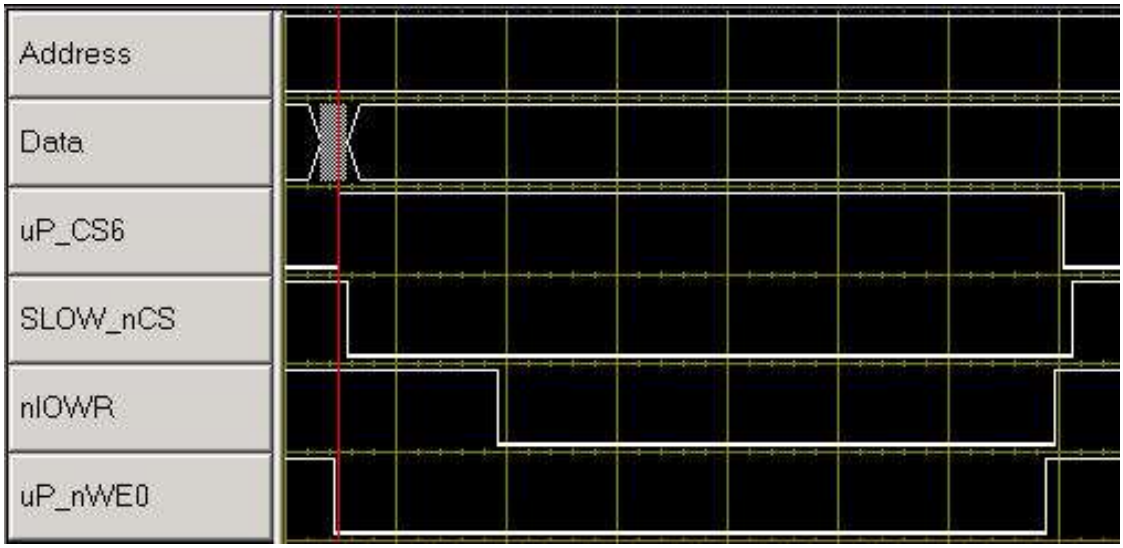


Figure 5.6: ISA-like Bus, SLOW_nCS Write Cycle Timing



Note: All timing parameters shown in 50 nanosecond (ns) divisions.

6 IO Controller Pin Information

Pin	Signal Name	Input/Output
14	uP_nCS0	Input
18	uP_nCS2	Input
17	uP_CS6	Input
56	SLOW_nCS	Output
58	FAST_nCS	Output
19	uP_CS7	Input
37	WR_LAN_25CLK	Input
29	WRLAN_nCS	Output
30	uP_nSDCS0	Input
44	CPLD_CS_nTOUCH	Output
46	CPLD_CS_EEPROM	Output
15	BOOT_nCS	Output
16	FLASH_nCS	Output
28	NSTANDBY	Input
54	CPLD_SCLK	Output
59	CPLD_TX	Output
63	CPLD_RX	Input
24	-	-
23	uP_CPLD_CLK	Input
6	uP_MA25	Input
2	uP_MA24	Input
1	uP_MA23	Input
4	uP_MA22	Input
3	uP_MA21	Input
32	uP_MODE3	Input
33	uP_MODE2	Input
34	uP_MODE1	Input
35	uP_MODE0	Input
42	uP_STATUS_2	Output
39	FL_VPEN	Output
60	FLASH_STS1	Input
61	FLASH_STS2	Input
40	WRLAN_ENABLE	Output
53	uP_CPLD_nIRQ	Output
94	TOUCH_nINT	Input/Output
97	WRLAN_INT	Input
42	uP_STATUS_2	Output
64	nSUSPEND	Input
43	uP_STATUS_1	Output
67	uP_MD0	Input/Output
68	uP_MD1	Input/Output
70	uP_MD2	Input/Output
71	uP_MD3	Input/Output
72	uP_MD4	Input/Output

Pin	Signal Name	Input/Output
74	uP_MD5	Input/Output
76	uP_MD6	Input/Output
77	uP_MD7	Input/Output
41	CPLD_GPIO_1	Output
52	CPLD_GPIO_2	Input/Output
9	CPLD_nIRQD	Input
10	PCC_nCD1	Input
11	PCC_nCD2	Input
12	uP_PCC_nCE1	Input
13	uP_PCC_nCE2	Input
65	uP_PCC_nOE	Input
66	uP_PCC_nIORD	Input
73	PCC_VS1	Input
80	PCC_nIOIS16	Input
82	uP_PCC_nSLOT1	Input
85	uP_PCC_nSLOT2	Input
86	PCC_nCE1B	Output
22	uP_nRD	Input
27	uP_nMWE0	Input
87	PCC_nCE2B	Output
55	LCD_VEEEN	Output
7	BUFF_nOE	Output
93	MFP20 – PCC_nCE1A	Output
8	BUFF_DIR_DATA	Output
78	WRLAN_nIOWR	Output
79	WRLAN_nIORD	Output
81	nIOWR	Output
89	nIORD	Output
90	BALE	Output
95	MFP22 – PCC_nCE2A	Output
91	nAEN	Output
99	MSTR_nRST	Input
92	CF_nCE	Output
36	uP_WAKEUP	Output
96	PCC_nDRV	Output
49	uP_USB1_PWR_EN	Output
50	uP_USB1_nOVR_CRNT	Output
45	CPLD_TDI	JTAG
47	CPLD_TMS	JTAG
48	CPLD_TCK	JTAG
83	CPLD_TDO	JTAG
57, 26	VCC	VCORE
38, 51, 20, 88, 98	VCCIO	3.3V
21,25,31,62,69,75,84,100	GND	GND
38, 51, 20, 88, 98	VCCIO	3.3V
21,25,31,62,69,75,84,100	GND	GND

