LH7A400-10
Card Engine

NOVO

LOGIC

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CARD ENGINE REV	APPROVAL	DATE
1	Paul Mueller	- First Draft Version	-	PGM	4/18/03
2	Charles Eddleston	- Initial Release	-	KTL	6/5/03
A	Charles Eddleston	- Production Release	-	KTL	6/16/03
B	Charles Eddleston	- Pin error corrections: J1C connector, J1B connector - Both the nCHRDY and uP_PCC_nCD1 signals changed to "3.3V." - CPLD_TCK changed to "pulled down through a 10K resistor to digital GND" - JTAG Important Notice inserted	-	JW	9/01/03
C	James Wicks	- Updated Figures 3.2, 3.3, 3.4, 4.1, and 4.2	-	KTL	9/17/03
D	James Wicks	- Added mode line description note	-	JW	9/19/03
E	James Wicks	- Section 4.2.1 Edit	-	JW	11/05/03
F	James Wicks Michael Anderson	- Changed "Interface Spec" to "IO Controller Spec" - Updated Product Brief Section;	-	JW	1/27/04
G	Kurt Larson	- Unused Pin Connector Description	B	KTL	2/10/04
H	Michael Aanenson	- IRQA,B,C interrupt pin descriptions changed to multiplexed GPIO instead of GPI - Added LH7A400 GPIO descriptions to pins that can be set up as GPIO on the processor - Removed IRQD from Multi Function Pin Table - Added GPIO group numbers into Multiplexing table - Changed references to Altera CPLD to Xilinx CPLD - Updated IO Controller memory map	B	HAR	2/20/04
I	Michael Aanenson Erik Reynolds	- Updated Multiplexed Signal Trade-Off table to correct errors with the listed signals and what LH7A400 GPIO port pins they went to. - Updated power tables in sec 1.7.1.1 - Updated document for the release of Card Engines Revision C and D. - Changed the 'Unused Treatment' for the uP_USB1_OVR_CRNT to 'leave floating'. It had been 'Use a 10k or 100k Pull Down'. If a design has a 10k or 100k pull down resistor on this signal, it will not affect operation.	C, D	ECR	3/24/04
J	James Wicks Michael Aanenson	- Correction: Section 5.4.3, Pin 62 changed from Port H Bit 7 to Port F Bit 7. - Correction: Section 5.4.4, Pin 14 changed from Port H Bit 6 to Port F Bit 6. - Correction: Section 5.1, changed pin description of uP_MODE0 pin (J1C pin 44) to default low. - Correction: CPLD_GPIO_1, CPLD_GPIO_2, uP_STATUS_1, and uP_STATUS_2: open drain info. added (this change also applicable for Rev B Card Engines)	C, D	HAR	12/06/04

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC PN & REV	APPROVAL	DATE
K	Michael Aanenson Jed Anderson	- Revision History Table: Changed "Card Engine Rev" category to "Schematic PN & Rev" - Removed Section 1.4 "Card Engine Advantages" - Section 1.6.1.1: Updated Core Supply Voltage Min and Max - Section 1.6.1.1: Added 1.8V power supply note - Section 2.7: Updated link to Intel website - Section 5.2: Corrected J1A pin #67 signal name "uP_USB1_nOVR_CRNT" - Section 5.4.3: Pin #62, fixed 'Optional Configuration' column to be PF7 instead of PH7 - Section 5.4.4: Pin #14, fixed 'Optional Configuration' column to be PF6 instead of PH6 - Section 7.1: Corrected Hirose PNs to reflect available parts - Section 7.1: Added Important Note - General formatting and grammatical changes throughout	80000126 Rev D01	MAA	05/04/07

Please check http://www.logicpd.com/auth/downloads/LH7A400/ for the latest revision of this manual, product change notifications, and additional application notes.

Table of Contents

Table of Figures

LH7A400 CARD ENGINE

CARD ENGINE ADVANTAGE

- Reduce Time to Market
  → 6 to 9 month savings
- Product-Ready Hardware Platform
- Production Quality Software
- Engineering Support

PRODUCT HIGHLIGHTS

- Ready-to-Run Windows® CE BSP
  Bootloader/Monitor
- Board Support Packages
- Custom Linux or Windows CE
- Device Driver Development

ORDERING INFORMATION

- Zoom™ Starter Development Kit
  (Model # SDK-LH7A400-10-6416)

CUSTOMER SUPPORT

Logic provides technical support for Application Development Kits. Various support packages are available; contact us for more information.

CONTACT

For more information on our Embedded Product Solutions, please contact Logic Sales at www.logicpd.com or 612.672.9495.

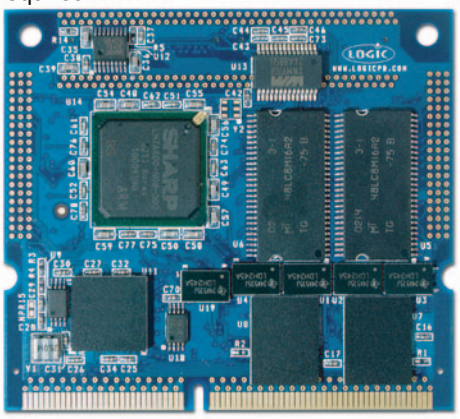
SHARP

BLUE TREAK
Powering Tomorrow's Vision

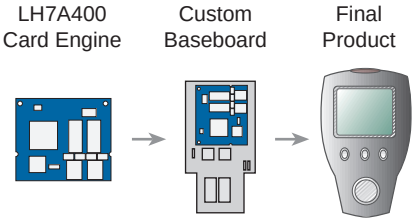
Microsoft® Windows® Embedded Partner
Gold-level Member

The LH7A400 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The use of custom application/peripheral boards make the Card Engine the ideal foundation for OEMs developing embedded computing products. The Card Engine includes BSPs that integrate seamlessly with OS development tools. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily migrate to next generation microprocessors and technology, when new functionality or performance is required.



Actual Size (2.37" x 2.67")



- **Processor** Sharp LH7A400 32-bit ARM922TDMI RISC microprocessor
  - Running up to 200 MHz (0 to 70 Degrees C) with 100 MHz bus speed
  - Running up to 166 MHZ (-40 to 85 Degrees C) with 83 MHz bus speed
- **SDRAM Memory** 32 or 64 MBytes
- **Flash Memory** NOR or NAND
  - 0, 16, or 32 Mbytes NOR
  - 0, 64, or 128 Mbytes NAND
- **Display** Programmable color LCD controller
  - Built-in driver supports up to 800 x 600 x 16-bit color (1024 x 768 x 8-bit color)
  - Supports STN, Color STN, HR-TFT, AD-TFT, TFT
- **Touch Screen** Four wire resistive touch controller (ADS7843)
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN 91C111 (MAC & PHY)
- **Audio** Audio codec (Wolfson WM9708)
- **Memory Card Expansion**
  - CompactFlash Type 1 card (memory-mode only)
  - PCMCIA of CF (2 slots)
  - Smart Card Interface (ISO7816)
  - MMC
- **USB** One device interface (USB 2.0 Full Speed)
- **Serial Ports** Three 16C550-like, standard UARTs
- **IrDA** SIR supports up to 115.2 Kbps
- **GPIO** Programmable depending on peripheral requirements
- **SPI**
- **Real TIme Clock**
- **Software**
  - BSPs: Windows CE, Linux[1], VxWorks[1]
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37" (60.2 mm) long x 2.67" (67.8 mm) wide x 0.17" (4.4 mm) high
  - 144 pin SODIMM Connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit

[1] *Third Party ports available from Sharp*

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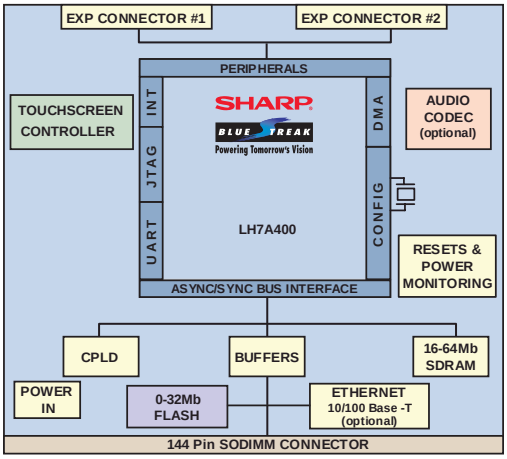
PN: 70000028 Rev G

LH7A400 CARD ENGINE

System on Module Block Diagram



Actual size (60.2mm x 67.8 mm)

The Card Engine CPLD provides the following functionality:

- CF Card Support (memory mode only)
- ISA-like bus interface
- SMSC LAN91C111 wired LAN bus interface and power control logic
- Buffer control logic
- Chip select decoder logic
- Flash program control logic
- Processor mode control logic
- IC code revision register
- PCMCIA Support logic

The CPLD code is available free of charge for customers designing the Card Engine into their final product or for purchase if implementing in a custom board solution.

Please contact Logic Sales at product.sales@logicpd.com for more information.

Standard System on Module Configuration

Logic Model Number	SDRAM (MB)	NOR Flash (MB)	NAND Flash (MB)	Ethernet	Audio	Touch	Temp. Rating
CENGLH7A400-10-503HC(R)	64	16	0	Y	Y	Y	0 to 70 deg C
CENGLH7A400-10-504HC(R)	64	32	0	Y	Y	Y	0 to 70 deg C

(R) An R in the model number denotes a RoHS compliant configuration.
**Please contact Logic for custom configurations and availability.*

System on Module Advantage: Less time, less cost, less risk ... More Innovation

Zoom™ Starter Development Kit (SDK)

SDKs simplify:
- *Application specific code development*
- *Evaluation of the MCU / System on Module*
- *The transfer of application code, OS and BSPs into production*

Card Engine (with common footprint)

Card Engine complete with:
- *Board Support Packages (Windows CE, Linux, and other RTOS)*
- *Bootloader provides in-field device management, manufacturing, and test capabilities*

Custom Baseboard (with Card Engine)

Baseboard provides:
- *Power*
- *Connectors*
- *Custom peripherals*
- *Custom form factor*

Final Product

Final Product results:
- *Accelerated time to market*
- *Reduced development cost*
- *Customer focuses on core competencies*

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PN: 70000028 Rev G

1.2 Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I²S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MMC	Multimedia Card
NC	No Connect
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System on Chip
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

- LH7A400-10 Card Engine IO Controller Specification
- LogicLoader™ User's Manual
- LH7A400 Universal Microcontroller User's Guide
- Xilinx XC2C128 CPLD data sheet
- Texas Instruments (Burr-Brown) ADS7843 data sheet
- Wolfson WM9708 AC'97 Audio CODEC data sheet

1.4 Card Engine Interface

Logic's common Card Engine interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common Card Engine footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

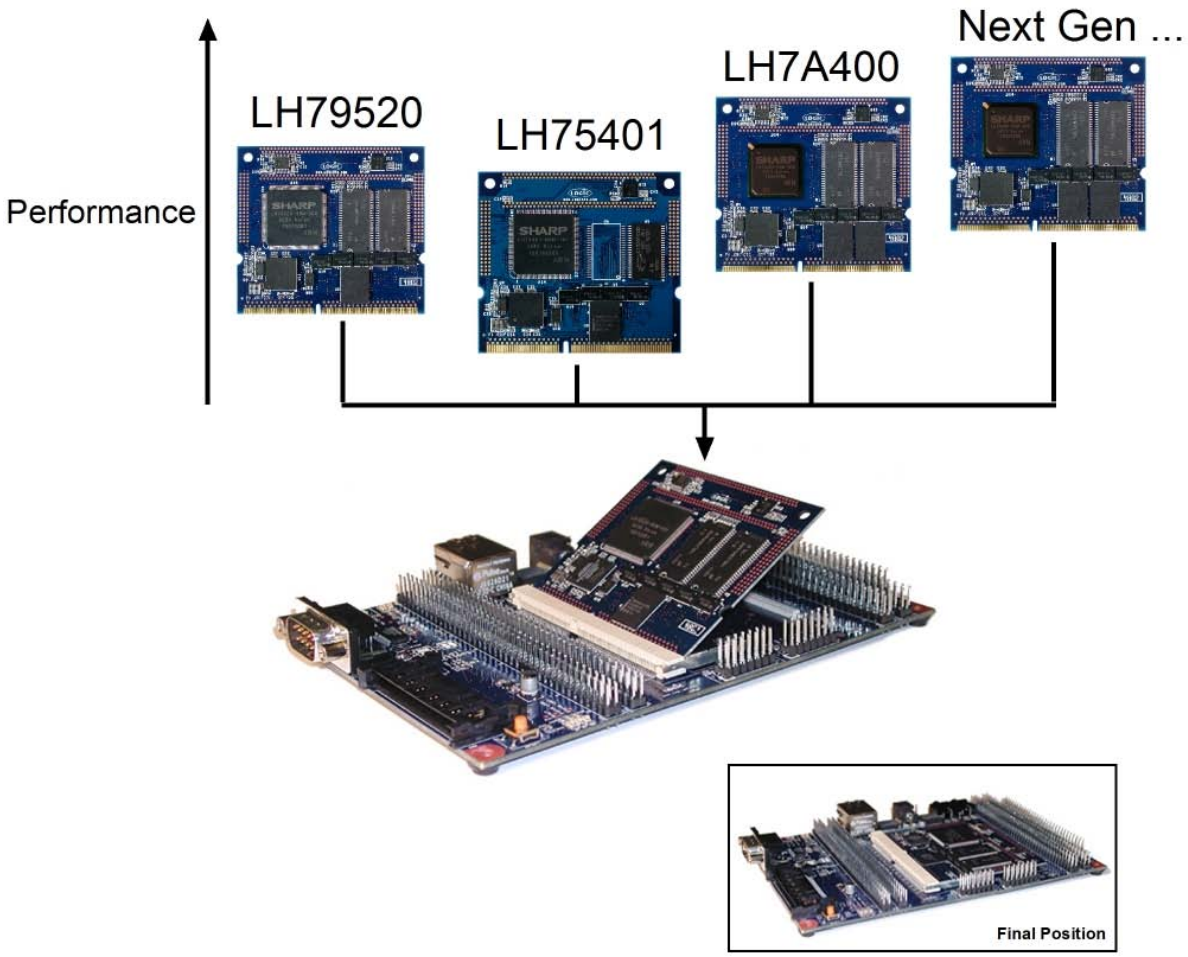

Figure 1.1: Card Engine Advantages

In fact, encapsulating a significant amount of your design onto the Card Engine reduces any long-term risk of obsolescence. If a component on the Card Engine design becomes obsolete, Logic will simply design for alternative part that is transparent to your product. Furthermore, Logic tests all Card Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

1.5 LH7A400-10 Card Engine Block Diagram

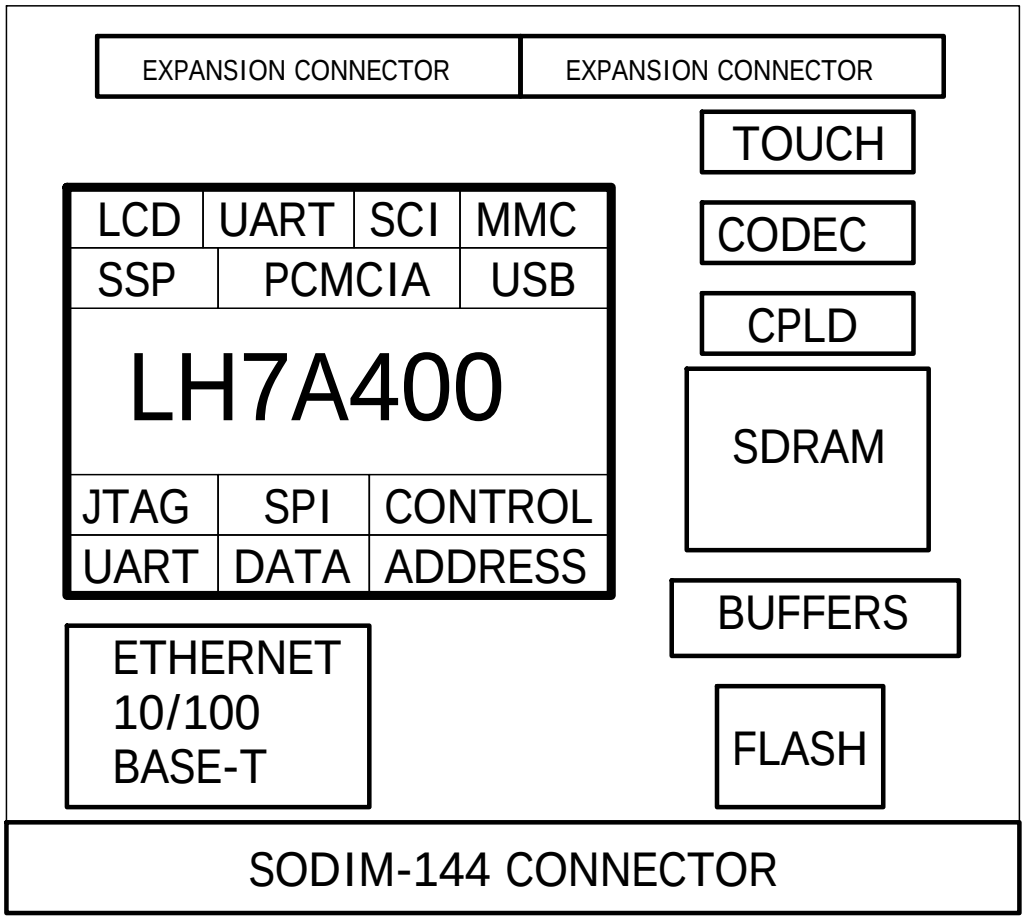

Figure 1.2: LH7A400-10 Card Engine Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC IO and Peripheral Supply Voltage	3.3V	-0.3 to 3.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.4	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.6.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.60	V	1
DC IO Supply Active Current	Note 4	234	275	mA	4
DC IO Supply Standby Current	Note 4	—	—	mA	4
DC IO Supply Sleep Current	Note 4	—	—	mA	4
DC Core Supply Voltage	1.71	1.8	1.89	V	1
DC Core Supply Active Current	Note 4	68	160	mA	4
DC Core Supply Standby Current	Note 4	—	—	mA	4
DC Core Supply Sleep Current	Note 4	0	—	mA	4
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions	—	2.35 x 2.6	—	Inches	
Weight	—	17	—	Grams	4
Connector Insertion/removal	—	50	—	Cycles	
Input signal High Voltage	—	2.0	—	V	
Input Signal Low Voltage	—	0.8	—	V	
Output Signal High Voltage	2.6	—	VIO	V	
Output Signal Low Voltage	GND	—	0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. This test was performed with the 91C111 chip power disabled.
3. Contact Logic for more information on an industrial temperature LH7A400-10 Card Engine
4. May vary depending on Card Engine configuration.

NOTE: Sharp recommends that the 1.8V power supply be energized before the 3.3V supply. If this is not possible, the 1.8V supply may not lag the 3.3V supply by more than 100 microseconds. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5V during power supply ramp up.

2 Electrical Specification

2.1 Microcontroller

2.1.1 LH7A400 Microcontroller

The LH7A400-10 Card Engine uses Sharp's highly integrated system on a chip LH7A400 microcontroller. Sharp's LH7A400 has a 32-bit ARM922T RISC core. Sharp's LH7A400 microcontroller is a system on a chip providing many integrated on-chip peripherals including:

Integrated ARM922T™ core
- 32-bit ARM922T™ RISC core
- 16kB cache: 8kB instruction cache and
- 8kB data cache
- MMU
- 4 GB logical address space

80 KB on-chip SDRAM
Integrated LCD controller
- Up to 800 x 600 resolution at 16-bit color
- (1024 x 786 at 8-bit color)
- Supports STN, TFT, and HR-TFT
- Up to 64,000 Colors

Three UARTs
Classic IrDA (up to 115.2 Kbps)
SPI
AC97 CODEC interface
USB client interface (USB 1.1)
MultiMediaCard / Secure Digital interface
Smart Card interface (ISO7816)
Smart battery monitor interface
Up to 60 General Purpose I/O Signals
Two 16-bit Pulse Width Modulators
- Ten DMA channels (used for: USB, MMC, and AC97)

Three programmable timers
RTC
Low power modes
5 volt tolerant inputs

See Sharp's LH7A400 Universal Microcontroller User's Guide for additional information.
http://www.sharpsma.com/

IMPORTANT NOTE: Please see http://www.sharpsma.com/ for any errata on the LH7A400.

2.1.2 LH7A400 Microcontroller Block Diagram

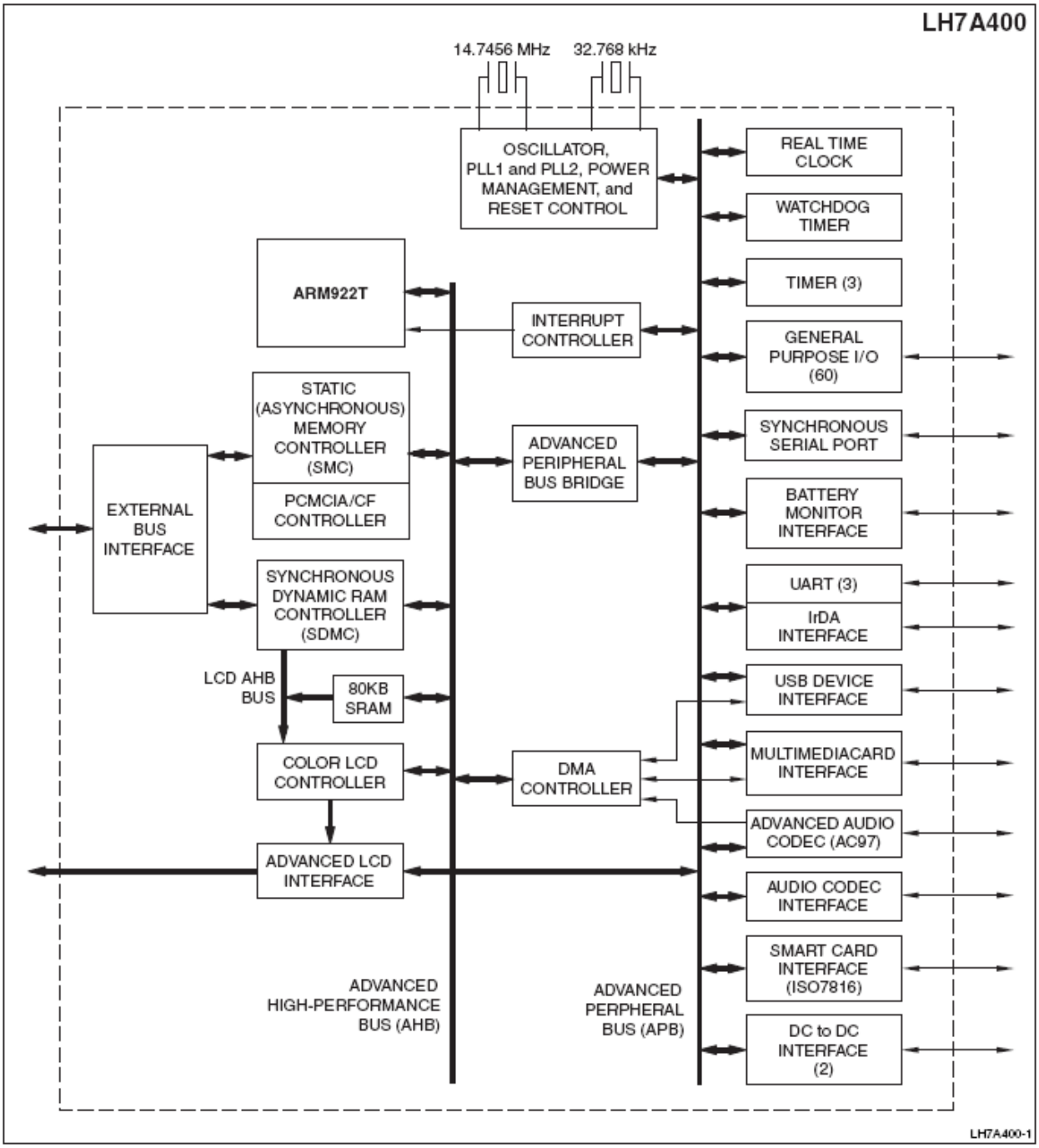

Figure 2.1: LH7A400 Microcontroller Block Diagram

2.2 Clocks

The LH7A400 requires two crystals in order to have proper internal timing. The first is a 14.7456 MHz crystal, which is used to generate many of the processors internal clocks through a series of dividers. The crystal signal, for example, is run through a PLL—the divisor being specified in the Clock Set register—to generate the FCLK signal. FCLK is then used internally as the Synchronous Bus Mode core clocking for the ARM922T core and cache. The 14.7456 MHz crystal is also used to create the HCLK, HCLK_CPU, PCLK, and peripheral clock signals. One such peripheral clock is set up through a second PLL to produce a 48.0 MHz clock for USB operations. One more signal stemming from the 14.7456 MHz crystal input is the uP_AUX_CLK signal, which is produced through a programmable divider on the Card Engine. The uP_AUX_CLK is provided on the 144-pin SODIMM expansion connector as the LH7A400 CLKOUT, and is set to a default of 14.7456 MHz.

The second required crystal runs at 32.768 kHz and is the only permanently running clock in the LH7A400, using a ripple divider to conserve power. This divider produces the 1 Hz signal for the RTC interface as well as intermediate frequencies of 16 kHz and 8 kHz for the state controller and PLL interlocks.

The LH7A400 is able to operate in either asynchronous, synchronous, or FastBus extension clocking modes. Choosing between these three modes depends on the desired application as each has certain advantages or disadvantages in system throughput and power consumption.

IMPORTANT NOTE: Please see Sharp's LH7A400 Universal Microcontroller User's Guide for additional information about the Standard Bus Clocking Modes and the relation between FCLK and HCLK.

The LH7A400's microcontroller core clock speed is initialized to 200 MHz on the Card Engine and the Bus speed is set at 100 MHz in the LogicLoader. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH7A400-10 Card Engine provides an external Bus clock, uP_BUS_CLK, on the 144-pin SODIMM connector. The uP_BUS_CLK, which is connected to the processor's SCLK, is set to a default of 100 MHz. SCLK also serves as the SDRAM and CPLD clock on the LH7A400-10 Card Engine.

LH7A400 Microcontroller Signal Name	LH7A400-10 Card Engine Net Name	Default Software Value in LogicLoader
FCLK	N/A	200 MHz
HCLK	N/A	100 MHz
SCLK	uP_BUS_CLK	100 MHz
PGMCLK	uP_AUX_CLK	14.7456 MHz

2.3 Memory

2.3.1 Synchronous DRAM

The LH7A400-10 Card Engine uses a 32-bit memory bus to interface to SDRAM. The memory can be configured as 16, 32, or 64 MB to meet the user's memory requirements and cost constraints. Logic's default memory configuration on both the SDK boards is specified as 32 MB.

2.3.2 Direct Memory Access (DMA)

Although the Sharp LH7A400 microcontroller has an internal DMA controller, it offers no external DMA channels. The 10 internal channels are all occupied by the USB, MMC, and AC97 controllers. If an external DMA channel is required, please contact Logic Product Development.

2.3.3 NOR flash

The LH7A400-10 Card Engine uses a 32-bit memory bus (split into 2, 16-bit channels, one to each flash memory) to interface to Intel StrataFlash memory chips. The onboard Card Engine memory can be configured as 8, 16, or 32 MB to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 16 MB on the SDK and 32 MB on the IDK. Because flash is one of the most expensive components on the LH7A400-10 Card Engine, it is important to contact Logic when determining the necessary flash size.

It is possible to expand the system's non-volatile storage capability by adding external flash IC's, CompactFlash, or NAND flash. See the LH7A400-10 Application Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 CompactFlash (memory-mapped mode only)

The LH7A400_10 Card Engine supports a CompactFlash memory mapped mode only slot that compliments the processor's standard dual PC card support. The LH7A400_10 Card Engine uses the CPLD to provide the necessary signals for a CompactFlash card interface in memory mapped mode only. The Zoom™ Starter Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. If hot swapping capability is desired, it can be achieved by using additional hardware on the user's base board. See the LH7A400-10_IO_Controller_Spec document for further details on the use of the memory-mapped CompactFlash interface.

IMPORTANT NOTE: The CPLD CompactFlash interface supports memory-mapped mode only. Use the LH7A400 processor's PC card slots for more PC card mode options.

2.4 MultiMediaCard (MMC)

The LH7A400-10 Card Engine provides one MMC controller that is compliant with all MCC System Specifications up to and including v3.2. This controller supports MMC-specific functions, acts as a host, and implements the standard MMC interface (SPI mode is not used). For more detailed operation and programming operations see the MultiMediaCard Association System Specification, available at www.mmca.org.

2.5 PCMCIA/CompactFlash (external)

Both PCMCIA and CF devices are externally supported on the LH7A400 Card Engine. To handle these devices, the static memory controller has allocated two of the eight configurable memory banks for PCMCIA and CF interfaces. The Card Engine can directly support one PCMCIA/CompactFlash card and has the capability to interface to two cards with minimal external circuitry. Please refer to the IDK kit for an example implementation. In order to properly take advantage of these features software parameters need to be set; see the "Static Memory Controller" section in the LH7A400 Amended User's Guide for more information.

2.6 10/100 Ethernet Controller

The LH7A400-10 Card Engine uses the SMSC 91C111 10/100 single chip Ethernet Controller to provide an easy-to-use interface. To facilitate use, six signals from the 91C111 are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LEDs. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides example circuit schematics in the LH7A400-10 Application Kit for reference.

IMPORTANT NOTE: The ENEEP signal on the SMSC 91C111 is connected to a zero ohm resistor that is not populated. This is because the ENEEP signal has a weak internal pull-up in the SMSC 91C111and if the signal is tied low it low will disable the serial EEPROM interface.

2.7 Audio CODEC

The LH7A400 processor has an internal AC97 controller that is compliant with the Audio CODEC '97 Component Specification, v2.2. This AC97 Controller implements a 5-pin serial interface to the AC97 Audio CODEC, in this case the Wolfson WM9708. From the Wolfson CODEC on the LH7A400-10 Card Engine there are 3 outputs, CODEC_OUTL, CODEC_OUTR, and MFP34 – MONO_OUT. All of these signals are available from the 80-pin expansion connectors.

NOTE: More information about the Intel AC97 standard is available on Intel's website at http://www.intel.com/design/chipsets/hdaudio.htm.

The Wolfson CODEC on the LH7A400 Card Engine performs full duplex 18-bit CODEC functions and supports variable sample rates from 8-48k samples/second. The Wolfson chip also has an onboard 24.576 MHz crystal which is used for the AC'97 master clock frequency.

If you are looking for a different CODEC option, Logic has previously interfaced different high performance audio CODECs into other Card Engines. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

2.8 Video Interface

Sharp's LH7A400 microcontroller has a built in LCD controller supporting STN, TFT, and HR-TFT panels at up to 800 x 600 x 16-bit or 1024 x 768 x 8-bit color resolution. See the LH7A400 Universal Microcontroller User's Guide for further information on the integrated LCD controller. The signals from the LH7A400's LCD controller are organized by bit and color and can all be interfaced through the J1A expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.9 Serial Interface

The LH7A400-10 Card Engine comes with the following serial channels: UARTA, UARTB, UARTC and SSP. If additional serial channels are required, please contact Logic for reference designs. UARTC supports both wired serial and infrared communications, supporting a digital encoded output and decoded input without analog processing.

2.9.1 UARTA

UARTA has been configured to be the LH7A400-10 development kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the SDK and IDK kits. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2K bits/sec, though it supports all common serial baud rates from 2.4kbps to 460.8kbps. UARTA is available off the 144-pin SODIMM connector. Please see the LH7A400 Universal Microcontroller User's Guide for further information.

2.9.2 UARTB

Serial Port UARTB has dual functionality, its primary function is as an asynchronous 16C550 compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user is responsible for providing an external RS232 transceiver for

RS232 applications. UARTB's baud rate can also be set to all common serial baud rates from 2.4kbps to 460.8kbps.

The UARTB pins are multiplexed with GPIO Ports B1-B5 and when UARTB is not in use, the GPIO pins can be used instead. UARTB is available off the J1B 80-pin expansion connector.

2.9.3 UARTC

Like UARTA and UARTB, UARTC supports serial communications. Unlike the previous UARTs, however, UARTC also supports the serial infrared communication protocol. When functioning as a serial port, UARTC will perform many of the characteristics as discussed above, except that UARTC does not have any status signals. If status signals are desired, it is necessary to map these control signals to GPIO ports.

In order to define UARTC's functionality, a programmable register is available to specify infrared or serial operation. Once a communication mode is chosen, the pins for the other connection are ignored, and vice-versa. The pins used for UARTC's IrDA functions are uP_IRTX and uP_IRRX and for UARTC's UART functions are uP_UARTC_RX and uP_UARTC_TX (serial). These signals are available on the J1B 80-pin expansion connector. UARTC's serial transmit and receive pins, are multiplexed with GPIO Ports B0 and C0 and are available for GPIO use when not employed as a UART interface.

Please see Sharp's LH7A400 Universal Microcontroller User's Guide for more information on using infrared communications.

2.9.4 SSP/SPI

The SSP interface on the LH7A400 Card Engine supports three data frame formats:
- Texas Instruments' SSI
- Motorola SPI
- National Semiconductor Microwire

By default, Logic has chosen to implement Motorola's SPI interface, although the other 2 options are made available by programming the Control Register 0's 2-bit Frame Format field. The SPI format is used to interface between the parallel data inside the SoC and synchronous serial communications on slave peripheral devices. The SPI interface is master-only, with programmable clock rate and pre-scale options that are used to generate the appropriate bit-rate and Serial Clock output. The Data Size Specification is also configurable, and as such the SPI port can receive or transport anywhere from 4 to 16 bits. The SPI signals are available off the 144-pin SODIMM connector. Please see the LH7A400 Universal Microcontroller User's Guide for further information.

2.10 USB Interface

The LH7A400 Card Engine is configured with one available USB device interface and is fully compliant with the USB 1.1, OpenHCI, and Intel UHCI specifications. This USB client supports full-speed (12M bits/sec) operation and both suspend and resume signaling. The USB device interface on the LH7A400 is able to transmit, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector. Please see the LH7A400 Universal Microcontroller User's Guide for further information on how to properly use these features.

IMPORTANT NOTE: In order for USB to be correctly implemented on the LH7A400 Card Engine, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 1.1 requirements specify that the impedance on each driver must be between 28Ω and 44Ω. For reference, see the impedance matching circuit on the Logic SDK or IDK board.

2.11 Touch Interface

The LH7A400-10 Card Engine implements the popular TI ADS7843 12-bit sampling ADC touch controller, supporting standard 4-wire resistive touch panels. The touch controller operates through the CPLD, which provides a parallel to SPI interface that connects to the LH7A400 microcontroller. In this case, SPI is used because many of Logic's customers take advantage of the on-chip SPI port for their applications. Logic, therefore, designs Card Engines to keep the serial channels free for user functions. Please see the LH7A400-10 Card Engine CPLD Interface and ADS7843 specifications for more information.

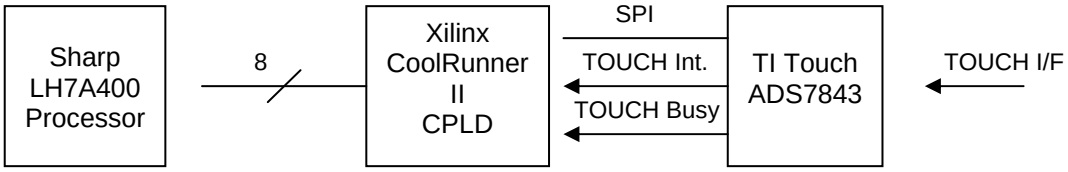

Figure 2.2: Touch Controller Block Diagram

2.12 General Purpose Analog & Digital I/O

Logic designed the LH7A400-10 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Card Engine that interface to the LH7A400, and the Xilinx CPLD. Some of these GPIO pins are interrupt capable while other signals are input or output only. Please see the Pin Descriptions section of this data sheet. The LH7A400 microcontroller does not contain an internal Analog to Digital Converter (ADC); however, the ADS7843 Touch Chip provides 2 analog inputs available off of the J1A expansion connector. Logic's LH7A400-10 IO Controller Specification provides the necessary information to interface to the touch controller. If certain peripherals are not desired, such as the LCD Controller, Chip Selects, IRQs, UARTS, AC97, PCMCIA and CompactFlash, Smart Card Interface, or BMI interface, then multiple GPIO pins become available. Please see the table in section 5.4 Multiplexed Signal Trade-Offs for a list of the available GPIO trade-offs.

2.13 CPLD

Please see the LH7A400-10_IO_Controller_Spec document for CPLD information.

2.14 Serial EEPROM Interface

Logic designed the LH7A400-10 Card Engine to have a low-cost 1 kb serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the LH7A400 microcontroller via the CPLD through an SPI interface – discussed in the touch screen controller section above. See Figure 2.3 below. For more information please view the LH7A400-10 IO Controller Specification.

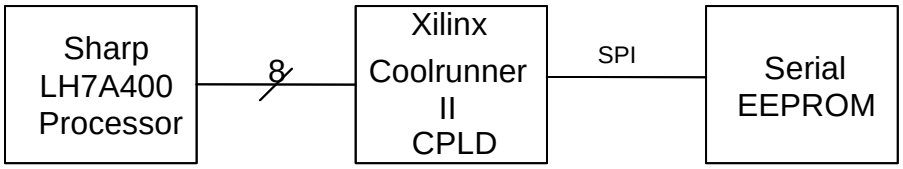

Figure 2.3: Serial EEPROM Block Diagram

2.15 Expansion Options

The LH7A400-10 Card Engine was designed for expansion, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the 144-pin SODIMM connector and two 80-pin expansion connectors. See the LH7A400-10 Card Engine schematics for more detail. A user may expand the Card Engine's functionality by adding PCI or ISA devices. Logic has used other audio CODECs, Ethernet ICs, co-processors, and components on the Card Engine boards in the past. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The LH7A400-10 Card Engine was designed to meet multiple applications for specific users and budget requirements. As a result, this Card Engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Flexible RAM footprint: 16, 32, or 64 MB SDRAM
- Flexible flash footprint: 8, 16, or 32 MB StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional Wolfson WM9708 Audio CODEC
- Optional TI ADS7843 Touch Controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all Card Engine peripheral hardware reset pins are connected to either the MSTR_nRST net or to the RESET_HIGH net as shown in the figure below. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the LH7A400-10 Card Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems.

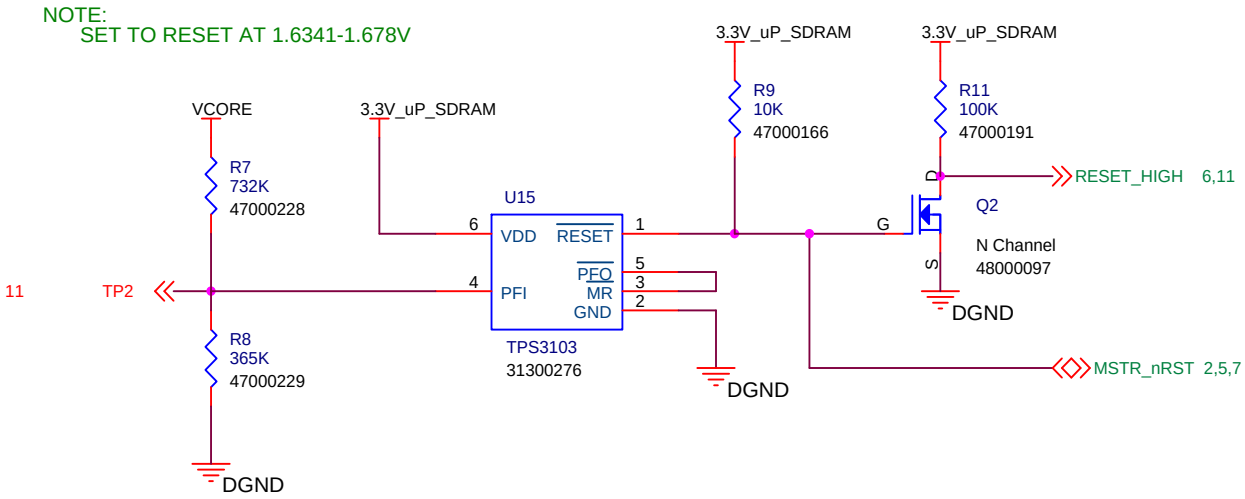

Figure 3.1: Reset Circuit

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal. The RESET_HIGH signal, on the other hand, is the active high output of the reset circuit and is not provided as part of the Card Engine connector interface.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will

cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details.

There are three conditions that will cause a system-wide reset: power-on, a low pulse on the MSTR_nRST signal, and the power fail comparator input (PFI pin) falling below the internal comparator threshold.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 2.941V. Once the 3.3V_uP_SDRAM supply surpasses 2.941V the reset chip will trigger a rising edge of MSTR_nRST after a 65-195ms delay (130ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that any external assertion source that triggers the MSTR_nRST signal, analog, or digital de-bouncing be used to generate a clean one shot reset signal.

Power Fail:
If the power fail comparator input pin (PFI pin) falls below the internal comparator threshold of 0.551V, it will create a low pulse on the MR input pin of the reset chip. The low assertion of the MR pin will assert the MSTR_nRST signal and will hold it low after the MR pin is de-asserted (PFI is above the comparator level and power is restored) for 65 to 195 ms (130 ms typical). Please see the TI TPS3103 data sheet at http://www.ti.com for additional details on reset timing and thresholds.

3.2.2 Soft Reset

Logic has created a soft reset signal, SW_nRESET, to be used as a reset for the LH7A400’s internal registers without affecting the peripherals on the rest of the board or the data stored in SDRAM. The data is saved because the SDRAM controller automatically places the SDRAM in self-refresh before the uP_SD_CLK clock is disabled. As in the Standby state described in section 3.5.4.2, the 32.768 kHz clock continues running, allowing the system to properly wake up. The SW_nRESET signal is an input to the LH7A400 processor’s user reset input pin.

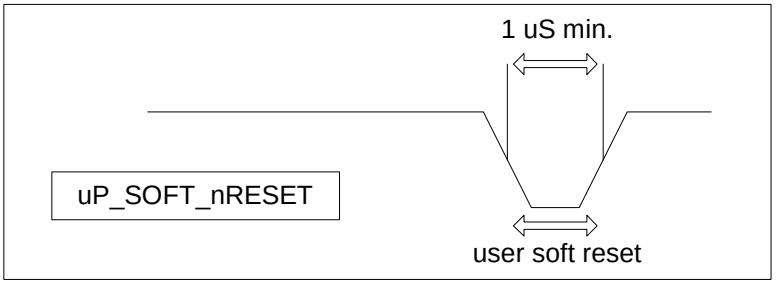

Figure 3.2: Soft Reset

See Sharp’s LH7A400 Universal Microcontroller User’s Guide for additional information on register conditions after a soft (manual) reset.

3.3 Interrupts

The LH7A400 Interrupt Controller collects interrupt request signals from on-chip and off-chip sources and processes the interrupt requests into an IRQ signal and an FIQ signal to the ARM922T core. The LH7A400 processor accepts inputs from 28 interrupt sources, and on the LH7A400 Card Engine, 4 sources are available to configure externally: ports F0-F3 and F4-F5 (F6-F7 are used internally). Table 3.3 shows a detailed list of the interrupt priorities for the LH7A400 processor – interrupts from enabled sources 4 through 27 request an IRQ exception (lower priority), whereas interrupts 3 through 0 request an FIQ exception (higher priority). If two interrupts with the same priority become active at the same time, the priority must be resolved in software. By default, the LH7A400-10 Card Engine interrupts are set to trigger on a LOW level and are pulled up to 3.3V_uP_SDRAM by 10k resistors. Refer to Sharp's LH7A400 Universal Microcontroller User's Guide for further information on using IRQ and FIQ interrupts.

BITS	NAME	INTERRUPT SOURCE
31-28	///	Reserved: Reading returns 0. Values written cannot be read.
27	BMIINTR	Battery Monitor Interface (BMI)
26	GPIO7INTR	Configurable External IRQ Interrupt on the GPIO Port F7 pin (GPIO)
25	GPIO6INTR	Configurable External IRQ Interrupt on the GPIO Port F6 pin (GPIO)
24	GPIO5INTR	Configurable External IRQ Interrupt on the GPIO Port F5 pin (GPIO)
23	GPIO4INTR	Configurable External IRQ Interrupt on the GPIO Port F4 pin (GPIO)
22	TC301	Timer3 (Timers)
21	DMAINTR	Direct Memory Access (DMA)
20	USBINTR	Universal Serial Bus (USB)
19	MMCINTR	MultiMedia Card (MMC)
18	AACINTR	AC97 Audio CODEC (AAC)
17	SCIINTR	Smart Card Interface (SCI)
16	UART3INTR	UART3 (UART)
15	SSEOTI	Synchronous Serial Interface (SSI)
14	LCDINTR	Liquid Crystal Display (LCD)
13	UART2INTR	UART2 (UART)
12	UART1INTR	UART1 (UART)
11	TINTR	64 Hz Tick (CSC)
10	RTCMI	Real Time Clock (RTC)
9	TC201	Timer2 (Timers)
8	TC101	Timer1 (Timers)
7	GPIO3INTR	Configurable External IRQ Interrupt on the GPIO Port F3 pin (GPIO)
6	GPIO2INTR	Configurable External IRQ Interrupt on the GPIO Port F2 pin (GPIO)
5	GPIO1INTR	Configurable External IRQ Interrupt on the GPIO Port F1 pin (GPIO)
4	CSINT	Audio CODEC (ACI)
3	MCINT	Media Change: This FIQ interrupt occurs at least 62.5 µs after a rising edge on the MEDCHG input pin (CSC).
2	WEINT	Watchdog Timer: This FIQ interrupt (WDT) occurs when the WDT overflows.
1	BLINT	Battery Low: This FIQ interrupt occurs at least 62.5 µs after the following signal combination has begun, and remains asserted while these conditions exist: NEXTPWR is HIGH, indicating no external power supply BATOK is LOW (CSC)
0	GPIO0FIQ	GPIO External Interrupt: Configurable External FIQ Interrupt on the GPIO Port F0 pin (GPIO)

Figure 3.3: Interrupt Priorities

IMPORTANT NOTE: For information on the use of the CPLD interrupt signal (PF7 on Rev A and earlier, PF3 on Rev B and later), uP_CPLD_nIRQ, see the LH7A400-10 IO Controller Specification (LH7A400-10_IO_Controller_Spec.doc).

3.4 JTAG Debugger Interface

The JTAG connection on the LH7A400 allows recovery of corrupted flash memory and real time applications debug. When choosing a debugger board, remember that many different third-party JTAG debuggers are available for Sharp ARM microcontrollers. The following signals make up the JTAG interface to the LH7A400: uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 20-pin 0.1" through-hole connector as demonstrated in the Sharp LH7A400 Universal Microcontroller User's Guide, or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20-pin connector out, realize that it may not be numbered as a standard 20-pin 0.1" IDC through-hole connector. See LH7A400-10 Card Engine Application Kit reference design for further details. Different IC manufacturers define the 20-pin IDC connector pin-out differently.

IMPORTANT NOTE ON USING JTAG: The Sharp LH7A400 processor requires a rising edge on the processor wake-up signal to bring the processor from Cold Boot state to Run state. Therefore, in order to use JTAG operation on the LH7A400-10 Card Engine, one must consult their JTAG manufacturer to find when the JTAG device requires the processor to be in the Run state. If the JTAG device issues a reset to the processor, then the wake-up signal must transition from low to high to return to the Run state before the JTAG debugger may connect. The JTAG device may be able to connect to the processor while it is in Standby state, but will not be able to do anything that requires processor functioning until woken.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the LH7A400-10 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, 3.3V_WRLAN, and VCORE. All power areas are inputs to the Card Engine with the exception of 3.3V_WRLAN, which is an output from the Card Engine.

3.5.1.1 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins are connected to a 3.3V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in this section below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the LH7A400-10 Card Engine. This supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the LH7A400 processor on the LH7A400-10 Card Engine. The 3.3VA supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions. The analog power pins on the LH7A400 are connected to the VCORE voltage with low-pass filtering.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This “power” supply net is an output from the Card Engine and is controlled through a registered bit in the on-board CPLD. For more details on this specific control bit, see the “LH7A400-10 IO Controller Specification” manual for specific details. Logic’s software BSP asserts this signal in order to properly manage power in the LAN91C111 Ethernet chip. However, this management does not put the part in a low enough power state for many applications.

The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the Card Engine will try to power itself through the impedance matching resistors. Please see Logic’s schematics for the SDK or IDK reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the Card Engine is to power the 91C111 chip separately and allow for complete, but independent shut down. Furthermore, the 3.3V_WRLAN output from the Card Engine is required to completely isolate the LAN circuit so that it is not back powered through the impedance matching resistors.

3.5.1.5 VCORE

The VCORE input pins are connected to a 1.8V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. Please see the description of Standby mode later in this section.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The LH7A400-10 Card Engine was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the LH7A400 there are many different software configurations that drastically effect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes (asynchronous, synchronous, FastBus), microcontroller power management states (run, halt, standby), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the LogicLoader™ User’s Manual or appropriate BSP manual.

IMPORTANT NOTE: Most of the LH7A400-10 Card Engine hardware architecture was designed for low power battery operated applications. The Altera CPLD, on the LH7A400-10 Rev A and earlier Card Engine designs, was chosen to optimize cost over power savings. If power-optimization is the primary goal of the design, please ensure that the design is utilizing LH7A400-10 Rev B or later Card Engines which incorporate a Xilinx Coolrunner CPLD.

3.5.3 Peripherals

Most peripherals provide software programmable power states. Sometimes, however, these programmable power states may not be the best solution. The SMSC 91C111 controller, for example, has software programmable power states which may not be sufficient for some applications. In order to solve this problem, Logic has provided hardware to cut power to the 91C111 IC. Please see the appropriate data sheets and the "LH7A400-10 IO Controller Specification" for more information.

The LH7A400-10 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3V_WRLAN, 3.3VA, and VCORE for a flexible hardware design. See Figure 3.4 below.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_ SDRAM	3.3VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to refresh.
3.3V	3.3VDC	Connects to the digital peripherals on the Card Engine.
3.3VA	3.3VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
VCORE	1.8V	Connects to the processor core voltage. See information on each specific processor for the VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperatures, etc.
3.3V_WRLAN	3.3V (This Pin is an output, see section 3.5.1.4)	Provides power to the SMSC 91C111 processor from the 3.3V area. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the IO Controller Specification for controlling this signal.

IMPORTANT NOTE: Because the power management on the SMSC 91C111 is not suitable for many applications, the PMOS FET was added to control power input into the wired LAN.

Figure 3.4: Power Plane Diagram

3.5.4 Microcontroller

The LH7A400 processor power management's scheme was designed to be easy to use. There are three power management states provided in the LH7A400 microcontroller: RUN, STANDBY, and HALT. Please see below for descriptions from all three states and the LH7A400 Universal Microcontroller User's Guide for more details

3.5.4.1 Run Mode

Run is the LH7A400-10 Card Engine's normal operating stat in which both oscillator inputs and all clocks are hardware enabled. The LH7A400 can enter Run mode from either the Standby or Halt states. From the Standby state, Run can be accessed on three conditions: a rising-edge on the wakeup pin (the uP_WAKEUP signal), an exit from the Clock Set register (after a the clock divisor has been adjusted and the new clock output has stabilized), or the falling-edge of an interrupt (interrupts are active low). A Halt to Run transition occurs on the falling-edge of an interrupt (interrupts are active low), Power Fail, or on a user reset (Soft Reset).

IMPORTANT NOTE: Two seconds after a power on reset, a rising edge transition on the uP_WAKEUP signal is required to transition from Standby to Run mode. The uP_WAKEUP signal is pulled to 3.3V_uP_SDRAM on the Card Engine so a pushbutton tied to ground implementation can easily be used to provide the required low to high transition on the uP_WAKEUP signal. The SDK and IDK kits have example circuitry for the required uP_WAKEUP signal transition.

3.5.4.2 Standby Mode

Standby is the LH7A400 Card Engine's hardware power down mode, allowing for minimal power consumption. In this mode, only the 32.768 kHz clock input is enabled and the Real Time Clock and state controller are the only active functional blocks. Before all the clocks are turned off, however, the SDRAM is put into self-refresh mode, and maintains the contents of memory while in the low power state. Standby mode can only be entered after a system power-on or on a progression from the Run state. A Run to Standby transition occurs on a Power Fail, User Reset (Soft Reset), Write Clock Set (new clock divisors specified), or read of the STBY register.

IMPORTANT NOTE: Two seconds after a power on reset, a rising edge transition on the uP_WAKEUP signal is required to transition from Standby to Run mode.

3.5.4.3 Halt Mode

The Halt state is designed to reduce power consumption while the LH7A400 is waiting for an event such as a keyboard input. In this mode, although the processor clock is halted, the 14.7456 MHz oscillator input is enabled, thereby allowing software to specify the other active and inactive clocks. In this way, it is possible to maintain the LCD image yet reduce system-wide power usage at the same time. The only way to transition to the Halt state is on a read from the HALT register while in the Run state.

IMPORTANT NOTE: Although Halt consumes less power than Run mode, it consumes more power than the Standby Mode. Thus, on a power failure, the LH7A400 system will actually leave the Halt state and transition to the Standby state (the same thing occurs on a SW_nRESET.

3.5.4.4 Wakeup

A rising edge on the LH7A400 processor's wakeup signal (net uP_WAKEUP) will transition the processor from the Standby to Run state. A rising edge transition on the wakeup signal is the only way to transition the system out of the power on reset Standby state, whereas the other Standby states can be exited through the use of an interrupt (if configured correctly).

The LH7A400-10 Card Engine employs a auto-wakeup feature if the SMSC91C111 Ethernet controller is populated on the Card Engine. The SMSC91C111 has a 25MHz output clock which is passed through a divider in the on-board CPLD which then creates a standing waveform on the uP_WAKEUP net. This standing waveform will auto-wake the processor from any Standby state. This auto-wakeup feature can be disabled by software after the processor boots up via a control bit in the on-board CPLD.

Please refer to the LH7A400-10_IO_Controller_Spec document for more information on how to enable or disable the auto-wakeup feature.

3.6 ESD Considerations

The LH7A400-10 Card Engine was designed to interface to a customer's peripheral board. The Card Engine was designed to be low cost and adaptable to many different applications. The LH7A400-10 Card Engine does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SDRAM Memory Map

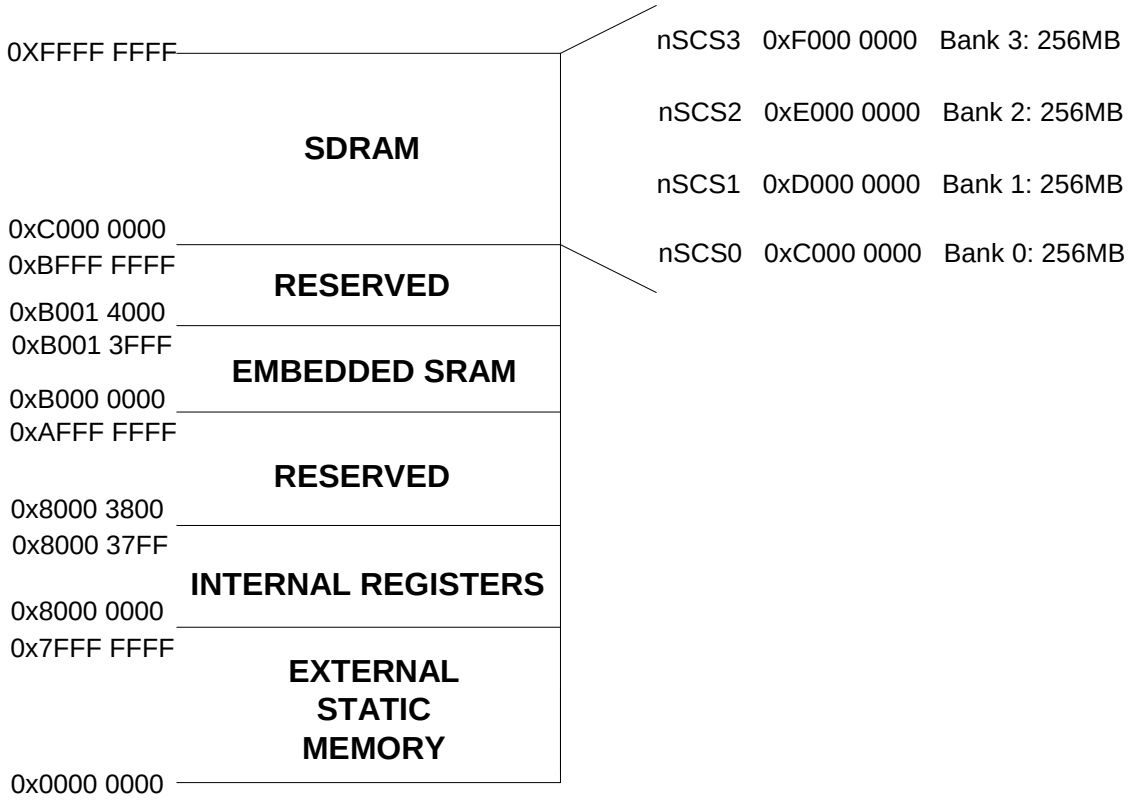

Figure 4.1: LH7A400 SDRAM Memory Map Diagram

4.2 External Static Memory Map

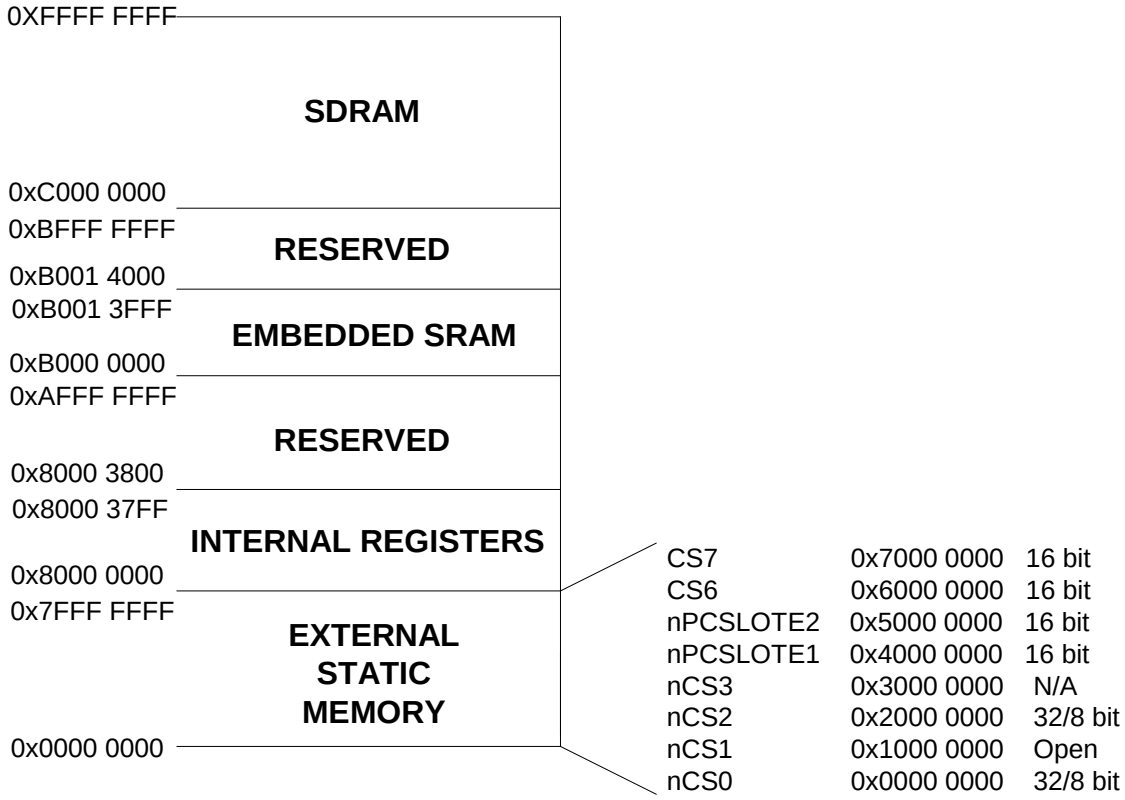

Figure 4.2: LH7A400 External Static Memory Map Diagram

NOTE: The bit numbers refer to the bank width at reset. Banks 1 and 3 (nCS0 and nCS2) are 32-bits wide if flash is used as the boot device and 8-bits wide if an EEPROM is used as the boot device.

4.2.1 Card Engine Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the Card Engine.

Chip Select	Bank	Start Address	Memory Description
CS7	7	0x7000 0000	IO Controller Peripherals (fast1)
CS6	6	0x6000 0000	IO Controller Peripherals (slow1)
nPCSLOTE2	5	0x5000 0000	Used for PC Card Interface
nPCSLOTE1	4	0x4000 0000	Used for PC Card Interface
nCS3	3	0x3000 0000	N/A2
nCS2	2	0x2000 0000	Boot Device (flash or Off-Board)
nCS1	1	0x1000 0000	Video
nCS0	0	0x0000 0000	Boot Device (flash or Off-Board)

Notes:
1. CPLD peripherals are components that get a decoded chip select from the CPLD (e.g., CPLD memory mapped registers, onboard SMSC 91C111 Ethernet controller. Please see the LH7A400-10 IO Controller Specification document for details.) These peripherals are separated into two different chip select banks, due to difference in timing: slow and fast.
2. Pin nCS3 is used for MMC select.

4.2.2 Chip Select 6 (CS6) – CPLD Peripherals (slow timing)

The table below indicates how the CPLD decodes chip select 6. For more detailed information see the LH7A400-10 IO Controller Specification.

Address Range	Memory Block Description	Size
0x6000 0000 – 0x601F FFFF	Reserved	2MB
0x6020 0000 – 0x603F FFFF	CF Chip Select	2MB
0x6040 0000 – 0x605F FFFF	ISA-like Bus Chip Select	2MB
0x6060 0000 – 0x61FF FFFF	Reserved - On-Board Expansion	2MB (X13)
0x6200 0000 – 0x62FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x6300 0000 – 0x63FF FFFF	Open – Available for User	1MB (X16)

4.2.3 Chip Select 5 (CS7) – CPLD Peripherals (fast timing)

The table below indicates how the CPLD decodes chip select 7. For more detailed information see the LH7A400-10 IO Controller Specification.

Address Range	Memory Block Description	Size
0x7000 0000 – 0x701F FFFF	Wired LAN Chip Select	2MB
0x7020 0000 – 0x703F FFFF	Card Engine Control Reg	2MB
0x7040 0000 – 0x705F FFFF	Reserved	2MB
0x7060 0000 – 0x707F FFFF	SPI Data Reg	2MB
0x7080 0000 – 0x709F FFFF	SPI Control Reg	2MB
0x70A0 0000 – 0x70BF FFFF	EEPROM SPI Reg	2MB
0x70C0 0000 – 0x70DF FFFF	Interrupt/Mask Reg	2MB
0x70E0 0000 – 0x70FF FFFF	Mode Reg	2MB
0x7100 0000 – 0x711F FFFF	Flash Reg	2MB
0x7120 0000 – 0x713F FFFF	Power Management Reg	2MB
0x7140 0000 – 0x715F FFFF	IO Controller Code Revision Reg	2MB
0x7160 0000 – 0x717F FFFF	Extended GPIO Reg	2MB
0x7180 0000 – 0x719F FFFF	GPIO Data Reg	2MB
0x71A0 0000 – 0x71BF FFFF	GPIO Direction Reg	2MB
0x71C0 0000 – 0x71FF FFFF	Reserved - On-Board Expansion	2MB (X2)
0x7200 0000 – 0x72FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x7300 0000 – 0x73FF FFFF	Open – Available for User	1MB (X16)

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs, active low or active high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the Card Engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SODIMM 144-Pin Descriptions

J1C Pin#	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I/O	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of external memory. Refer to the reset description found in section 3.2.1 for more information on how this signal is driven. Every peripheral on the Card Engine with a reset line is reset with the assertion of this signal. Refer to LH7A400 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	SW_nRESET	I	Active Low. This signal initiates a soft reset (manual reset) – external memory contents are retained during reset. This pin is connected to the CPLD; please see LH7A400-10 IO Controller Specification for detailed information on the use of the CPLD based reset. The SW_nRESET must be implemented in software in order to function properly. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nCS	O	Active Low. Chip select for area 7 of LH7A400-10 memory -- the "fast" peripheral chip select area. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts FAST_nCS.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8	SLOW_nCS	O	Active Low. Chip select for area 6 of LH7A400-10 memory -- the “slow” peripheral chip select area. See memory map for details. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts SLOW_nCS.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nMCS	O	Active Low. Buffered chip select for area 1 of LH7A400-10 memory. This is the "video" chip select area. This chip select is also capable of controlling additional external SDRAM. This is set to a 32 bit wide area and can be changed based on the user's needs. See memory map for details.
11	nACT_LED/LAN_LED1	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.

J1C Pin#	Signal Name	I/O	Description
12	BOOT_nCS	O	Active Low. This signal is the chip select for boot ROM in area 0 when uP_MODE3 is low. When uP_MODE3 is high, this signal is the chip select for a specific memory mapped address in the slow chip select area of LH7A400-10 memory (16 bit wide area 2). See memory map for details.
13	nLNK_LED/LAN_LED2	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in. See the LH7A400-10 IO Controller Specification for further details.
15	nSTANDBY	I	Active Low. CPU power mode signal. If supported by installed software, a low nSTANDBY signal is meant to cause the Card Engine to enter standby mode (hardware power down), where the contents of the SDRAM are placed in self-refresh and will be maintained. From standby, run is entered in response to a rising edge on wakeup, after an exit from CLKSET, or in response to an interrupt or fast interrupt falling edge (IRQ/FIQ – assuming interrupts are enabled). Software must be implemented in order for this signal to operate properly. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the LH7A400-10 IO Controller Specification for further details.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid or the processor data bus is in use. See the LH7A400-10 IO Controller Specification for further details.
21	uP_WAKEUP	I	Triggers on rising edge. This CPU power mode signal causes run mode to be entered from standby mode. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. **IMPORTANT NOTE:** If the auto-wakeup feature is not enabled, the user MUST provide a rising edge on this signal for the processor to transition from Standby to Run mode. The processor will not execute any instructions until this signal has had a rising edge transition at least two seconds after a power on reset.
22		NC	
23	CPLD_nIRQD	I	Active Low. Dedicated hardware interrupt on LH7A400-10. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
24	uP_TEST1	I	This is connected to Test Mode Pin 0 on the LH7A400 processor. Please see the section on Operating Modes in the LH7A400 technical datasheet for detailed operation. A high state on this signal is required for normal processor operation. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
25	uP_nIRQC	I	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
26	uP_TEST2	I	This is connected to Test Mode Pin 1 on the LH7A400 processor. For normal mode leave open, for JTAG mode tie to GND. For more information, please see the section on Operating Modes in the LH7A400 technical datasheet for detailed operation. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor to put the processor in normal operation mode.

J1C Pin#	Signal Name	I/O	Description
27	uP_nIRQB	I	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
28	MSTR_nRST	I/O	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of external memory. Refer to the reset description found in section 3.2.1 for more information on how this signal is driven. Every peripheral on the Card Engine with a reset line is reset with the assertion of this signal. Refer to LH7A400 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
29	uP_nIRQA	I	Active Low. Dedicated hardware interrupt on LH7A400-10. May also be configured as a GPIO pin. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
30	uP_TMS	I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
31		NC	No internal connection (not implemented on the LH7A400-10)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use. This signal is pulled up to 3.3V through a 10K resistor.
33		NC	No internal connection (not implemented on the LH7A400-10)
34	uP_TDI	I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
35		NC	No internal connection (not implemented on the LH7A400-10)
36	uP_TCK	I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V through a 10K resistor.
37		NC	No internal connection (not implemented on the LH7A400-10)
38	uP_MODE3	I	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished in the CPLD: if signal uP_MODE3 is high (internal boot device), then flash_nCS = uP_nCS0 and BOOT_nCS = uP_nCS2 and vice-versa if uP_MODE3 is low. This defaults to high (onboard flash) if left unconnected (pulled to 3.3V_uP_SDRAM through a 10K pull-up resistor).
39	uP_UARTA_RTS	O	The LH7A400 does not directly support UART RTS signals, but Logic BSPs create this signal using an available LH7A400 GPIO signal. If Logic software is not used, this signal can be used as a GPIO.
40	uP_MODE2	I	The LH7A400 processor only supports Little Endian memory operations. On development kits by Logic Product Development, the generic use of this pin is an Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left unconnected (pulled to 3.3V_uP_SDRAM through a 10K pull-up resistor). This pin can also be used as a General Purpose input and read from the CPLD register.
41	uP_UARTA_CTS	I	UART2 Clear to Send Signal.
42	uP_MODE1	I	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = 8 bit, 0/1 = 16 bit, 1/0 = 32 bit, 1/1 = 32 bit. This defaults to high if left unconnected (pulled to 3.3V_uP_SDRAM through a 10K pull-up resistor).
43	uP_UARTA_TX	O	UART 2 transmit output signal. Internally pulled up on the LH7A400 processor.
44	uP_MODE0	I	Bus width setting. uP_MODE1/uP_MODE0 - 0/0 = 8 bit, 0/1 = 16 bit, 1/0 = 32 bit, 1/1 = 32 bit. This defaults to low if left unconnected (pulled to DGND through a 10K pull-down resistor).
45	uP_UARTA_RX	I	Serial Communication Interface (UARTA) data input.
46		NC	No internal connection (not implemented on the LH7A400-10)
47		NC	No internal connection (not implemented on the LH7A400-10)
48		NC	No internal connection (not implemented on the LH7A400-10)
49	uP_UARTA_DSR	O	UARTA data set ready signal.
50		NC	No internal connection (not implemented on the LH7A400-10)

J1C Pin#	Signal Name	I/O	Description
51	nSUSPEND	I	Active low. This signal is one of the CPLD interrupts and is meant to activate software that will suspend LH7A400 operations. This pin is connected directly to the CPLD and it is pulled up to 3.3V_uP_SDRAM by a 10k resistor. Software is required for proper suspend operation.
52		NC	No internal connection (not implemented on the LH7A400-10)
53	uP_AUX_CLK	O	This signal is a programmable auxiliary clock that is set to 14.7496 (max value) by default.
54		NC	No internal connection (not implemented on the LH7A400-10)
55	DGND	I	Digital Ground (0V)
56		NC	No internal connection (not implemented on the LH7A400-10)
57	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
58	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
59	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
60	VCORE	I	CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
65	uP_SPI_FRM	O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI data transmission or reception.
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 100MHz and is connected to the SDRAM as well as the CPLD. This signal is, by default, unavailable in an effort to reduce on board EMI noise. It can be made available upon request, please contact Logic for more information.
67	uP_SPI_TX	O	This output transmits synchronous SPI data.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_RX	I	This input receives synchronous SPI data.
70	uP_nRAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into row addressing mode.
71	uP_SPI_SCK	O	SPI clock signal. SPI transmit/receive data is valid on the rising edge of this clock (data is output from one falling edge to the next and clocked in on the rising edge). This signal is pulled-down internally on the LH7A400 processor
72	uP_nCAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into column addressing mode.
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74	uP_nMWE3	O	Active low. Buffered write enable for buffered data bus bits 24->31.
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	nWE2	O	Active Low. This is the LH7A400 Address bit 0 that can be used as a buffered Write Enable 2 signal.
77	uP_MD2	I/O	Buffered Data Bus bit 2.

J1C Pin#	Signal Name	I/O	Description
78	nWE1	O	Active Low. This is the LH7A400 Address bit 0 that can be used as a buffered Write Enable 1 signal.
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0	O	Active low. Buffered write enable for buffered data bus bits [7:0].
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active Low. When low, this buffered signal signifies a write cycle on the bus. When high, this signal signifies that the current bus cycle is a read cycle or that the bus is inactive. This signal is asserted whenever processor WE0 or SDWE signals are asserted so it can be used in both synchronous and asynchronous memory areas. Since this signal is based on WE0 for the asynchronous memory areas, it will only be asserted low on long word aligned writes to those areas. Non long word aligned writes to the asynchronous memory areas will not be indicated with this signal
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	Active low. This buffered signal is the read strobe that latches data output from external peripherals.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86		NC	No internal connection (not implemented on the LH7A400-10)
87	uP_MD7	I/O	Buffered Data Bus bit 7.
88		NC	No internal connection (not implemented on the LH7A400-10)
89	DGND	I	Digital Ground (0V)
90	uP_MA0	O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	O	Buffered Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)
108	uP_MA9	O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.
116	uP_MA13	O	Buffered Address Bus bit 13.

J1C Pin#	Signal Name	I/O	Description
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	O	Buffered Address Bus bit 16.
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.
136	uP_MA23	O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	O	Buffered Address Bus bit 24.
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

J1A Pin#	Signal Name	I/O	Description
1	LCD_VSYNC	O	LCD VSYNC (TFT Signal).
2	LCD_HSYNC	O	LCD HSYNC (TFT Signal).
3	LCD_DCLK	O	LCD Panel Data Clock
4		NC	No internal connection (not implemented on the LH7A400-10)
5	LCD_MDISP	O	LCD enable signal (TFT signal).
6	LCD_VEEEN	O	Active high. This signal is the enable for the LCD panel Vee. It is controlled in the CPLD; see the LH7A400-10 IO Controller Specification for further details.
7	LCD_VDDEN	O	Active high. This signal is the LCD panel Vcc enable. May also be configured as a LH7A400 GPIO pin.
8		NC	No internal connection (not implemented on the LH7A400-10)
9	DGND	I	Digital Ground (0V)
10	LCD_CLS	O	LCDCLS Signal Output (Row Driver Clock) – This signal is only used with a HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
11	LCD_SPS	O	LCDSPS Signal Output (Row Reset) – This signal is only used with a HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
12	LCD_PSAVE	O	LCDPS Signal Output (Power Save)–This signal is only used with a HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
13	LCD_SPL	O	LCDSPL Signal Output (Start Pulse Left) – This signal is only used with the HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
14	LCD_HRLP	O	LCD Horizontal Sync Pulse/ Line clock (Latch Pulse) – This signal is only used with the HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
15		NC	No internal connection (not implemented on the LH7A400-10)
16	LCD_REV	O	LCDREV Signal Output (Grey Scale Voltage Reverse) – This signal is only used with the HR-TFT interface. May also be configured as a LH7A400 GPIO pin.
17	uP_STATUS_1	O	This signal is a general purpose output (GPO). It is controlled by a memory-mapped address in the CPLD. This signal is an open drain signal; baseboard designs may need to pull this signal high depending on signaling needs. For more information on how this signal is driven, see the LH7A400-10 IO Controller Specification. This signal is typically used by Logic's software solutions as a system status indication.
18	uP_STATUS_2	O	This signal is a general purpose output (GPO). It is controlled by a memory-mapped address in the CPLD. This signal is an open drain signal; baseboard designs may need to pull this signal high depending on signaling needs. For more information on how this signal is driven, see the LH7A400-10 IO Controller Specification. This signal is typically used by Logic's software solutions as a system status indication.
19	uP_AC97_BITCLK	I/O	Clock output from the onboard AC97 CODEC. If no CODEC is populated, the LH7A400 can accept an external AC97 bit clock on this signal.
20	uP_AC97_RESET	O	AC97 reset line to an AC97 compliant audio CODEC. May also be configured as a LH7A400 GPIO pin.
21	uP_AC97_SYNC	O	This signal is the AC97 sync output to an AC97 compliant audio CODEC. The CODEC Frequency is set on CODEC to be 48Khz, while the default frequency for the sync is set up to be 2.9491Mhz (14.7456MHz / 5) on the processor.
22	uP_AC97_SD_IN	I	This signal is the AC97 output from the processor to the AC97 compliant audio CODEC.

J1A Pin#	Signal Name	I/O	Description
23	uP_AC97_SD_OUT	O	This signal is the AC97 input from the processor to the AC97 compliant audio CODEC.
24	DGND	I	Digital Ground (0V)
25	A/D1	I	Analog input into the touch screen controller: 0 to 3.3V swing possible.
26	A/D2	I	Analog input into the touch screen controller: 0 to 3.3V swing possible
27	AGND	I	Analog Ground (0V)
28		NC	No internal connection (not implemented on the LH7A400-10)
29		NC	T No internal connection (not implemented on the LH7A400-10)
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio CODEC.
32	CODEC_INR	I	Right channel stereo line input of the audio CODEC.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch panel controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch panel controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch panel controller.
39	TOUCH_TOP	I	This is the X- position input to the four-wire resistive touch panel controller.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. Note that R0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and G0, which are connected to LCD_D15 on the processor
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1 is connected to LCD_D0.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2 is connected to LCD_D1.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3 is connected to LCD_D2.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4 is connected to LCD_D3.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5 is connected to LCD_D4. May also be configured as a LH7A400 GPIO pin.
48	G0	O	The LCD data bus used to transmit data to the LCD module. Note that G0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and R0, which are connected to LCD_D15 on the processor
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1 is connected to LCD_D5. May also be configured as a LH7A400 GPIO pin.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2 is connected to LCD_D6. May also be configured as a LH7A400 GPIO pin.

J1A Pin#	Signal Name	I/O	Description
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3 is connected to LCD_D7. May also be configured as a LH7A400 GPIO pin.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4 is connected to LCD_D8. May also be configured as a LH7A400 GPIO pin.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5 is connected to LCD_D9. May also be configured as a LH7A400 GPIO pin.
54	B0	O	The LCD data bus used to transmit data to the LCD module. Note that B0 is an intensity bit for the LCD display and therefore is tied to the other intensity bits, G0 and R0, which are connected to LCD_D15 on the processor. May also be configured as a LH7A400 GPIO pin.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1 is connected to LCD_D10. May also be configured as a LH7A400 GPIO pin.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2 is connected to LCD_D11. May also be configured as a LH7A400 GPIO pin.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3 is connected to LCD_D12. May also be configured as a LH7A400 GPIO pin.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4 is connected to LCD_D13. May also be configured as a LH7A400 GPIO pin.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5 is connected to LCD_D14. May also be configured as a LH7A400 GPIO pin.
61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. LH7A400-10 IO Controller Specification for further details. This signal is pulled up to 3.3V through a 10K resistor.
62	uP_PCC_RDYA	I	This signal is the RDY signal for slot A on the LH7A400-10 Card Engine. This signal is pulled up to 3.3V through a 10K resistor. Please refer to the PCMCIA reference or IDK design for proper Dual slot PCMCIA support. May also be configured as a LH7A400 GPIO pin.
63	CPLD_GPIO_1	O	This signal is a general purpose output (GPO). It is controlled by a memory-mapped address in the CPLD. This signal is an open drain signal; baseboard designs may need to pull this signal high depending on signaling needs. For more information on how this signal is driven, see the LH7A400-10 IO Controller Specification.
64	CPLD_GPIO_2	O	This signal is a general purpose I/O (GPIO). It is controlled by a memory-mapped address in the CPLD. When configured as an output, this signal is an open drain signal; baseboard designs may need to pull this signal high depending on signaling needs See the LH7A400-10 IO Controller Specification for further details.
65		NC	No internal connection (not implemented on the LH7A400-10)
66	DGND	I	Digital Ground (0V)
67	uP_USB1_nOVR_CRNT - VBUS	I	Active high. This is a data carrier detect signal used to determine whether or not the USB interface is currently in use.
68		NC	No internal connection (not implemented on the LH7A400-10)
69	uP_USB1_PWR_EN	O	Active high. Enables power supply for USB.
70		NC	No internal connection (not implemented on the LH7A400-10)
71		NC	No internal connection (not implemented on the LH7A400-10).

J1A Pin#	Signal Name	I/O	Description
72	uP_USB1_M	I	USB data I/O minus. Route as a differential pair with uP_USB1_P.
73	uP_USB1_P	I	USB data I/O plus. Route as a differential pair with uP_USB1_M.
74	BUFF_nOE	O	Active low. This signal is the output enable for all five buffers on the Card Engine. This signal is pulled up to 3.3V through a 10K resistor in order to ensure the buffers are tri-stated upon powering up the Card Engine. When low, the buffers are active. See the LH7A400-10 IO Controller Specification for further details on how this signal is driven.
75		NC	No internal connection (not implemented on the LH7A400-10)
76	BUFF_DIR_DATA	O	Active high. Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). See the LH7A400-10 IO Controller Specification for further details.
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the AC97 compliant audio CODEC. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio CODEC Technical Datasheet for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different Card Engines.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the Card Engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different Card Engines.

5.3 J1B Expansion Connector Pin Description

J1B Pin#	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled down through a 10K resistor to digital GND.
2	CPLD_TDO	O	This input transmits data out of the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
3	CPLD_TMS	I	This input indicates the mode of CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
4	CPLD_TDI	I	This input receives data on the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible. This signal is pulled up to 3.3V through a 10K resistor.
5	uP_PCC_nOE	O	This signal is PC Card Output Enable, Attribute and Common Memory space read control. May also be configured as a LH7A400 GPIO pin.
6	uP_PCC_nWE	O	This signal is for PC Card Enable, Attribute and Common Memory space write control. May also be configured as a LH7A400 GPIO pin.
7	uP_PCC_nIORD	O	This signal is for PC Card IO Read Output. May also be configured as a LH7A400 GPIO pin.
8	uP_PCC_nIOWR	O	This signal is for PC Card IO Write Output. May also be configured as a LH7A400 GPIO pin.
9	DGND	I	Digital Ground (0V)
10	uP_PCC_RESET	O	This signal is PC Card Reset Card 1. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
11	PCC_nCE1B	O	Active low. This signal is PC Card Enable 1 and is used with PCC_nCE2B to decode low and high byte accesses for slot B.
12	PCC_nCE2B	O	Active low. This signal is PC Card Enable 2 and is used with PCC_nCE1B to decode low and high byte accesses for slot B.
13	PCC_nIOIS16	I	This signal is an input to the onboard CPLD. The state of this pin can be read from the MODE register. See the LH7A400-10 IO Controller Specification for further details.
14	uP_PCC_RDYB	I	This is the PC Card ready signal input in dual card mode. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
15	uP_PCC_nWAIT	I	This is the PC Card wait signal input in dual card mode. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
16	uP_PCC_BVD2	I	This signal is the Battery Sense 2 signal and is connected to GPIO Port A bit 5. This signal is pulled up to 3.3V through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
17	uP_PCC_BVD1	I	This signal is the Battery Sense 1 signal and is connected to GPIO Port A bit 4. This signal is pulled up to 3.3V through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
18	PCC_nCD2	I	This signal is connected to the onboard CPLD. The state of this pin can be read from a register in the CPLD. This signal is pulled up to 3.3V through a 10K resistor. See the LH7A400-10 IO Controller Specification for further details.

J1B Pin#	Signal Name	I/O	Description
19	PCC_nCD1	I	This signal is connected to the onboard CPLD. The state of this pin can be read from a register in the CPLD. This signal is pulled up to 3.3V through a 10K resistor. See the LH7A400-10 IO Controller Specification for further details.
20	uP_PCC_REG	O	This signal is for PC Card Register Memory Accesses. May also be configured as a LH7A400 GPIO pin.
21	DGND	I	Digital Ground (0V)
22	PCC_VS1	I	This is the PC Card Voltage Sense 1 signal. This signal is pulled up to 3.3V through a 10K resistor. This signal is connected to the onboard CPLD. The state of this pin can be read from a register in the CPLD. See the LH7A400-10 IO Controller Specification for further details.
23	uP_PCC_VS2	I	This is the PC Card Voltage Sense 2 signal. This signal is pulled up to 3.3V through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
24	PCC_nDRV	O	This is the PC Card drive output signal. The signal can driven from the onboard CPLD. See the LH7A400-10 IO Controller Specification for further details.
25	uP_PCC_PCDIR	O	This signal is used for PC Card data direction. May also be configured as a LH7A400 GPIO pin.
26	uP_DQM3	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[24:32].
27	uP_DQM2	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[16:23].
28	uP_DQM1	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[8:15].
29	uP_DQM0	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[0:7].
30	uP_IRTX	O	This is the IrDA Transmit signal, which is used for the Infrared Mode on UARTC.
31	uP_IRRX	I	This is the IrDA Receive signal, which is used for the Infrared Mode on UARTC.
32	DGND	I	Digital Ground (0V)
33	MFP1 - uP_KEY_COL0	I/O	This signal is Column 0 of the keyboard column drivers.
34	MFP2 - uP_KEY_COL1	I/O	This signal is Column 1 of the keyboard column drivers.
35	MFP3 - uP_KEY_COL2	I/O	This signal is Column 2 of the keyboard column drivers.
36	MFP4 - uP_KEY_COL3	I/O	This signal is Column 3 of the keyboard column drivers.
37	MFP5 - uP_KEY_COL4	I/O	This signal is Column 4 of the keyboard column drivers.
38	MFP6 - uP_KEY_COL5	I/O	This signal is Column 5 of the keyboard column drivers.
39	MFP7 - uP_KEY_COL6	I/O	This signal is Column 6 of the keyboard column drivers.
40	MFP8 - uP_KEY_COL7	I/O	This signal is Column 7 of the keyboard column drivers.
41	uP_UARTB_TX	O	UART 3 transmit output signal on the LH7A400. This signal is internally pulled-down on the LH7A400 if UART 3 is enabled. May also be configured as a LH7A400 GPIO pin.
42	uP_UARTB_RX	I	UART 3 receive input signal on the LH7A400. May also be configured as a LH7A400 GPIO pin.
43	uP_UARTB_CTS	O	UART 3 clear to send on the LH7A400-10. May also be configured as a LH7A400 GPIO pin.
44	DGND	I	Digital Ground (0V)
45	uP_UARTB_RTS	O	GPIO on LH7A400 used by Logic BSPs to create UARTB RTS signal. May also be configured as a LH7A400 GPIO pin.

J1B Pin#	Signal Name	I/O	Description
46	uP_UARTC_TX	O	UART 1 transmit output signal on the LH7A400. May also be configured as a LH7A400 GPIO pin.
47	uP_UARTC_RX	I	UART 1 receive input signal on the LH7A400. May also be configured as a LH7A400 GPIO pin.
48	MFP9 - uP_MMC_CMD	I/O	This bi-directional signal is used for MMC card initialization and data transfer commands.
49	MFP10 - uP_MMC_nSELECT	I/O	This signal is used as the MMC chip select.
50	MFP11 - uP_MMC_DATA	I/O	This signal is the MMC bi-directional data channel with width of one line, operating in a push-pull mode with only one card or the MMC Controller driving this line at a time.
51	MFP12 - uP_MMC_CLK	I/O	This is the MMC CLOCK, which can vary from 0 – 20 MHz. During each cycle of this signal, a one-bit transfer occurs on the command and data lines.
52	MFP13 - uP_SCI_CLK	I/O	This signal is the Smart Card Interface Clock
53	MFP14 - uP_A25 - SCI_IO	I/O	This signal is the Smart Card Interface data I/O. This signal is pulled down to digital ground through a 10K resistor.
54	MFP15 - uP_SCI_MEDCHG	I/O	Boot Media Device Change Used with the uP_MODE0 and uP_MODE1 signals to specify boot memory device. In this case, both MODE0 and MODE1 are pulled up and therefore the processor is prepared to boot up from a 32Kbit source on reset.
55	DGND	I	Digital Ground (0V)
56	MFP16 - uP_SCI_DETECT	I/O	This signal is the Smart Card Detection signal. Upon smart card insertion, this signal is asserted to notify the LH7A400 that a new card is present. This signal is pulled down to digital ground through a 10K resistor. May also be configured as a LH7A400 GPIO pin.
57	MFP17 - uP_SCI_VCCEN	I/O	This signal is the Smart Card Supply Voltage Enable. May also be configured as a LH7A400 GPIO pin.
58	MFP18 - uP_SCI_RESET	I/O	This signal is the Smart Card Interface Reset.
59	MFP19 - PWMEN0	I/O	Active low. This signal is the DC-DC converter pulse width modulator 0 enable.
60	MFP20 – PCC_nCE1A	O	Active low. This signal is PC Card Enable 1 and is used with PCC_nCE2A to decode low and high byte accesses for slot A.
61	MFP21 - PWM0	I/O	This signal is the DC-DC converter pulse width modulator 0 Output.
62	MFP22 – PCC_nCE2A	O	Active low. This signal is PC Card Enable 2 and is used with PCC_nCE1A to decode low and high byte accesses for slot A.
63	MFP23 - uP_BMI_CLK	I/O	This signal is the Smart Battery Clock. May also be configured as a LH7A400 GPIO pin.
64	MFP24 - uP_BMI_IO_SWI	I/O	This signal is the Smart Battery Data line. May also be configured as a LH7A400 GPIO pin.
65	MFP25 - uP_nBATCHG	I/O	This is the Battery Charge signal. This signal is pulled up to 3.3V through a 10K resistor.
66	DGND	I	Digital Ground (0V)
67	MFP26 - uP_BATOK	I/O	This is the Battery OK signal. When the board is not plugged into external power, a transition to the run state may not occur unless a valid battery is present and the BATOK signal is high. This signal is pulled up to 3.3V through a 10K resistor.
68	MFP27 – PWM1	I/O	PWM output from LH7A400 processor. This can be enabled and disabled in software.
69	MFP28 - uP_nMCS2	I/O	Active low. This signal is the buffered output of the processor's Memory Chip Select 2.
70	MFP29 - uP_SDCKE	I/O	LH7A400 SDRAM controllers SDCKE signal. This signal is used to interface with external SDRAM ICs.

J1B Pin#	Signal Name	I/O	Description
71	MFP30 - uP_nSDCS2	I/O	Active low. This signal is the processor's Synchronous Memory Chip Select 2.
72	MFP31 - uP_nSDCS1	I/O	Active low. This signal is the processor's Synchronous Memory Chip Select 1.
73	MFP32 - uP_nEXTPWR	I/O	Active low. This is the Power Supply signal. When the board is plugged into external power, this signal is asserted and the Card Engine is allow to transition to the run state (which also may occur if the battery is in use). This signal is pulled down to digital ground through a 10K resistor.
74	MFP33 - uP_BUZZER	I/O	This signal is the timer buzzer (254kHz Max) output signal that is controlled by internal registers. This signal is pulled down internally on the LH7A400.
75	MFP34 - MONO_OUT	I/O	The signal is the main mono output from the AC97 CODEC.
76	MFP35 - PC_BEEP	I/O	This is an analog input to the AC97 CODEC, typically used for PCBEEP signal.
77	DGND	I	Digital Ground (0V)
78	MFP36 - CD_IN_L	I/O	This is an analog input to the AC97 CODEC, typically used for CD line-in left signal.
79	MFP37 - CD_IN_R	I/O	This is an analog input to the AC97 CODEC, typically used for CD line-in right signal.
80	MFP38 - CD_GND	I/O	This signal is the CD input common mode reference (ground) to the AC97 CODEC.

5.4 Multiplexed Signal Trade-Offs

5.4.1 GPIO vs. Functionality Trade Offs

If a function, such as LCD, is being used, the LH7A400 processor does not allow unused pins to be used as GPIO. For example, if the LCD controller is being used, the LCD_CLS pin could not be used as a GPIO, even if it is not needed in the design. Below, you will find a table of these functions that contain GPIO, and a GPIO group number. If a pin is a member of a group, you will find the GPIO group number next to it in the Multiplexing Tables below.

Group #	Group / Function	Description
1	General GPIO	These pins can be used as GPIO with no group restrictions
2	LCD	LCD controller signals.
3	AC97 / Audio	AC97 controller signals.
4	PCMCIA / CF	PCMCIA and CF Signals.
5	UARTB	A400 UART3 Signals
6	UARTC	A400 UART1 Signals
7	Smart Card Interface	Smart Card Interface
8	BMI	Battery Monitor Interface

5.4.2 J1C Connector SODIMM 144-Pin Multiplexing

J1C Pin#	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description	GPIO Group
25	uP_nIRQC	INT2	Interrupt 2 Input	PF2	Port F bit 2 I/O	1
27	uP_nIRQB	INT1	Interrupt 1 Input	PF1	Port F bit 1 I/O	1
29	uP_nIRQA	INT0	Interrupt 0 Input	PF0	Port F bit 0 I/O	1
39	uP_UARTA_RTS	UARTA RTS	UARTA RTS	PA6	Port A bit 6 I/O	1

5.4.3 J1A Expansion Connector Pin Multiplexing

J1A Pin#	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description	GPIO Group
1	LCD_VSYNC	LCDFP	TFT LCD Vertical Sync Pulse Output	LCDFP	STN LCD Frame Pulse Output	2
2	LCD_HSYNC	LCDLP	TFT LCD Horizontal Sync Pulse Output	LCDLP	STN LCD Line Sync Pulse Output	2
5	LCD_MDISP	LCDENAB	TFT LCD Data Enable	LCDM	STN LCD AC bias signal	2
7	LCD_ VDDEN	LCDVDDEN	LCDVDDEN (Digital supply enable)	PC2	Port C bit 2 I/O	2
10	LCD_CLS	LCDCLS	ADTFT/HRTFT LCD CLS Signal Output (Gate Driver Clock)	PC5	Port C bit 5 I/O	2
11	LCD_SPS	LCDFP	ADTFT/HRTFT LCD SPS (row reset)	PC4	Port C bit 4 I/O	2
12	LCD_PSAVE	LCDPS	ADTFT/HRTFT LCD PS (power save)	PC1	Port C bit 1 I/O	2
13	LCD_SPL	LCDSPL	ADTFT/HRTFT LCD SPL Signal Output (line start pulse left)	PC7	Port C bit 7 I/O	2

J1A Pin#	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description	GPIO Group
14	LCD_HRLP	LCDHRLP	ADTFT/HRTFT LCD HRLP Signal Output (horizontal sync pulse)	PC6	Port C bit 6 I/O	2
16	LCD_REV	LCDREV	ADTFT/HRTFT LCD REV Signal Output (AC bias)	PC3	Port C bit 3 I/O	2
20	uP_AC97_RESET	AC97RESET	AC97 reset signal	PH6	Port H bit 6 I/O	3
47	R5	LCDVD4	LCD Data 4 I/O	PE0	Port E bit 0 I/O	2
49	G1	LCDVD5	LCD Data 5 I/O	PE1	Port E bit 1 I/O	2
50	G2	LCDVD6	LCD Data 6 I/O	PE2	Port E bit 2 I/O	2
51	G3	LCDVD7	LCD Data 7 I/O	PE3	Port E bit 3 I/O	2
52	G4	LCDVD8	LCD Data 8 I/O	PD0	Port D bit 0 I/O	2
53	G5	LCDVD9	LCD Data 9 I/O	PD1	Port D bit 1 I/O	2
54, 48, 41	B0,R0,G0	LCDVD15	LCD Intensity (same signal on these pins)	PD7	Port D bit 7 I/O	2
56	B1	LCDVD10	LCD Data 10 I/O	PD2	Port D bit 2 I/O	2
57	B2	LCDVD11	LCD Data 11 I/O	PD3	Port D bit 3 I/O	2
58	B3	LCDVD12	LCD Data 12 I/O	PD4	Port D bit 4 I/O	2
59	B4	LCDVD13	LCD Data 13 I/O	PD5	Port D bit 5 I/O	2
60	B5	LCDVD14	LCD Data 14 I/O	PD6	Port D bit 6 I/O	2
62	uP_PCC_RDYA	PCRDYA	PC Card Ready Signal A	PF7	Port F bit 7 I/O	4

5.4.4 J1B Expansion Connector Pin Multiplexing

J1B Pin#	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description	GPIO Group
5	uP_PCC_nOE	nPCOE	PC Card Output Enable	PG0	Port G bit 0 I/O	4
6	uP_PCC_nWE	nPCWE	PC Card Write Enable	PG1	Port G bit 1 I/O	4
7	uP_PCC_nIORD	nPCIOR	PC Card IO Write Output	PG2	Port G bit 2 I/O	4
8	uP_PCC_nIOWR	nPCIOW	PC Card IO READ Output	PG3	Port G bit 3 I/O	4
10	uP_PCC_RESET	PCRESET1	PC Card Reset 1 Output	PH0	Port H bit 0 I/O	4
14	uP_PCC_RDYB	PCRDYB	PC Card Ready Signal B	PF6	Port F bit 6 I/O	4
15	uP_PCC_nWAIT	nPCWAIT1	PC Card wait signal	PH4 / PH5	Port H bit 4 I/O Port H bit 5 I/O (Tied to both pins for use as dual PCMCIA/CF WAIT signals. If using as GPIO, use only Port H bit 4)	4
16	uP_PCC_BVD2	PCBVD2	PC Card Battery Voltage Detect 2	PA5	Port A bit 5 I/O	4
17	uP_PCC_BVD1	PCBVD1	PC Card Battery Voltage Detect 1	PA4	Port A bit 4 I/O	4
20	uP_PCC_REG	PCREG	PC Card Reg	PG4	Port G bit 4 I/O	4
23	uP_PCC_VS2	nPCSLOTE2	PC Card Voltage Sense 2 Input	PA3	Port A bit 3 I/O	4
25	uP_PCC_PCDIR	PCDIR	CF and PCMCIA Direction	PG7	Port G bit 7 I/O	4
41	uP_UARTB_TX	UARTTX3	UART B TX Output Only	PB1	Port B bit 1 I/O	5
42	uP_UARTB_RX	UARTRX3	UART B RX Input Only	PB2	Port B bit 2 I/O	5

J1B Pin#	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description	GPIO Group
43	uP_UARTB_CTS	UARTCTS3	UART B RX Clear To Send	PB3	Port B bit 3 I/O	5
45	uP_UARTB_RTS	UARTRTS3	UART B Request To Send	PA7	Port A bit 7 I/O	1**
46	UP_UARTC_TX	UARTTX1	UART C TX Output Only	PC0	Port C bit 0 I/O	6
47	UP_UARTC_RX	UARTRX1	UART C RX Input Only	PB0	Port B bit 0 I/O	6
48	MFP9 – uP_MMC_CMD	MMCCMD	MMC Command	MMSPIDIN	MMC SPI Mode Data Input	
49	MFP10 – uP_MMC_nSELECT	nMMSPICS	MMC SPI Mode Chip Select	nCS3	Asynchronous memory Chip Select 3	
50	MFP11 – uP_MMC_DATA	MMCDATA	MMC bi-directional data channel	MMSPIDOUT	MMC SPI Mode Data Output	
51	MFP12 – uP_MMC_CLK	MMCCLK	MMC Clock	MMSPICLK	MMC SPI Mode Clock	
52	MFP13 – uP_SCI_CLK	SCCLK	Smart Card interface clock	A26	Address bit 26 output	
53	MFP14 – uP_A25 - SCI_IO	SCIO	Smart Card I/O	A25	Address bit 25 output	
56	MFP16 – uP_SCI_DETECT	SCDETECT	Smart Card detection	PF5 or INT5	Port F bit 5 I/O or Interrupt 5 Input	7
57	MFP17 – uP_SCI_VCCEN	SCVCCEN	Smart Card Supply Voltage Enable	PF4 or INT4	Port F bit 4 I/O or Interrupt 4 Input	7
58	MFP18 – uP_SCI_RESET	SCRST	Smart Card Interface Reset	A27	Address bit 27 output	
63	MFP23 – uP_BMI_CLK	SMBCLK	Smart Battery Clock	PB7	Port B bit 7 I/O	8
64	MFP24 – uP_BMI_IO_SWI	SMBD	Smart Battery Data	PB6 or SWID	Port B bit 6 I/O or Single Wire Data	8

****IMPORTANT NOTE:** The uP_UARTB_RTS signal is a GPIO pin, although Logic's software uses it as a UARTB signal. If Logic's software is not used, this pin may be configured as a GPIO pin (rather than a UARTB signal).

6 Unused Pin Treatments

6.1 J1C Connector SODIMM 144-Pin Unused Pin Treatments

J1C Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	Leave floating.
2	MSTR_nRST	I/O	Leave floating. Internal pull up.
3	ETHER_RX(+)	I	Leave floating.
4	SW_nRESET	I	Leave floating. Internal pull up.
5	ETHER_TX(-)	O	Leave floating.
6	FAST_nCS	O	Leave floating.
7	ETHER_TX(+)	O	Leave floating.
8	SLOW_nCS	O	Leave floating.
9	DGND	I	Required. Digital Ground (0V)
10	VIDEO_nMCS	O	Leave floating.
11	ACT_LED/LAN_LED1	O	Leave floating.
12	BOOT_nCS	O	Leave floating.
13	LNK_LED/LAN_LED2	O	Leave floating.
14	nIOWR	O	Leave floating.
15	nSTANDBY	I	Leave floating. Internal pull up.
16	nIORD	O	Leave floating.
17	DGND	I	Required. Digital Ground (0V)
18	3.3V_WRLAN	O	Leave floating.
19	3.3V	I	Required. Power Supply (3.3V)
20	BALE	O	Leave floating.
21	uP_WAKEUP	I	Leave floating. This signal is
22		NC	Leave floating. No internal connection
23	CPLD_nIRQD	I	Leave floating. Internal pull up.
24	uP_TEST1	I	Leave floating. Internal pull up.
25	uP_nIRQC	I	Leave floating. Internal pull up.
26	uP_TEST2	I	Leave floating. Internal pull up.
27	uP_nIRQB	I	Leave floating. Internal pull up.
28	MSTR_nRST	I/O	Leave floating. Internal pull up.
29	uP_nIRQA	I	Leave floating. Internal pull up.
30	uP_TMS	I	Leave floating. Internal pull up.
31		NC	Leave floating. No internal connection
32	uP_TDO	O	Leave floating. Internal pull up.
33		NC	Leave floating. No internal connection
34	uP_TDI	I	Leave floating. Internal pull up.
35		NC	Leave floating. No internal connection
36	uP_TCK	I	Leave floating. Internal pull up.
37		NC	Leave floating. No internal connection
38	uP_MODE3	I	Leave floating. Internal pull up.
39	uP_UARTA_RTS	O	Leave floating.
40	uP_MODE2	I	Leave floating. Internal pull up.
41	uP_UARTA_CTS	I	Leave floating. Internal pull down.
42	uP_MODE1	I	Leave floating. Internal pull up.

J1C Pin #	Signal Name	I/O	Description
43	uP_UARTA_TX	O	Leave floating.
44	uP_MODE0	I	Leave floating. Internal pull down.
45	uP_UARTA_RX	I	Leave floating. Internal pull up.
46		NC	Leave floating. No internal connection
47		NC	Leave floating. No internal connection
48		NC	Leave floating. No internal connection
49	uP_UARTA_DSR	O	Leave floating.
50		NC	Leave floating. No internal connection
51	nSUSPEND	I	Leave floating. Internal pull up.
52		NC	Leave floating. No internal connection
53	uP_AUX_CLK	O	Recommend termination load near connector. 75ohm resistor in series with 10pF capacitor to DGND.
54		NC	Leave floating. No internal connection
55	DGND	I	Required. Digital Ground (0V)
56		NC	Leave floating. No internal connection
57	VCORE	I	Required. VCORE is fixed at 1.8V.
58	VCORE	I	Required. VCORE is fixed at 1.8V.
59	VCORE	I	Required. VCORE is fixed at 1.8V.
60	VCORE	I	Required. VCORE is fixed at 1.8V.
61	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
62	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
63	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
64	3.3V_uP_SDRAM	I	Required. uP and SDRAM Power Supply 3.3 V
65	uP_SPI_FRM	O	Leave floating.
66	uP_BUS_CLK	O	Recommend termination load near connector. 75ohm resistor in series with 10pF capacitor to DGND.
67	uP_SPI_TX	O	Leave floating.
68	DGND	I	Required. Digital Ground (0V)
69	uP_SPI_RX	I	Leave floating. Internal pull up.
70	uP_nRAS	O	Leave floating.
71	uP_SPI_SCK	O	Leave floating.
72	uP_nCAS	O	Leave floating.
73	uP_MD0	I/O	Leave floating.
74	uP_nMWE3	O	Leave floating.
75	uP_MD1	I/O	Leave floating.
76	nWE2	O	Leave floating.
77	uP_MD2	I/O	Leave floating.
78	nWE1	O	Leave floating.
79	uP_MD3	I/O	Leave floating.
80	uP_nMWE0	O	Leave floating.
81	uP_MD4	I/O	Leave floating.
82	uP_nMWR	O	Leave floating.
83	uP_MD5	I/O	Leave floating.
84	uP_nMRD	O	Leave floating.
85	uP_MD6	I/O	Leave floating.
86		NC	Leave floating. No internal connection
87	uP_MD7	I/O	Leave floating.

J1C Pin #	Signal Name	I/O	Description
88		NC	Leave floating. No internal connection
89	DGND	I	Required. Digital Ground (0V)
90	uP_MA0	O	Leave floating.
91	uP_MD8	I/O	Leave floating.
92	uP_MA1	O	Leave floating.
93	uP_MD9	I/O	Leave floating.
94	uP_MA2	O	Leave floating.
95	uP_MD10	I/O	Leave floating.
96	uP_MA3	O	Leave floating.
97	uP_MD11	I/O	Leave floating.
98	uP_MA4	O	Leave floating.
99	uP_MD12	I/O	Leave floating.
100	uP_MA5	O	Leave floating.
101	uP_MD13	I/O	Leave floating.
102	uP_MA6	O	Leave floating.
103	uP_MD14	I/O	Leave floating.
104	uP_MA7	O	Leave floating.
105	uP_MD15	I/O	Leave floating.
106	uP_MA8	O	Leave floating.
107	3.3V	I	Leave floating.
108	uP_MA9	O	Leave floating.
109	DGND	I	Required. Digital Ground (0V)
110	uP_MA10	O	Leave floating.
111	uP_MD16	I/O	Leave floating.
112	uP_MA11	O	Leave floating.
113	uP_MD17	I/O	Leave floating.
114	uP_MA12	O	Leave floating.
115	uP_MD18	I/O	Leave floating.
116	uP_MA13	O	Leave floating.
117	uP_MD19	I/O	Leave floating.
118	uP_MA14	O	Leave floating.
119	uP_MD20	I/O	Leave floating.
120	uP_MA15	O	Leave floating.
121	uP_MD21	I/O	Leave floating.
122	uP_MA16	O	Leave floating.
123	uP_MD22	I/O	Leave floating.
124	uP_MA17	O	Leave floating.
125	uP_MD23	I/O	Leave floating.
126	uP_MA18	O	Leave floating.
127	DGND	I	Required. Digital Ground (0V)
128	uP_MA19	O	Leave floating.
129	uP_MD24	I/O	Leave floating.
130	uP_MA20	O	Leave floating.
131	uP_MD25	I/O	Leave floating.
132	uP_MA21	O	Leave floating.
133	uP_MD26	I/O	Leave floating.
134	uP_MA22	O	Leave floating.

J1C Pin #	Signal Name	I/O	Description
135	uP_MD27	I/O	Leave floating.
136	uP_MA23	O	Leave floating.
137	uP_MD28	I/O	Leave floating.
138	uP_MA24	O	Leave floating.
139	uP_MD29	I/O	Leave floating.
140	uP_MA25	O	Leave floating.
141	uP_MD30	I/O	Leave floating.
142	nAEN	O	Leave floating.
143	uP_MD31	I/O	Leave floating.
144	3.3V	I	Required. Power Supply (3.3V)

6.2 J1A Expansion Connector Unused Pin Treatments

J1A Pin #	Signal Name	I/O	Description
1	LCD_VSYNC	O	Leave floating.
2	LCD_HSYNC	O	Leave floating.
3	LCD_DCLK	O	Leave floating.
4		NC	Leave floating. No internal connection
5	LCD_MDISP	O	Leave floating.
6	LCD_VEEEN	O	Leave floating.
7	LCD_VDDEN	O	Leave floating.
8		NC	Leave floating. No internal connection
9	DGND	I	Required. Digital Ground (0V)
10	LCD_CLS	O	Leave floating.
11	LCD_SPS	O	Leave floating.
12	LCD_PSAVE	O	Leave floating.
13	LCD_SPL	O	Leave floating.
14	LCD_HRLP	O	Leave floating.
15		NC	Leave floating. No internal connection
16	LCD_REV	O	Leave floating.
17	uP_STATUS_1	O	Leave floating.
18	uP_STATUS_2	O	Leave floating.
19	uP_AC97_BITCLK	I/O	Leave floating.
20	uP_AC97_RESET	O	Leave floating.
21	uP_AC97_SYNC	O	Leave floating.
22	uP_AC97_SD_IN	I	Leave floating.
23	uP_AC97_SD_OUT	O	Leave floating.
24	DGND	I	Required. Digital Ground (0V)
25	A/D1	I	Leave floating.
26	A/D2	I	Leave floating.
27	AGND	I	Required. Analog Ground (0V)
28		NC	Leave floating. No internal connection
29		NC	Leave floating. No internal connection
30	3.3VA	I	Required. Analog Power Supply (3.3V)
31	CODEC_INL	I	Leave floating.
32	CODEC_INR	I	Leave floating.
33	CODEC_OUTL	O	Leave floating.
34	CODEC_OUTR	O	Leave floating.
35	AGND	I	Required. Analog Ground (0V)
36	TOUCH_LEFT	I	Leave floating.
37	TOUCH_RIGHT	I	Leave floating.
38	TOUCH_BOTTOM	I	Leave floating.
39	TOUCH_TOP	I	Leave floating.
40	3.3VA	I	Required. Analog Power Supply (3.3V)
41	R0	O	Leave floating.
42	R1	O	Leave floating.
43	R2	O	Leave floating.
44	DGND	I	Required. Digital Ground (0V)
45	R3	O	Leave floating.
46	R4	O	Leave floating.
47	R5	O	Leave floating.
48	G0	O	Leave floating.
49	G1	O	Leave floating.
50	G2	O	Leave floating.
51	G3	O	Leave floating.
52	G4	O	Leave floating.
53	G5	O	Leave floating.
54	B0	O	Leave floating.
55	DGND	I	Required. Digital Ground (0V)

J1A Pin #	Signal Name	I/O	Description
56	B1	O	Leave floating.
57	B2	O	Leave floating.
58	B3	O	Leave floating.
59	B4	O	Leave floating.
60	B5	O	Leave floating.
61	CF_nCE	O	Leave floating.
62	uP_PCC_RDYA	I	Leave floating. Internal pull up.
63	CPLD_GPIO_1	O	Leave floating.
64	CPLD_GPIO_2	O	Leave floating.
65		NC	Leave floating. No internal connection
66	DGND	I	Required. Digital Ground (0V)
67	uP_USB1_nOVR_CRNT - VBUS	I	Leave floating.
68		NC	Leave floating. No internal connection
69	uP_USB1_PWR_EN	O	Leave floating.
70		NC	Leave floating. No internal connection
71		NC	Leave floating. No internal connection
72	uP_USB1_M	I	Leave floating.
73	uP_USB1_P	I	Leave floating.
74	BUFF_nOE	O	Leave floating.
75		NC	Leave floating. No internal connection
76	BUFF_DIR_DATA	O	Leave floating.
77	DGND	I	Required. Digital Ground (0V)
78	MIC_IN	I	Leave floating.
79	POWER_SENSE1	O	Leave floating.
80	POWER_SENSE2	O	Leave floating.

6.3 J1B Expansion Connector Unused Pin Treatments

J1B Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	Leave floating. Internal pull down.
2	CPLD_TDO	O	Leave floating.
3	CPLD_TMS	I	Leave floating. Internal pull up.
4	CPLD_TDI	I	Leave floating. Internal pull up.
5	uP_PCC_nOE	O	Leave floating.
6	uP_PCC_nWE	O	Leave floating.
7	uP_PCC_nIORD	O	Leave floating.
8	uP_PCC_nIOWR	O	Leave floating.
9	DGND	I	Required. Digital Ground (0V)
10	uP_PCC_RESET	O	Leave floating.
11	PCC_nCE1B	O	Leave floating.
12	PCC_nCE2B	O	Leave floating.
13	PCC_nIOIS16	I	Leave floating.
14	uP_PCC_RDYB	I	Leave floating. Internal pull up.
15	uP_PCC_nWAIT	I	Leave floating. Internal pull up.
16	uP_PCC_BVD2	I	Leave floating. Internal pull up.
17	uP_PCC_BVD1	I	Leave floating. Internal pull up.
18	PCC_nCD2	I	Leave floating. Internal pull up.
19	PCC_nCD1	I	Leave floating. Internal pull up.
20	uP_PCC_REG	O	Leave floating.
21	DGND	I	Required. Digital Ground (0V)
22	PCC_VS1	I	Leave floating. Internal pull up.
23	uP_PCC_VS2	I	Leave floating. Internal pull up.
24	PCC_nDRV	O	Leave floating.
25	uP_PCC_PCDIR	O	Leave floating.
26	uP_DQM3	O	Leave floating.
27	uP_DQM2	O	Leave floating.
28	uP_DQM1	O	Leave floating.
29	uP_DQM0	O	Leave floating.
30	uP_IRTX	O	Leave floating.
31	uP_IRRX	I	Leave floating. Internal pull up.
32	DGND	I	Required. Digital Ground (0V)
33	MFP1 - uP_KEY_COL0	I/O	Leave floating.
34	MFP2 - uP_KEY_COL1	I/O	Leave floating.
35	MFP3 - uP_KEY_COL2	I/O	Leave floating.
36	MFP4 - uP_KEY_COL3	I/O	Leave floating.
37	MFP5 - uP_KEY_COL4	I/O	Leave floating.
38	MFP6 - uP_KEY_COL5	I/O	Leave floating.
39	MFP7 - uP_KEY_COL6	I/O	Leave floating.
40	MFP8 - uP_KEY_COL7	I/O	Leave floating.
41	uP_UARTB_TX	O	Leave floating.
42	uP_UARTB_RX	I	Leave floating. Internal pull up.
43	uP_UARTB_CTS	O	Leave floating. Internal pull down.
44	DGND	I	Required. Digital Ground (0V)
45	uP_UARTB_RTS	O	Leave floating.
46	uP_UARTC_TX	O	Leave floating.
47	uP_UARTC_RX	I	Leave floating. Internal pull up.
48	MFP9 - uP_MMC_CMD	I/O	Leave floating.
49	MFP10 - uP_MMC_nSELECT	I/O	Leave floating.
50	MFP11 - uP_MMC_DATA	I/O	Leave floating.
51	MFP12 - uP_MMC_CLK	I/O	Leave floating.
52	MFP13 - uP_SCI_CLK	I/O	Leave floating.
53	MFP14 - uP_A25 - SCI_IO	I/O	Leave floating. Internal pull down.
54	MFP15 - uP_SCI_MEDCHG	I/O	Leave floating. Internal pull down.
55	DGND	I	Required. Digital Ground (0V)

J1B Pin #	Signal Name	I/O	Description
56	MFP16 - uP_SCI_DETECT	I/O	Leave floating. Internal pull down.
57	MFP17 - uP_SCI_VCCEN	I/O	Leave floating.
58	MFP18 - uP_SCI_RESET	I/O	Leave floating. Internal pull up.
59	MFP19 - PWMEN0	I/O	Leave floating.
60	MFP20 – PCC_nCE1A	O	Leave floating.
61	MFP21 - PWM0	I/O	Leave floating.
62	MFP22 – PCC_nCE2A	O	Leave floating.
63	MFP23 - uP_BMI_CLK	I/O	Leave floating.
64	MFP24 - uP_BMI_IO_SWI	I/O	Leave floating.
65	MFP25 - uP_nBATCHG	I/O	Leave floating. Internal pull up.
66	DGND	I	Required. Digital Ground (0V)
67	MFP26 - uP_BATOK	I/O	Leave floating. Internal pull up.
68	MFP27 - PWMI	I/O	Leave floating.
69	MFP28 - uP_nMCS2	I/O	Leave floating.
70	MFP29 - uP_SDCKE	I/O	Leave floating.
71	MFP30 - uP_nSDCS2	I/O	Leave floating.
72	MFP31 - uP_nSDCS1	I/O	Leave floating.
73	MFP32 - uP_nEXTPWR	I/O	Leave floating. Internal pull down.
74	MFP33 - uP_BUZZER	I/O	Leave floating.
75	MFP34 - MONO_OUT	I/O	Leave floating.
76	MFP35 - PC_BEEP	I/O	Leave floating.
77	DGND	I	Required. Digital Ground (0V)
78	MFP36 - CD_IN_L	I/O	Leave floating.
79	MFP37 - CD_IN_R	I/O	Leave floating.
80	MFP38 - CD_GND	I/O	Leave floating.

7 Mechanical Specifications

7.1 Interface Connectors

The LH7A400-10 Card Engine connects to a PCB board through an industry standard 144-pin SODIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SODIMM Connector must be 3.7mm mating height.

IMPORTANT NOTE: If the product requires safe removal of the Card Engine during the product's lifecycle, the design should allow at least 7.65 mm (0.30") of clearance beyond the Card Engine's back edge (opposite of the SODIMM connector) before placing any baseboard components. This extra space on the baseboard provides room to use an extractor tool to safely remove the Card Engine from the baseboard without flexing the PCB. Please see Logic's White Paper 318 *Card Engine Insertion and Extraction Procedure* for more details.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(86)	DF12(3.0)-80DS-0.5V(86)
J1C	Amp	Card Edge	390112-1

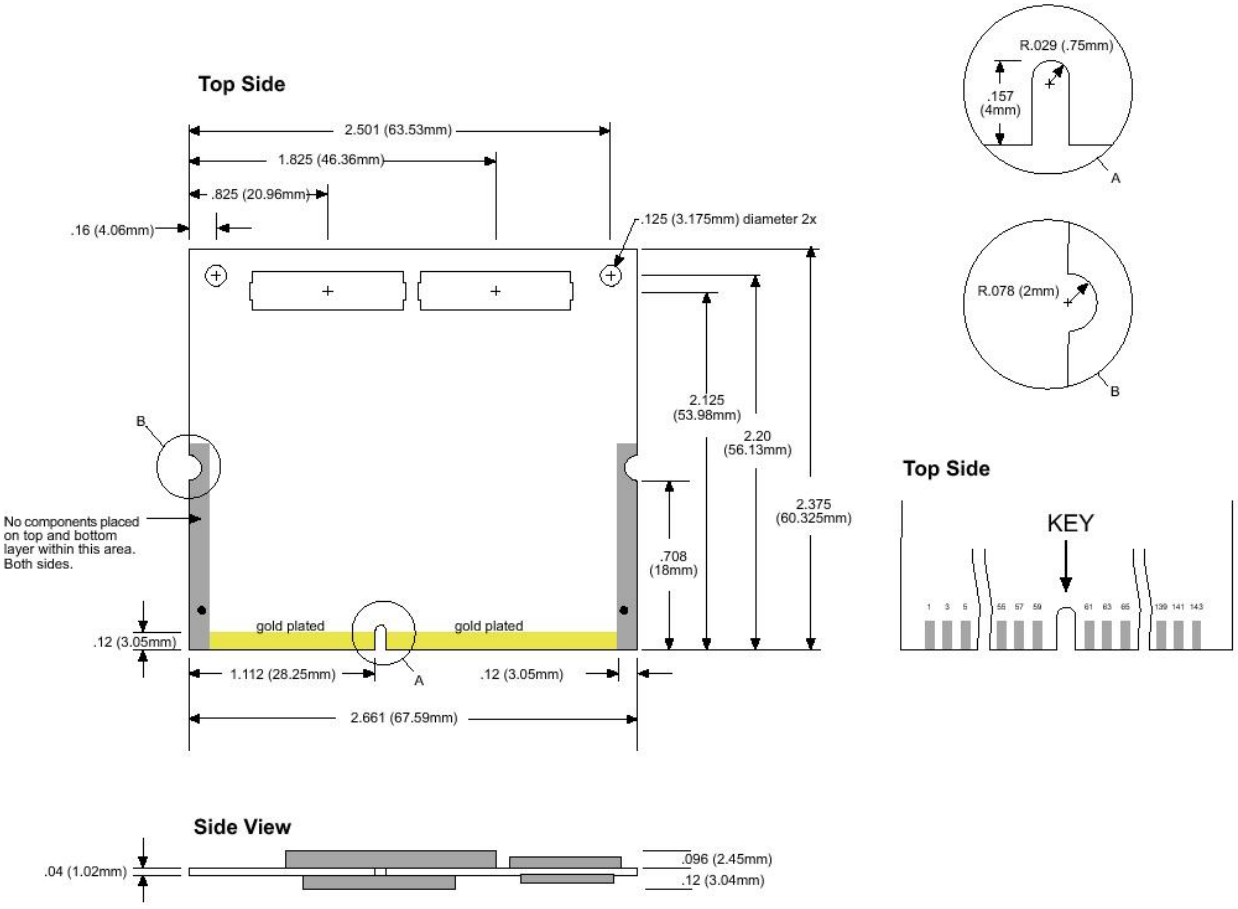

Figure 7.1: Card Engine Mechanical Drawing

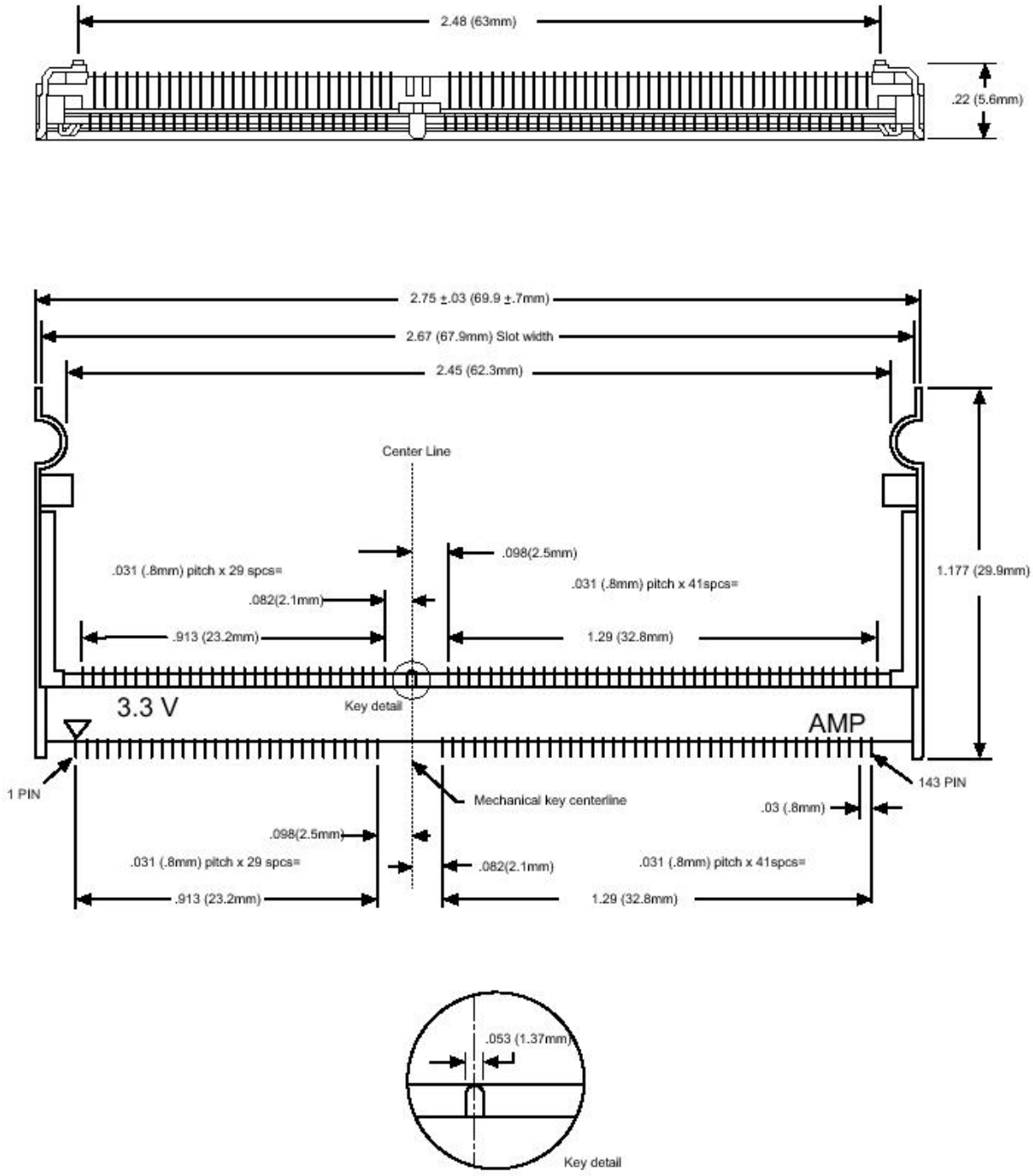

Figure 7.2: SODIMM Connector Specification

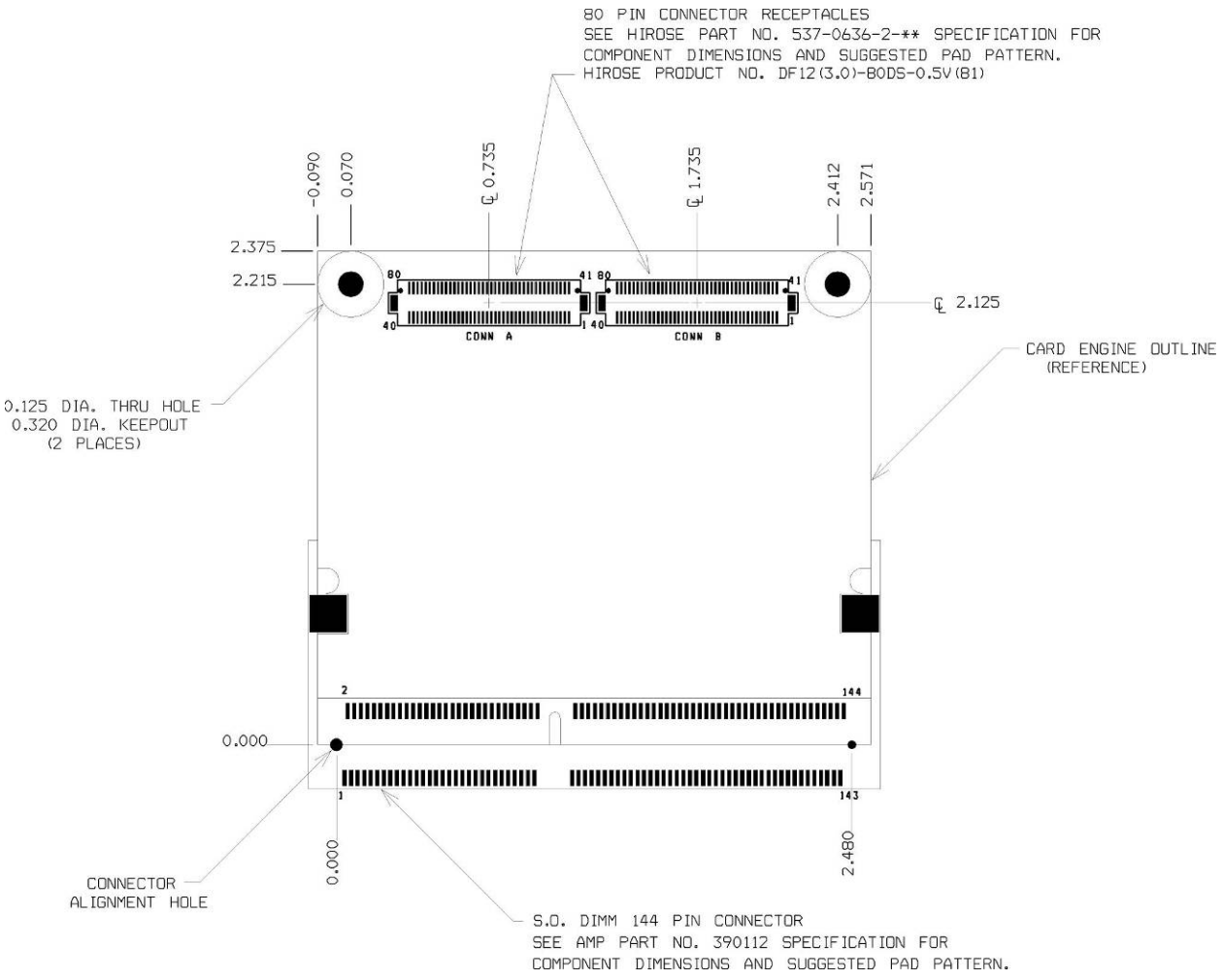

Figure 7.3: Recommended PCB Layout

