Logic Product Development
Technical Data

Logic Part Number: 1008209
Rev. A, 10/2007

MPC8360 COM Express SOM Hardware Specification

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PRODUCT BRIEF:
Logic :: Freescale

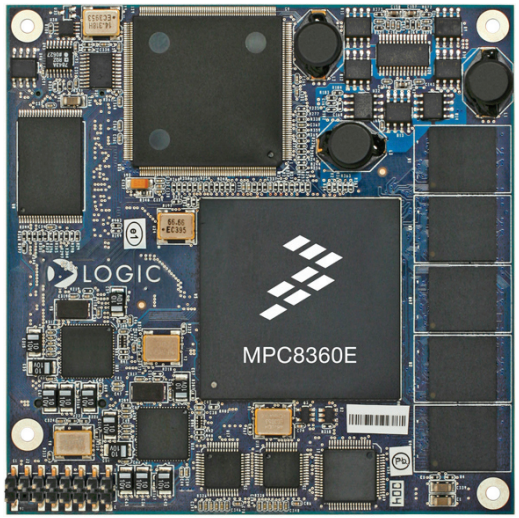
MPC8360 COM Express System on Module

The MPC8360 COM Express System on Module (SOM) is a compact, product-ready hardware and software solution that fast forwards embedded designs.

The MPC8360 SOM adheres to the COM Express Compact form factor and is based on the Type III pin-out specification. This combination offers the essential features for industrial, networking, and medical applications. Using a SOM allows engineers to design a custom baseboard that meets their specific needs and is compatible with other Logic SOMs. This compatibility makes it easy for developers to upgrade their product for greater functionality and performance—while still using their original baseboard design.

By starting with the corresponding Zoom™ PowerQUICC™ Development Kit, developers can write application software on the same hardware that will be used in the final product.

The MPC8360 PowerQUICC™ processor from Freescale Semiconductor provides both control and communications processing in a single chip, making it a cost-effective solution for any product requiring deterministic industrial networking protocols.



MPC8360 COM Express SOM

Designing a product around Logic's SOM allows developers to easily combine their core technologies with the high performance of the MPC8360 PowerQUICC™ processor.

MPC8360 COM EXPRESS :: HIGHLIGHTS:

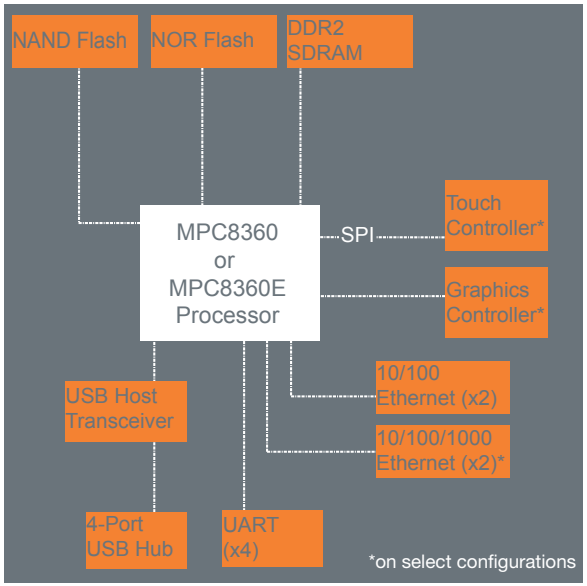
+ Product-ready SOM with the Freescale PowerQUICC™ MPC8360 processor running at 400 MHz or MPC8360E processor running at 667 MHz
+ COM Express Compact form factor 95 mm x 95 mm x 14.5 mm
+ Long product life-cycle
+ U-Boot bootloader installed in flash
+ Linux Board Support Packages (BSPs)
+ 0 ˚C to 70 ˚C (commercial temp) or -40 ˚C to 85 ˚C (industrial temp)
+ RoHS compliant

ZOOM™ PowerQUICC™ KIT :: FEATURES:

+ Application baseboard
+ MPC8360 COM Express SOM (COMMPC8360E-10-2752FCR)
+ Production-ready QUICCEngine™ micro-code for PROFIBUS, IEEE(R) 1588, and Ethernet PowerLink available from third-parties
+ Necessary accessories to immediately get up and running
+ Kit available from Freescale (MPC8360E-RDK)
+ See Zoom™ PowerQUICC™ Development Kit product brief for more information

LOGIC

MPC8360 COM Express Block Diagram



MPC8360 COM Express Ordering Information

Model Number	Speed (MHz)	SDRAM (MB)	NAND Flash (MB)	NOR Flash (MB)	Graphics/ Touch	Ethernet	Temperature
COMMPC8360-10-1652LCR	400	128	64	8	N	10/100	0 ˚C to 70 ˚C
COMMPC8360E-10-2752FCR	667	256	64	8	Y	10/100/1000	0 ˚C to 70 ˚C

+Contact Logic for availability of industrial temp configurations.

ZOOM™ PowerQUICC™ Development Kit Ordering Information

Model Number	COM Express Configuration	Recommended Resale
MPC8360E-RDK	COMMPC8360E-10-2752FCR	$999

LOGIC WEBSITE :: DESIGN RESOURCES:

+Logic Technical Support : http://www.logicpd.com/support/
+Technical Discussion Group : http://www.logicpd.com/support/tdg/
+Frequently Asked Questions (FAQ) : http://www.logicpd.com/support/faq/
+For more information contact Logic Sales : product.sales@logicpd.com

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freescale™ semiconductor

Product Features

Processor
+Freescale PowerQUICC™ MPC8360 processor running at 400 MHz or MPC8360E processor running at 667 MHz

SDRAM Memory
+DDR2; 128, 256, 512 MB, or 1 GB
+ECC support

Flash Memory
+NOR flash; 8 or 16 MB (8 MB standard)
+NAND flash; 64 or 128 MB (64 MB standard)

Display
+Programmable color graphics controller (Fujitsu MB86277)
+Built-in driver supports up to 1024 x 768 with LVDS interface
+LVDS can be converted to 18-bit LCD on baseboard

Touch Screen
+Integrated 4-wire touch screen controller

Network Support
+Two 10/100 Base-T Ethernet controllers for application/debug
+Two 10/100/1000 Base-T Ethernet controllers for application/debug

PC Card Expansion
+32-bit PCI connection

USB
+Four USB 2.0 full-speed host interfaces

Serial Ports
+Four 16C550 compatible UARTs

GPIO
+Programmable I/O depending on peripheral requirements

Software
+U-Boot bootloader
+Linux BSP

Mechanical
+COM Express Compact form factor 95 mm wide x 95 mm long x 14.5 mm high

RoHS Compliant

PN: 1007946 Rev B

1.2 Acronyms

ACI	Audio CODEC Interface
ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CCM	Clock Controller Module
CPLD	Complex Programmable Logic Device
CSPI	Configurable Serial Peripheral Interface
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FEC	Fast Ethernet Controller
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I2S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IPIC	Integrated Programmable Interrupt Controller
IRQ	Interrupt Request
LCD	Liquid Crystal Display
MMC	Multi Media Card
NC	No Connect
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RCW	Reset Configuration Words
RISC	Reduced Instruction Set Computer
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System on Chip
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Scope of Document

This Hardware Specification is unique to the design and use of the MPC8360 COM Express SOM as designed by Logic and does not intend to include information outside of that scope. Detailed information about the Freescale MPC8360E PowerQUICC processor or any other device component on the COM Express SOM can be found in their respective manuals and specification documents. Specific documents mentioned within this Hardware Specification include:

- *MPC8360 COM Express SOM Schematics* (available from Logic at http://www.logicpd.com/auth/)
- *MPC8360E PowerQUICC™ II Pro Integrated Communications Processor Family Reference Manual* (hereafter refered to as *MPC8360E Processor Reference Manual*, available from Freescale at http://www.freescale.com/PowerQUICC)
- *MB86277 <MINT> Graphics Controller Specifications* (available from Fujitsu's website)
- *USB 2.0 Specification* (available from USB.org at http://www.usb.org/developers/docs/)
- *PCI Local Bus Specification*

1.4 COM Express Interface

Logic's common COM Express interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common COM Express footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of a product design onto the COM Express SOM reduces any long-term risk of obsolescence. If a component on the COM Express SOM design becomes obsolete, Logic will design for an alternative part that is transparent to the end-product. Furthermore, Logic tests all modules prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

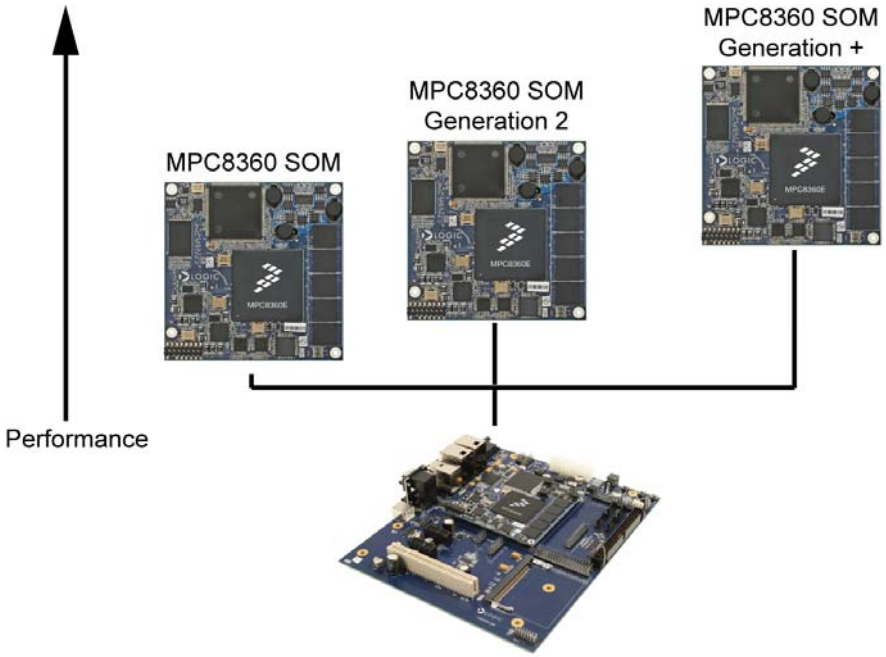

Figure 1.1: COM Express SOM Advantages

1.5 MPC8360 COM Express SOM Block Diagram

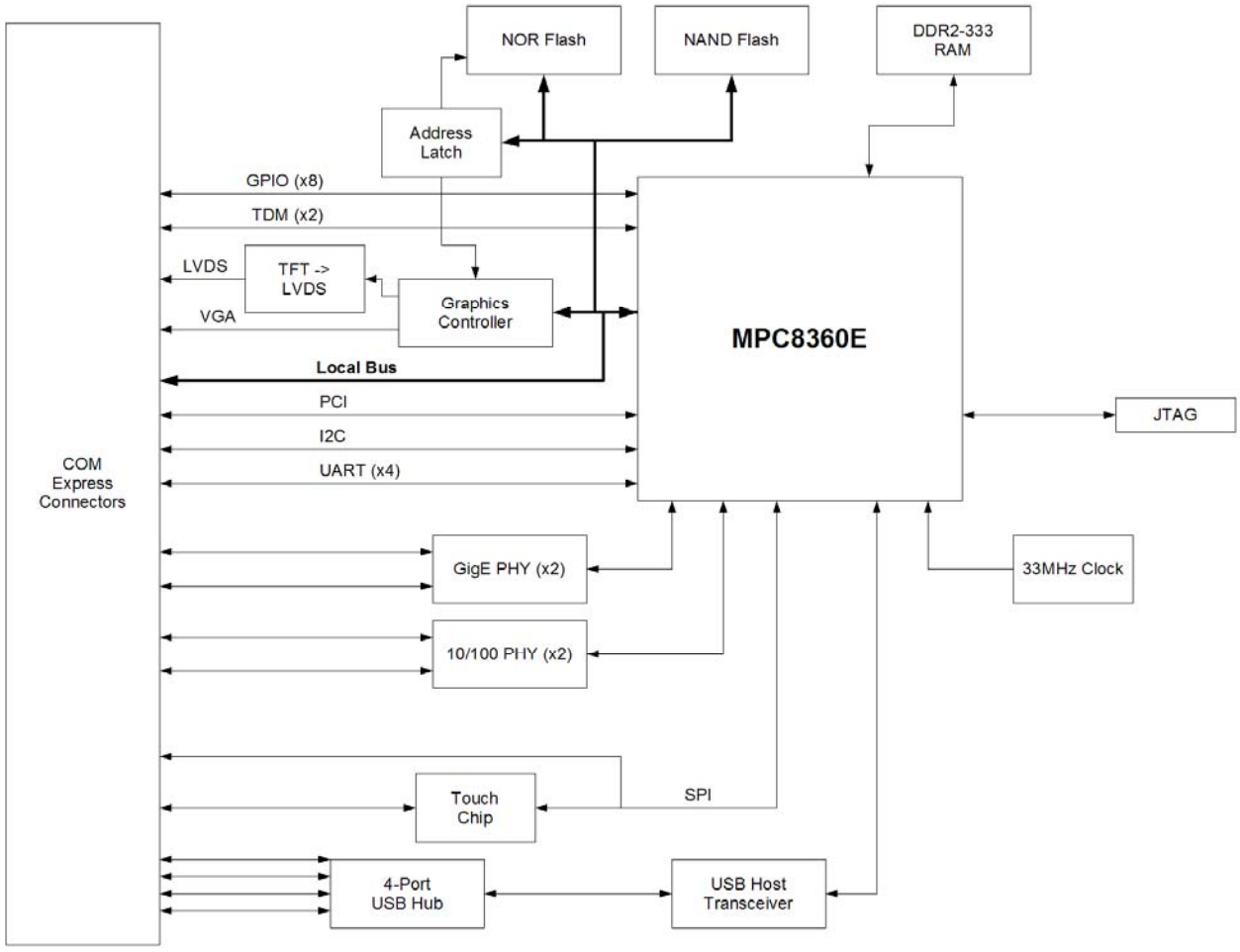

Figure 1.2: MPC8360 COM Express SOM Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC 12V Supply Voltage	12V	VSS-0.3 to 15	V
Standby Voltage	VCC5VSB	VSS-0.3 to 5.5	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the SOM and its components.

1.6.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC 12V Input Voltage	9.6	12	14.4	V	
DC 12V Active Current	—	—	—	mA	
DC 12V Suspend Current	—	—	—	mA	
DC 12V Standby Current	—	—	—	mA	
Standby Voltage	4.5	5	5.5	V	
DC 5V Active Current	—	—	—	mA	
DC 5V Suspend Current	—	—	—	mA	
DC 5V Standby Current	—	—	—	mA	
Commercial Operating Temperature	0	25	70	°C	
Storage Temperature	-40	25	85	°C	
Dimensions	—	95 x 95 x 14.5	—	mm	
Weight	—	65	—	Grams	1
Connector Insertion/Removal	—	30	—	Cycles	
Input Signal High Voltage	0.8 x VREF	—	VREF	V	2
Input Signal Low Voltage	GND	—	0.2 x VREF	V	2
Output Signal High Voltage	0.8 x VREF	—	VREF	V	2
Output Signal Low Voltage	GND	—	0.2 x VREF	V	2

Notes:

1. May vary depending on COM Express configuration.
2. VREF represents the peripheral I/O supply reference for the specific CPU voltage rail.

2 Electrical Specification

2.1 Microcontroller

2.1.1 MPC8360E Microcontroller

The MPC8360 COM Express SOM uses Freescale's highly integrated MPC8360E processor. This device features the e300c1 core and provides many integrated on-chip peripherals, including (as listed in Freescale's *MPC8360E Processor Reference Manual*):

- e300c1 Power Architecture™ processor core
  - Enhanced version of the MPC603e core
  - High-performace, superscaler processor core with a four-stage pipeline and low interrupt latency times
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache and 32-Kbyte data cache with lockable capabilities
  - Dynamic power management
  - Enhanced hardware program debug features
  - Software-compatible with Freescale processor families implementing Power Architecture technology
  - Separate PLL that is clocked by the system bus clock
- QUICC Engine 2.0 block
  - Two 32-bit RISC controllers for flexible support of the communications peripherals with the following features:
  - One clock per instruction
  - Separate PLL for operating frequency that is independent of system's bus and core frequency for power and performance optimization
  - 32-bit instruction object code
  - Executes code from internal ROM or RAM
  - 32-bit arithmetic logic unit (ALU) data path
  - Modular architecture allowing for easy functional enhancements
  - Slave bus for CPU access of registers and multiuser RAM space
  - 48 Kbytes of instruction RAM
  - 48 Kbytes of multiuser data RAM
  - QE peripheral request interface (for SEC, PCI, and IEEE Std. 1588™)
- Eight universal communication controllers (UCCs)
- ATM controller
- Universal serial bus (USB) controller
- Many general purpose I/O (GPIO) signals
- 2 serial DMA channels
- Time slot assigner and 8 TDM serial interfaces

See Freescale's *MPC8360E Processor Reference Manual* for additional information.

IMPORTANT NOTE: Please visit http://www.freescale.com/PowerQUICC for errata on the MPC8360E processor and documentation.

2.1.2 MPC8360E Microcontroller Block Diagram

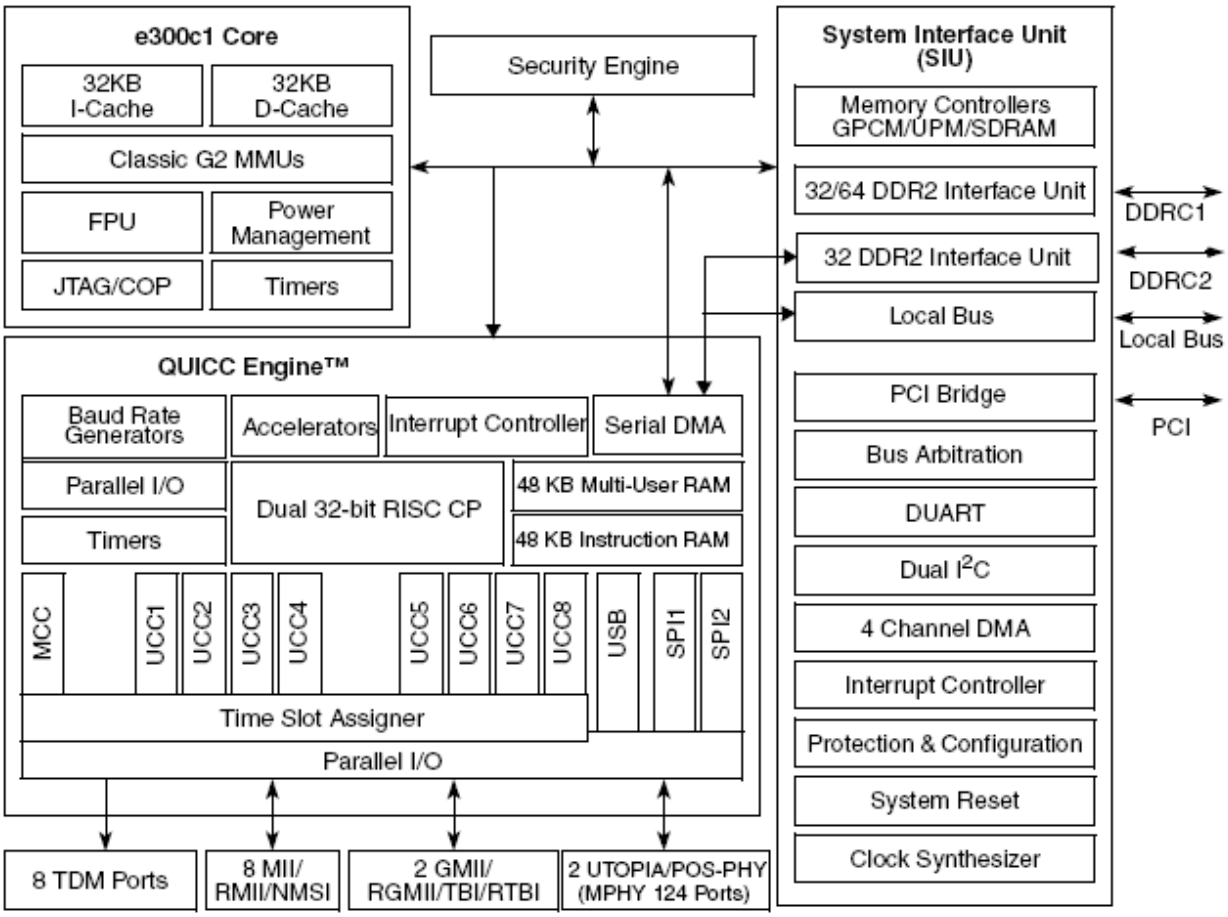

Figure 2.1: MPC8360E Microcontroller Block Diagram

2.2 Clocks

The MPC8360E requires an oscillator to enable proper internal timing. A 33.33 MHz oscillator is used to generate the processor's internal clocks through a series of PLLs. To generate the core CPU clock, the 33.33 MHz signal is run through a System PLL controlled by the value set in the Reset Configuration Words. The output of the System PLL is used to supply the Core PLL as well as the timing units for the Local Bus and the DDR memory controller. There is also a separate PLL for the QUICC Engine clock which is also based off the 33.33 MHz oscillator input.

IMPORTANT NOTE: Please see Freescale's *MPC8360E Processor Reference Manual* for additional information about processor clocking.

The MPC8360E clock speeds are set in the Reset Configuraton Words (RCW). The RCW can be changed to allow different clock speeds.

The MPC8360 COM Express SOM provides two external bus clocks, uP_LCLK1 and uP_LCLK2. These clocks are enabled by default. uP_LCLK0 is the clock used for the onboard graphics controller. uP_SDCLK[0:4]+/- serve as the DDR2 SDRAM clocks on the MPC8360 COM Express SOM.

2.3 Memory

2.3.1 DDR2 SDRAM

The MPC8360 COM Express SOM uses a 64-bit memory bus to interface to DDR2 SDRAM. The MPC8360 COM Express SOM can handle configurations of 128 Mbytes, 256 Mbytes, 512 Mbytes, or 1 Gbytes SDRAM in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on the COM Express SOM included in the Development Kit is 256 Mbytes.

The MPC8360 COM Express SOM also has support for multi-bit error detection and single bit error detection and correction ECC.

2.3.2 Direct Memory Access

The Freescale MPC8360E microcontroller has a direct memory access (DMA) controller which contains 4 DMA channels for use with internal peripherals to achieve highly efficient data throughput. For more information on using the DMA interface, please refer to the *MPC8360E Processor Reference Manual*.

2.3.3 NOR Flash

The MPC8360 COM Express SOM uses a 16-bit memory bus to interface to NOR flash memory. The onboard memory can be configured as 8 or 16 Mbytes to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 8 Mbytes on the COM Express SOM included in the Zoom PowerQUICC Development Kit.

2.3.4 NAND Flash

The MPC8360 COM Express SOM uses an 8-bit memory bus to interface to NAND flash. The product supports configurations of 64 or 128 Mbytes. The COM Express SOM included in the standard Zoom PowerQUICC Development Kit contains 64 Mbytes of NAND flash.

It is possible to expand the SOM's non-volatile storage capability by adding external NOR flash or NAND flash. Please refer to the *MPC8360 COM Express SOM Schematics* for reference designs or contact Logic for other possible peripheral designs.

2.4 Ethernet Controllers

2.4.1 10/100/1000

The MPC8360 COM Express SOM uses two Broadcom BCM5481 Ethernet transceivers to provide an easy-to-use Gigabit networking interface. Please note the TRDx+/- pairs must be routed as differential pairs on the baseboard printed circuit board (PCB).

2.4.2 10/100

Two National DP83848 Ethernet transceivers provide the 10/100 networking interface on the MPC8360 COM Express SOM. Please note the TD+/- and RD+/- pairs must be routed as differential pairs on the baseboard PCB.

2.5 Display Interface

The MPC8360 COM Express SOM uses the Fujitsu MB86277 (MINT) graphics controller. The MINT supports display resolutions up to 1024 x 768 at 24 bpp. Please refer to the *MB86277 <MINT> Graphics Controller Specifications* for further information on the graphics controller. The signals from the MINT graphics controller are provided in 24-bit digital RGB and analog RGB. The digital RGB is converted to LVDS format. Both LVDS and analog RGB are available through the expansion connectors. Logic has written drivers for numerous display panels of different types and sizes. Please contact Logic before selecting a panel for your application.

2.6 Serial Interfaces

The MPC8360 COM Express SOM comes with the following serial channels: UART1, UART2, UART3, UART4, SPI, and I2C. If additional serial channels are required, please contact Logic for reference designs. Please see the *MPC8360E Processor Reference Manual* for further information regarding serial communications.

2.6.1 UART1

UART1 has been configured to be the MPC8360 Development Kit's main serial port. It is an asynchronous PC16550D-compatible UART. This UART provides a high-speed serial interface that uses First In / First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the COM Express SOM are Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example baseboard reference design with the Zoom PowerQUICC Development Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data transfer rates.

The UART1 baud rate is set by default to 115.2 Kbits/sec, though it supports most common serial baud rates.

2.6.2 UART2

Serial Port UART2 is an asynchronous PC16550D-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the MPC8360 COM Express SOM are TTL level signals, not RS232 level signals. The UART2 baud rate can also be set to most common serial baud rates.

2.6.3 UART3

Serial Port UART3 is an asynchronous UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the MPC8360 COM Express SOM are TTL level signals, not RS232 level signals. The UART3 baud rate can also be set to most common serial baud rates.

2.6.4 UART4

Serial Port UART4 is an asynchronous UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the MPC8360 COM Express SOM are TTL level signals, not RS232 level signals. The UART4 baud rate can also be set to most common serial baud rates.

2.6.5 SPI

There are two Serial Peripheral Interface (SPI) ports on the MPC8360 COM Express SOM. The first port communicates with the onboard EEPROM and touch chip. It is also available through the expansion connectors. The second port communicates to the Ethernet transceivers. Please see the *MPC8360E Processor Reference Manual* for further information.

2.6.6 I2C

The MPC8360 COM Express SOM supports two external I2C ports. For both ports, the clock and data signals have 2.2K pull-up resistors to 3.3V. Please see the *MPC8360E Processor Reference Manual* for further information.

2.7 USB Interface

The MPC8360 COM Express SOM supports four USB 2.0 full-speed host ports. All ports can operate up to 12 Mbytes/sec. The MPC8360E processor has an internal USB controller. The MPC8360 COM Express SOM has an external NXP ISP1105 transceiver to support a single port. The single port coming out of the ISP1105 is fed into a NXP ISP1520 4-port hub. For more information on using the USB interface, please see the *MPC8360E Processor Reference Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the MPC8360 COM Express SOM, additional impedance matching circuitry may be required on the USBx+ and USBx- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with a 90-ohm differential impedance. Refer to the *USB 2.0 Specification* for detailed information.

2.8 ADC/Touch Interface

The MPC8360 COM Express SOM uses an Analog Devices AD7843 for the touch screen controller (TSC). The controller includes a 12-bit analog-to-digital converter (ADC). This TSC is used to support standard 4-wire resistive touch panels. The TSC has two A/D signals that are externally available through the expansion connectors. The device is connected to the CPU by the SPI interface.

2.9 PCI Interface

The MPC8360E processor is compatible with the *PCI Local Bus Specification*, Rev. 2.2. The MPC8360 COM Express SOM operates in host mode. Please refer to the *MPC8360E Processor Reference Manual* for more information.

2.10 General Purpose I/O

Logic designed the MPC8360 COM Express SOM to be flexible and provide multiple options for digital General Purpose I/Os (GPIO). There are numerous digital GPIO pins on the MPC8360 COM Express SOM that interface to the MPC8360E processor. See the “Pin Descriptions and Functions” Section of this Hardware Specification for more information. If certain peripherals are not desired, such as UARTs or PCI, then multiple GPIO pins become available for custom use.

2.11 Expansion/Feature Options

The MPC8360 COM Express SOM was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user’s design. It is possible for a user to

expand the SOM's functionality even further by adding local bus devices. Logic has experience implementing additional options, including audio codecs, Ethernet ICs, co-processors, and components on SOMs. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The MPC8360 COM Express SOM was designed to meet multiple applications for users with specific design and budget requirements. As a result, this SOM supports a variety of embedded operating systems and supports the following custom hardware configurations:

- Flexible memory footprint: 128, 256, 512 Mbytes, or 1 Gbyte DDR2 SDRAM
- Flexible NOR flash footprint: 8 or 16 Mbytes NOR flash
- Flexible NAND flash footprint: 64 or 128 Mbytes NAND flash
- Optional Broadcom BCM5481 10/100/1000 Ethernet transceiver(s)
- Optional National DP83848 10/100 Ethernet transceiver(s)
- Optional Fujitsu MB86277 (MINT) graphics controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

The MPC8360 COM Express SOM has a reset input (uP_nPORESET) and a reset output (uP_nSRESET). External devices use uP_nPORESET to assert reset to the product. The SOM uses uP_nSRESET to indicate to other devices that the SOM is in reset.

3.2.1 Master Reset (uP_nPORESET)—Reset Input

Logic suggests that custom designs implementing the MPC8360 COM Express SOM specify the uP_nPORESET signal as the “pin hole” reset used in commercial embedded systems. The uP_nPORESET triggers a power-on-reset event to the MPC8360E processor and resets the entire CPU.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition. Powering-up in a low or bad power condition will cause data corruption and possible temporary system lockup.

A low pulse on the uP_nPORESET signal, asserted by an external source (for example, the reset button on the custom design application) will bring uP_nPORESET low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external uP_nPORESET signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the uP_nPORESET signal, analog or digital, use de-bouncing to generate a clean, one-shot reset signal.

3.2.2 SOM Reset (uP_nSRESET)—Reset output

All hardware peripherals should connect their hardware-reset pin to the uP_nSRESET signal on the expansion connector, unless the peripheral is needed to fetch the Reset Configuration Words (RCW). If needed for the RCW, the peripheral should be connected to uP_nPORESET. Internally all MPC8360 COM Express SOM peripheral hardware reset pins are connected to the uP_nSRESET net (except NOR flash because of the power-up sequence).

3.3 Interrupts

The MPC8360 COM Express SOM uses the integrated programmable interrupt controller (IPIC). The IPIC prioritizes and manages interrupts from both internal and external sources. Refer to Freescale's *MPC8360E Processor Reference Manual* for further information on using interrupts.

3.4 JTAG Debugger Interface

The JTAG connection on the MPC8360 COM Express SOM allows recovery of corrupted flash memory and real-time application debug. There are several third-party JTAG debuggers available for Freescale microcontrollers. The following signals make up the JTAG interface to the MPC8360 COM Express SOM: uP_TDI, uP_TMS, uP_TCK, uP_TDO, nCKSTOP_OUT, nCKSTOP_IN, COP_nTRST, and uP_nHRESET. These signals interface directly to a 16-pin 0.1" connector, shown as reference designator J2 on the *MPC8360 COM Express SOM Schematics*.

3.5 Power Management

3.5.1 System Power Supplies

The MPC8360 COM Express SOM has two power areas: 12V and VCC5VSB. All power areas are inputs to the MPC8360 COM Express SOM.

3.5.1.1 12V

The 12V input is the main source of power for the MPC8360 COM Express SOM. This input expects a voltage between 9.6V and 14.4V, with 12V as the standard. The 12V input is passed through several buck converters to create all onboard voltages. This supply must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification", unless experiencing power down or critical power conditions.

3.5.1.2 VCC5VSB

The VCC5VSB voltage powers the power button circuit. The baseboard should provide 5V to VCC5VSB at all times. VCC5VSB also generates 5V for the USB hub circuit. VCC5VSB must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification".

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The MPC8360 COM Express SOM was designed to keep these aspects in mind while providing maximum flexibility in software and system integration.

On the MPC8360 COM Express SOM there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states (dynamic power management, shutting down unused blocks, software-controlled power-down states), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel). These settings are typically initialized in the startup software routines and may be later modified in the operating system and

application software. Information for these items can be found in the appropriate documents such as the Freescale *MPC8360E Processor Reference Manual* or the specific software BSP manual.

3.6 ESD Considerations

The MPC8360 COM Express SOM was designed to interface to a customer's peripheral board, while remaining low cost and adaptable to different applications. As such, the MPC8360 COM Express SOM does not provide any onboard ESD protection circuitry—this must be provided by the end-product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory and I/O Mapping

On the Freescale MPC8360E microcontroller, all address mapping for the local bus and external chip selects is configurable. Please consult Freescale's *MPC8360E Processor Reference Manual* for details.

DDR2 SDRAM

The MPC8360E processor contains dedicated chip selects for the DDR2 SDRAM interface. MEMC1_MCS0 is used as the chip select for the DDR2 SDRAM on the MPC8360 COM Express SOM.

Local Bus

Mapped chip select signals for the Local Bus are available as outputs from the microcontroller and are assigned as follows:

LCS0* = NOR flash
LCS1 = NAND flash
LCS2 = Graphics Controller
LCS3* = Available for use by an off-board external device (BOOT_nCS)
LCS4 = Available for use by an off-board external device (uP_nLCS4)
LCS5 = Available for use by an off-board external device (uP_nLCS5)

*LCS0 and LCS3 connection is controlled by MODE3. When MODE3 is high, LCS0 connects to NOR flash and LCS3 goes to the expansion connectors; When MODE3 is low, LCS0 connects to the expansion connectors and LCS3 goes to the NOR flash.

5 Pin Descriptions and Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of uBoot (bootloader). Many of the signals defined in the tables below can be configured as input or outputs—all GPIOs on the MPC8360E processor can be configured as input, output, input/output, or disabled—and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

5.1 J1A Connector 220-Pin Descriptions

5.1.1 J1A Row A Pin Descriptions

J1A Pin#	Signal Name	I/O	Voltage	Description
A1	GND	I	GND	Ground. Connect to digital ground.
A2	ENET1_TRD3-	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 3. Route as differential pair with ENET1_TRD3+. Requires external magnetics. See example FlexATX baseboard design for reference components.
A3	ENET1_TRD3+	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 3. Route as differential pair with ENET1_TRD3-. Requires external magnetics. See example FlexATX baseboard design for reference components.
A4	ENET1_LED2	O	3.3V	This signal is used with ENET1_LED1 to determine the Ethernet 1 link speed. See Section 5.3.
A5	ENET1_LED1	O	3.3V	This signal is used with ENET1_LED2 to determine the Ethernet 1 link speed. See Section 5.3.
A6	ENET1_TRD2-	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 2. Route as differential pair with ENET1_TRD2+. Requires external magnetics. See example FlexATX baseboard design for reference components.
A7	ENET1_TRD2+	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 2. Route as differential pair with ENET1_TRD2-. Requires external magnetics. See example FlexATX baseboard design for reference components.
A8	NC	NC	NA	No connect. Do not connect.
A9	ENET1_TRD1-	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 1. Route as differential pair with ENET1_TRD1+. Requires external magnetics. See example FlexATX baseboard design for reference components.
A10	ENET1_TRD1+	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 1. Route as differential pair with ENET1_TRD1-. Requires external magnetics. See example FlexATX baseboard design for reference components.
A11	GND	I	GND	Ground. Connect to digital ground.
A12	ENET1_TRD0-	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 0. Route as differential pair with ENET1_TRD0+. Requires external magnetics. See example FlexATX baseboard design for reference components.
A13	ENET1_TRD0+	I/O	3.3V	Gigabit Ethernet 1 transmit/receive pair 0. Route as differential pair with ENET1_TRD0-. Requires external magnetics. See example FlexATX baseboard design for reference components.
A14	ENET1_CT	O	2.5V	Gigabit Ethernet 1 center tap. This signal is the reference voltage for Etherenet 1 magnetics center tap. See example FlexATX baseboard design for reference components.
A15	GPIO_PD13	I/O	3.3V	Reserved for future use. Connected to GPIO_PD13 of the MPC8360. See Note 1 at the bottom of this table.
A16	NC	NC	NA	Reserved for future use. Do not connect.
A17	NC	NC	NA	Reserved for future use. Do not connect.
A18	GPIO_PD19	I/O	3.3V	Reserved for future use. Connected to GPIO_PD19 of the MPC8360. See Note 1 at the bottom of this table.
A19	NC	NC	NA	Reserved for future use. Do not connect.
A20	NC	NC	NA	Reserved for future use. Do not connect.
A21	GND	I	GND	Ground. Connect to digital ground.

J1A Pin#	Signal Name	I/O	Voltage	Description
A22	NC	NC	NA	Reserved for future use. Do not connect.
A23	NC	NC	NA	Reserved for future use. Do not connect.
A24	nPS_ON	O	3.3V	Active low. This signal is used to turn the 12V power rail on and off. When low, the 12V supply is on. When high, the 12V supply is off. It can be connected directly to an ATX supply's nPS_ON signal. If not used with an ATX supply, a pull-up resistor to VCC5VSB is required on the baseboard.
A25	NC	NC	NA	Reserved for future use. Do not connect.
A26	NC	NC	NA	Reserved for future use. Do not connect.
A27	GPIO_PD22	I/O	3.3V	Reserved for future use. Connected to GPIO_PD22 of the MPC8360. See Note 1 at the bottom of this table.
A28	NC	NC	NA	Reserved for future use. Do not connect.
A29	TDM1_RXD	I/O	3.3V	TDM 1 receive data. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A30	TDM1_TXD	I/O	3.3V	TDM 1 transmit data. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A31	GND	I	GND	Ground. Connect to digital ground.
A32	GPIO_PD24	I/O	3.3V	Reserved for future use. Connected to GPIO_PD24 of the MPC8360. See Note 1 at the bottom of this table.
A33	GPIO_PD25	I/O	3.3V	Reserved for future use. Connected to GPIO_PD25 of the MPC8360. See Note 1 at the bottom of this table.
A34	GPIO_PD27	I/O	3.3V	Reserved for future use. Connected to GPIO_PD27 of the MPC8360. See Note 1 at the bottom of this table.
A35	NC	NC	NA	Reserved for future use. Do not connect.
A36	uP_SPI_nSEL	I/O	3.3V	SPI interface chip select. When the MPC8360 is in master mode, indicates a multiple-master error. In slave mode, acts as a chip select. Pulled up to 3.3V_IO_VDD through a 10K resistor.
A37	uP_SPI_CLK	I/O	3.3V	SPI interface clock. Pulled up to 3.3V_IO_VDD through a 10K resistor.
A38	PTP_PPS3	O	3.3V	IEEE1588 Real Time Clock pulse per second output 3. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A39	PTP_PPS2	O	3.3V	IEEE1588 Real Time Clock pulse per second output 2. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A40	PTP_PPS1	O	3.3V	IEEE1588 Real Time Clock pulse per second output 1. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A41	GND	I	GND	Ground. Connect to digital ground.
A42	USB2-	I/O	3.3V	USB host port 2 data minus signal. Route as differential pair with USB2+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
A43	USB2+	I/O	3.3V	USB host port 2 data plus signal. Route as differential pair with USB2-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
A44	USB2_nOC	I	3.3V	Active low. USB host ports 2 and 3 over current flag. Indicates an over current condition exists on the USB host port(s). Pulled up to 3.3V_IO_VDD through a 10K resistor.
A45	USB0-	I/O	3.3V	USB host port 0 data minus signal. Route as differential pair with USB0+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
A46	USB0+	I/O	3.3V	USB host port 0 data plus signal. Route as differential pair with USB0-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
A47	NC	NC	NA	No connect. Do not connect.
A48	PTP_EXT_TRIG1	I	3.3V	IEEE1588 Real Time Clock input trigger to capture timestamps 1. See Freescale's *MPC8360E Processor Reference Manual* for more information.

J1A Pin#	Signal Name	I/O	Voltage	Description
A49	PTP_EXT_TRIG2	I	3.3V	IEEE1588 Real Time Clock input trigger to capture timestamps 2. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A50	TDM0_TSYNC	I	3.3V	TDM 0 transmit data sync. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A51	GND	I	GND	Ground. Connect to digital ground.
A52	TOUCH_TOP	I	max 3.3V	Touch panel TOP input signal.
A53	TOUCH_RIGHT	I	max 3.3V	Touch panel RIGHT input signal.
A54	GPIO_PA13	I/O	3.3V	COM Express GPI0. Connected to GPIO_PA13 of the MPC8360.
A55	uP_UART3_CTS	I	3.3V	Clear To Send signal for UART3.
A56	uP_UART3_RTS	O	3.3V	Ready To Send signal for UART4.
A57	GND	I	GND	Ground. Connect to digital ground.
A58	uP_UART4_CTS	I	3.3V	Clear To Send signal for UART4.
A59	uP_UART4_RTS	O	3.3V	Ready To Send signal for UART4.
A60	GND	I	GND	Ground. Connect to digital ground.
A61	TDM0_CLKO	O	3.3V	TDM 0 clock out. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A62	TDM0_nRQ	O	3.3V	TDM 0 IDL request permission to transmit on D channel. See Freescale's *MPC8360E Processor Reference Manual* for more information.
A63	GPIO_PB4	I/O	3.3V	COM Express GPI1. Connected to GPIO_PB4 of the MPC8360.
A64	NC	NC	NA	Reserved for future use. Do not connect.
A65	NC	NC	NA	Reserved for future use. Do not connect.
A66	GND	I	GND	Ground. Connect to digital ground.
A67	GPIO_PA16	I/O	3.3V	COM Express GPI2. Connected to GPIO_PA16 of the MPC8360.
A68	NC	NC	NA	Reserved for future use. Do not connect.
A69	NC	NC	NA	Reserved for future use. Do not connect.
A70	GND	I	GND	Ground. Connect to digital ground.
A71	LVDS_A0+	O	3.3V	Digital video group 0 LVDS out. Route as differential pair with LVDS_A0-. Route pair with 100 ohms differntial impedance.
A72	LVDS_A0-	O	3.3V	Digital video group 0 LVDS out. Route as differential pair with LVDS_A0+. Route pair with 100 ohms differntial impedance.
A73	LVDS_A1+	O	3.3V	Digital video group 1 LVDS out. Route as differential pair with LVDS_A1-. Route pair with 100 ohms differntial impedance.
A74	LVDS_A1-	O	3.3V	Digital video group 1 LVDS out. Route as differential pair with LVDS_A1+. Route pair with 100 ohms differntial impedance.
A75	LVDS_A2+	O	3.3V	Digital video group 2 LVDS out. Route as differential pair with LVDS_A2-. Route pair with 100 ohms differntial impedance.
A76	LVDS_A2-	O	3.3V	Digital video group 2 LVDS out. Route as differential pair with LVDS_A2+. Route pair with 100 ohms differntial impedance.
A77	GPIO_PC22	I/O	3.3V	LVDS VDD Enable. GPIO_PC22 of the MPC8360 is used to enable/disable VDD for the LVDS interface.
A78	LVDS_A3+	O	3.3V	Digital video group 3 LVDS out. Route as differential pair with LVDS_A3-. Route pair with 100 ohms differntial impedance.
A79	LVDS_A3-	O	3.3V	Digital video group 3 LVDS out. Route as differential pair with LVDS_A3+. Route pair with 100 ohms differntial impedance.
A80	GND	I	GND	Ground. Connect to digital ground.
A81	LVDS_A_CK+	O	3.3V	Digital video LVDS clock out. Route as differential pair with LVDS_A_CK-. Route pair with 100 ohms differntial impedance.
A82	LVDS_A_CK-	O	3.3V	Digital video LVDS clock out. Route as differential pair with LVDS_A_CK+. Route pair with 100 ohms differntial impedance.
A83	I2C2_CLK	I/O	3.3V	I2C interface 2 clock signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
A84	I2C2_DATA	I/O	3.3V	I2C interface 2 data signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
A85	GPIO_PA22	I/O	3.3V	COM Express GPI3. Connected to GPIO_PA22 of the MPC8360.

J1A Pin#	Signal Name	I/O	Voltage	Description
A86	GPIO_PC24	I/O	3.3V	Reserved for future use. Connected to GPIO_PC24 of the MPC8360. See Note 1 at the bottom of this table.
A87	GPIO_PC25	I/O	3.3V	Reserved for future use. Connected to GPIO_PC25 of the MPC8360. See Note 1 at the bottom of this table.
A88	NC	NC	NA	Reserved for future use. Do not connect.
A89	NC	NC	NA	Reserved for future use. Do not connect.
A90	GND	I	GND	Ground. Connect to digital ground.
A91	NC	NC	NA	No connect. Do not connect.
A92	NC	NC	NA	No connect. Do not connect.
A93	GPIO_PB6	I/O	3.3V	COM Express GPO0. Connected to GPIO_PB6 of the MPC8360.
A94	NC	NC	NA	No connect. Do not connect.
A95	NC	NC	NA	No connect. Do not connect.
A96	GND	I	GND	Ground. Connect to digital ground.
A97	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A98	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A99	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A100	GND	I	GND	Ground. Connect to digital ground.
A101	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A102	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A103	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A104	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A105	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A106	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A107	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A108	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A109	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
A110	GND	I	GND	Ground. Connect to digital ground.

Note 1: These pins are reserved for future use, but are connected to GPIOs of the MPC8360E processor. They may be used as GPIO, but are not guaranteed to be GPIOs for future MPC83xx COM Express SOM families.

5.1.2 J1A Row B Pin Descriptions

J1A Pin#	Signal Name	I/O	Voltage	Description
B1	GND	I	GND	Ground. Connect to digital ground.
B2	ENET1_LED3	O	3.3V	Active high. Ethenet 1 activity indicator.
B3	uP_UART1_TX	O	3.3V	Data Transmit signal for UART1.
B4	uP_UART1_RX	I	3.3V	Data Receive signal for UART1.
B5	uP_UART1_CTS	I	3.3V	Clear To Send signal for UART1.
B6	uP_UART1_RTS	O	3.3V	Ready To Send signal for UART1.
B7	uP_UART2_TX	O	3.3V	Data Transmit signal for UART2.
B8	uP_UART2_RX	I	3.3V	Data Receive signal for UART2.
B9	uP_UART2_CTS	I	3.3V	Clear To Send signal for UART2.
B10	uP_UART2_RTS	O	3.3V	Ready To Send signal for UART2.

J1A Pin#	Signal Name	I/O	Voltage	Description
B11	GND	I	GND	Ground. Connect to digital ground.
B12	nPWR_BTN	I	3.3V	Active low. Power button signal. When this signal transitions low, power is switched on the SOM (on -> off, off -> on). Pulled up to VCC5VSB through a 10K resistor.
B13	GPIO_PD7	I/O	3.3V	Reserved for future use. Connected to GPIO_PD7 of the MPC8360. See Note 1 at the bottom of this table.
B14	GPIO_PD10	I/O	3.3V	Reserved for future use. Connected to GPIO_PD10 of the MPC8360. See Note 1 at the bottom of this table.
B15	GPIO_PD15	I/O	3.3V	Reserved for future use. Connected to GPIO_PD15 of the MPC8360. See Note 1 at the bottom of this table.
B16	NC	NC	NA	Reserved for future use. Do not connect.
B17	NC	NC	NA	Reserved for future use. Do not connect.
B18	GPIO_PD21	I/O	3.3V	Reserved for future use. Connected to GPIO_PD21 of the MPC8360. See Note 1 at the bottom of this table.
B19	NC	NC	NA	Reserved for future use. Do not connect.
B20	NC	NC	NA	Reserved for future use. Do not connect.
B21	GND	I	GND	Ground. Connect to digital ground.
B22	NC	NC	NA	Reserved for future use. Do not connect.
B23	NC	NC	NA	Reserved for future use. Do not connect.
B24	NC	NC	NA	No connect. Do not connect.
B25	NC	NC	NA	Reserved for future use. Do not connect.
B26	NC	NC	NA	Reserved for future use. Do not connect.
B27	GPIO_PD23	I/O	3.3V	Reserved for future use. Connected to GPIO_PD23 of the MPC8360. See Note 1 at the bottom of this table.
B28	TDM1_RSYNC	I	3.3V	TDM 1 receive data sync. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B29	TDM1_TSYNC	I	3.3V	TDM 1 transmit data sync. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B30	TDM1_CLKO	O	3.3V	TDM 1 clock out. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B31	GND	I	GND	Ground. Connect to digital ground.
B32	TDM1_nRQ	O	3.3V	TDM 1 IDL request permission to transmit on D channel. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B33	I2C1_CLK	I/O	3.3V	I2C interface 1 clock signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
B34	I2C1_DATA	I/O	3.3V	I2C interface 1 data signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
B35	GPIO_PC1	I/O	3.3V	Reserved for future use. Connected to GPIO_PC1 of the MPC8360. See Note 1 at the bottom of this table.
B36	uP_SPI_MOSI	I/O	3.3V	SPI interface master output slave input signal. Pulled up to 3.3V_IO_VDD through a 10K resistor.
B37	uP_SPI_MISO	I/O	3.3V	SPI interface master input slave output signal. Pulled up to 3.3V_IO_VDD through a 10K resistor.
B38	PTP_ALARM1	O	3.3V	IEEE1588 Real Time Clock alarm output trigger 1. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B39	PTP_ALARM2	O	3.3V	IEEE1588 Real Time Clock alarm output trigger 2. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B40	PTP_REF_CLK	O	3.3V	IEEE1588 Real Time Clock divided output clock. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B41	GND	I	GND	Ground. Connect to digital ground.
B42	USB3-	I/O	3.3V	USB host port 3 data minus signal. Route as differential pair with USB3+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
B43	USB3+	I/O	3.3V	USB host port 3 data plus signal. Route as differential pair with USB3-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.

J1A Pin#	Signal Name	I/O	Voltage	Description
B44	USB0_nOC	I	3.3V	Active low. USB host ports 0 and 1 over current flag. Indicates an over current condition exists on the USB host port(s). Pulled up to 3.3V_IO_VDD through a 10K resistor.
B45	USB1-	I/O	3.3V	USB host port 1 data minus signal. Route as differential pair with USB1+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
B46	USB1+	I/O	3.3V	USB host port 1 data plus signal. Route as differential pair with USB1-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differntial impedance.
B47	PTP_CLK	I	3.3V	IEEE1588 Real Time Clock external oscillator input. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B48	TDM0_RSYNC	I	3.3V	TDM 0 receive data sync. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B49	uP_nPORESET	I	3.3V	Active low. External reset input to the SOM. This signal should be used to reset all devices on the SOM including the MPC8360. Pulled up to 3.3V_IO_VDD through a 10K resistor.
B50	uP_nSRESET	O	3.3V	Active low. Reset output from the MPC8360 that drives all onboard reset inputs (except NOR flash). This signal should be used to drive reset inputs on external chips that require similar timing as the onboard devices. Pulled up to 3.3V_IO_VDD through a 1.5K resistor.
B51	GND	I	GND	Ground. Connect to digital ground.
B52	TOUCH_LEFT	I	max 3.3V	Touch panel LEFT input signal.
B53	TOUCH_BOTTOM	I	max 3.3V	Touch panel BOTTOM input signal.
B54	GPIO_PB1	I/O	3.3V	COM Express GPO1. Connected to GPIO_PB1 of the MPC8360.
B55	uP_UART3_TX	O	3.3V	Data Transmit signal for UART3.
B56	uP_UART3_RX	I	3.3V	Data Receive signal for UART3.
B57	GPIO_PB0	I/O	3.3V	COM Express GPO2. Connected to GPIO_PB0 of the MPC8360.
B58	uP_UART4_TX	O	3.3V	Data Transmit signal for UART3.
B59	uP_UART4_RX	I	3.3V	Data Receive signal for UART3.
B60	GND	I	GND	Ground. Connect to digital ground.
B61	TDM0_RXD	I/O	3.3V	TDM 0 receive data. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B62	TDM0_TXD	I/O	3.3V	TDM 0 transmit data. See Freescale's *MPC8360E Processor Reference Manual* for more information.
B63	GPIO_PA14	I/O	3.3V	COM Express GPO3. Connected to GPIO_PA14 of the MPC8360.
B64	NC	NC	NA	Reserved for future use. Do not connect.
B65	NC	NC	NA	Reserved for future use. Do not connect.
B66	NC	NC	NA	Reserved for future use. Do not connect.
B67	nINT_BTN	I	3.3V	This signal can be used as an external interrupt. It is connected to CE_PD17of the MPC8360. Refer to the Freescale *MPC8360E Processor Reference Manual* for more information. Pulled up to 3.3V_IO_VDD through a 10K resistor.
B68	NC	NC	NA	Reserved for future use. Do not connect.
B69	NC	NC	NA	Reserved for future use. Do not connect.
B70	GND	I	GND	Ground. Connect to digital ground.
B71	ENET4_nACT	O	3.3V	Active low. Ethernet 4 activity indicator.
B72	ENET4_RD-	I	3.3V	Ethernet 4 receive signal. Route as diferential pair with ENET4_RD+. Requires external magnetics. See example FlexATX baseboard design for reference components.
B73	ENET4_RD+	I	3.3V	Ethernet 4 receive signal. Route as diferential pair with ENET4_RD-. Requires external magnetics. See example FlexATX baseboard design for reference components.
B74	ENET4_nLINK100	O	3.3V	Active low. Ethernet 4 speed indicator. High when 100Mb/s mode. Low when 10Mb/s mode.
B75	ENET4_nLINK	O	3.3V	Active low. Ethernet 4 link indicator.

J1A Pin#	Signal Name	I/O	Voltage	Description
B76	ENET4_TD-	O	3.3V	Ethernet 4 transmit signal. Route as diferential pair with ENET4_TD+. Requires external magnetics. See example FlexATX baseboard design for reference components.
B77	ENET4_TD+	O	3.3V	Ethernet 4 transmit signal. Route as diferential pair with ENET4_TD-. Requires external magnetics. See example FlexATX baseboard design for reference components.
B78	GPIO_PD1	I/O	3.3V	Reserved for future use. Connected to GPIO_PD1 of the MPC8360. See Note 1 at the bottom of this table.
B79	GPIO_PC16	I/O	3.3V	Active high. LVDS Backlight Enable. This signal is connected to GPIO_PC16 of the MPC8360.
B80	GND	I	GND	Ground. Connect to digital ground.
B81	A/D1	I	max 3.3V	Analog to digital converter input 1.
B82	A/D2	I	max 3.3V	Analog to digital converter input 2.
B83	GPIO_PB7	I/O	3.3V	LVDS Backlight Control. This signal is connected to GPIO_PB7 of the MPC8360.
B84	VCC5VSB	I	5V	External 5V standby power input. This supply should always be on. It powers the power button circuitry.
B85	VCC5VSB	I	5V	External 5V standby power input. This supply should always be on. It powers the power button circuitry.
B86	VCC5VSB	I	5V	External 5V standby power input. This supply should always be on. It powers the power button circuitry.
B87	VCC5VSB	I	5V	External 5V standby power input. This supply should always be on. It powers the power button circuitry.
B88	NC	NC	NA	No connect. Do not connect.
B89	VGA_RED	O	Analog	Analog Red Output. Requires external 75 Ohm pull down.
B90	GND	I	GND	Ground. Connect to digital ground.
B91	VGA_GRN	O	Analog	Analog Green Output. Requires external 75 Ohm pull down.
B92	VGA_BLU	O	Analog	Analog Blue Output. Requires external 75 Ohm pull down.
B93	HSYNC	O	3.3V	Horizontal Sync signal.
B94	VSYNC	O	3.3V	Vertical Sync signal.
B95	I2C2_CLK	I/O	3.3V	I2C interface 2 clock signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
B96	I2C2_DATA	I/O	3.3V	I2C interface 2 data signal. Pulled up to 3.3V_IO_VDD through a 2.2K resistor.
B97	GPIO_PA8	I/O	3.3V	Reserved for future use. Connected to GPIO_PA8 of the MPC8360. See Note 1 at the bottom of this table.
B98	GPIO_PA27	I/O	3.3V	Reserved for future use. Connected to GPIO_PA27 of the MPC8360. See Note 1 at the bottom of this table.
B99	NC	NC	NA	Reserved for future use. Do not connect.
B100	GND	I	GND	Ground. Connect to digital ground.
B101	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B102	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B103	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B104	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B105	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B106	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B107	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B108	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.

J1A Pin#	Signal Name	I/O	Voltage	Description
B109	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
B110	GND	I	GND	Ground. Connect to digital ground.

Note 1: These pins are reserved for future use, but are connected to GPIOs of the MPC8360E processor. They may be used as GPIO, but are not guaranteed to be GPIOs for future MPC83xx COM Express SOM families.

5.2 J1B Connector 220-Pin Descriptions

5.2.1 J1B Row C Pin Descriptions

J1B Pin#	Signal Name	I/O	Voltage	Description
C1	GND	I	GND	Ground. Connect to digital ground.
C2	ENET2_LED3	O	3.3V	Active high. Ethenet 2 activity indicator.
C3	ENET2_TRD3-	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 3. Route as differential pair with ENET2_TRD3+. Requires external magnetics. See example FlexATX baseboard design for reference components.
C4	ENET2_TRD3+	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 3. Route as differential pair with ENET2_TRD3-. Requires external magnetics. See example FlexATX baseboard design for reference components.
C5	ENET2_LED2	O	3.3V	This signal is used with ENET2_LED1 to determine the Ethernet 2 link speed. See Section 5.3.
C6	ENET2_TRD2-	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 2. Route as differential pair with ENET2_TRD2+. Requires external magnetics. See example FlexATX baseboard design for reference components.
C7	ENET2_TRD2+	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 2. Route as differential pair with ENET2_TRD2-. Requires external magnetics. See example FlexATX baseboard design for reference components.
C8	ENET2_LED1	O	3.3V	This signal is used with ENET2_LED2 to determine the Ethernet 2 link speed. See Section 5.3.
C9	ENET2_TRD1-	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 1. Route as differential pair with ENET2_TRD1+. Requires external magnetics. See example FlexATX baseboard design for reference components.
C10	ENET2_TRD1+	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 1. Route as differential pair with ENET2_TRD1-. Requires external magnetics. See example FlexATX baseboard design for reference components.
C11	GND	I	GND	Ground. Connect to digital ground.
C12	ENET2_TRD0-	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 0. Route as differential pair with ENET2_TRD0+. Requires external magnetics. See example FlexATX baseboard design for reference components.
C13	ENET2_TRD0+	I/O	3.3V	Gigabit Ethernet 2 transmit/receive pair 0. Route as differential pair with ENET2_TRD0-. Requires external magnetics. See example FlexATX baseboard design for reference components.
C14	ENET2_CT	O	2.5V	Gigabit Ethernet 2 center tap. This signal is the reference voltage for Etherenet 2 magnetics center tap. See example FlexATX baseboard design for reference components.
C15	NC	NC	NA	No connect. Do not connect.
C16	PCI_nGNT2	I/O	3.3V	Active low. PCI grant 2.
C17	PCI_nREQ2	I/O	3.3V	Active low. PCI request 2. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C18	PCI_nGNT1	I/O	3.3V	Active low. PCI grant 1.
C19	PCI_nREQ1	I/O	3.3V	Active low. PCI request 1. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C20	PCI_nGNT0	I/O	3.3V	Active low. PCI grant 0.
C21	GND	I	GND	Ground. Connect to digital ground.

J1B Pin#	Signal Name	I/O	Voltage	Description
C22	PCI_nREQ0	I/O	3.3V	Active low. PCI request 0. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C23	PCI_nRESET	I	3.3V	Active low. PCI reset.
C24	PCI_AD0	I/O	3.3V	PCI Address/Data 0.
C25	PCI_AD2	I/O	3.3V	PCI Address/Data 2.
C26	PCI_AD4	I/O	3.3V	PCI Address/Data 4.
C27	PCI_AD6	I/O	3.3V	PCI Address/Data 6.
C28	PCI_AD8	I/O	3.3V	PCI Address/Data 8.
C29	PCI_AD10	I/O	3.3V	PCI Address/Data 10.
C30	PCI_AD12	I/O	3.3V	PCI Address/Data 12.
C31	GND	I	GND	Ground. Connect to digital ground.
C32	PCI_AD14	I/O	3.3V	PCI Address/Data 14.
C33	PCI_C/nBE1	I/O	3.3V	Active low. PCI byte enable 1. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C34	PCI_nPERR	I/O	3.3V	Active low. PCI parity error. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C35	NC	NC	NA	No connect. Do not connect.
C36	PCI_nDEVSEL	I/O	3.3V	Active low. PCI device select. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C37	PCI_nIRDY	I/O	3.3V	Active low. PCI initiator ready. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C38	PCI_C/nBE2	I/O	3.3V	Active low. PCI byte enable 2. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C39	PCI_AD17	I/O	3.3V	PCI Address/Data 17.
C40	PCI_AD19	I/O	3.3V	PCI Address/Data 19.
C41	GND	I	GND	Ground. Connect to digital ground.
C42	PCI_AD21	I/O	3.3V	PCI Address/Data 21.
C43	PCI_AD23	I/O	3.3V	PCI Address/Data 23.
C44	PCI_C/nBE3	I/O	3.3V	Active low. PCI byte enable 3. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
C45	PCI_AD25	I/O	3.3V	PCI Address/Data 25.
C46	PCI_AD27	I/O	3.3V	PCI Address/Data 27.
C47	PCI_AD29	I/O	3.3V	PCI Address/Data 29.
C48	PCI_AD31	I/O	3.3V	PCI Address/Data 31.
C49	PCI_nIRQA	I	3.3V	Active low. PCI interrupt A. Pulled up to 3.3V_IO_VDD through a 10K resistor.
C50	PCI_nIRQB	I	3.3V	Active low. PCI interrupt B. Pulled up to 3.3V_IO_VDD through a 10K resistor.
C51	GND	I	GND	Ground. Connect to digital ground.
C52	uP_LAD0	I/O	3.3V	Local bus multiplexed address/data 0.
C53	uP_LAD2	I/O	3.3V	Local bus multiplexed address/data 2.
C54	GND	O	GND	Ground. Connected to digital ground on the SOM. This pin can be used on the baseboard to identify the SOM as a Type III COM Express module.
C55	uP_LAD4	I/O	3.3V	Local bus multiplexed address/data 4.
C56	uP_LAD6	I/O	3.3V	Local bus multiplexed address/data 6.
C57	NC	NC	NA	No connect. Do not connect.
C58	uP_LAD8	I/O	3.3V	Local bus multiplexed address/data 8.
C59	uP_LAD10	I/O	3.3V	Local bus multiplexed address/data 10.
C60	GND	I	GND	Ground. Connect to digital ground.
C61	uP_LAD12	I/O	3.3V	Local bus multiplexed address/data 12.
C62	uP_LAD14	I/O	3.3V	Local bus multiplexed address/data 14.
C63	NC	NC	NA	No connect. Do not connect.
C64	NC	NC	NA	No connect. Do not connect.
C65	uP_LAD16	I/O	3.3V	Local bus multiplexed address/data 16.
C66	uP_LAD18	I/O	3.3V	Local bus multiplexed address/data 18.

J1B Pin#	Signal Name	I/O	Voltage	Description
C67	NC	NC	NA	No connect. Do not connect.
C68	uP_LAD20	I/O	3.3V	Local bus multiplexed address/data 20.
C69	uP_LAD22	I/O	3.3V	Local bus multiplexed address/data 22.
C70	GND	I	GND	Ground. Connect to digital ground.
C71	uP_LAD24	I/O	3.3V	Local bus multiplexed address/data 24.
C72	uP_LAD26	I/O	3.3V	Local bus multiplexed address/data 26.
C73	GPIO_PA28	I/O	3.3V	Reserved for future use. Connected to GPIO_PA28 of the MPC8360. See Note 1 at the bottom of this table.
C74	uP_LAD28	I/O	3.3V	Local bus multiplexed address/data 28.
C75	uP_LAD30	I/O	3.3V	Local bus multiplexed address/data 30.
C76	GND	I	GND	Ground. Connect to digital ground.
C77	NC	NC	NA	No connect. Do not connect.
C78	uP_LA27	I/O	3.3V	Local bus non-multiplexed address 27.
C79	uP_LA29	I/O	3.3V	Local bus non-multiplexed address 29.
C80	GND	I	GND	Ground. Connect to digital ground.
C81	uP_LA31	I/O	3.3V	Local bus non-multiplexed address 31.
C82	NC	NC	NA	No connect. Do not connect.
C83	NC	NC	NA	No connect. Do not connect.
C84	GND	I	GND	Ground. Connect to digital ground.
C85	BOOT_nCS	O	3.3V	This signal can be used to boot from an external device. It is controlled by MODE3. When MODE3 is high, uP_nLCS3 is routed to BOOT_nCS. When MODE3 is low, uP_nLCS0 is routed to BOOT_nCS.
C86	uP_nLCS5	O	3.3V	Local bus chip select 5. Pulled up to 3.3V_IO_VDD through a 10K resistor.
C87	GND	I	GND	Ground. Connect to digital ground.
C88	uP_LDP3	O	3.3V	Local bus data polarity 3.
C89	uP_LDP1	O	3.3V	Local bus data polarity 1.
C90	GND	I	GND	Ground. Connect to digital ground.
C91	uP_nLWE1	O	3.3V	Local bus write enable/byte lane data mask/byte select 1. See Freescale's *MPC8360E Processor Reference Manual* for more information.
C92	uP_nLWE3	O	3.3V	Local bus write enable/byte lane data mask/byte select 3. See Freescale's *MPC8360E Processor Reference Manual* for more information.
C93	GND	I	GND	Ground. Connect to digital ground.
C94	uP_LALE	O	3.3V	Local bus external address latch enable.
C95	uP_LGPL1	O	3.3V	Local bus general purpose line 1/write enable. See Freescale's *MPC8360E Processor Reference Manual* for more information. Pulled down to GND through a 1K resistor.
C96	GND	I	GND	Ground. Connect to digital ground.
C97	NC	NC	NA	No connect. Do not connect.
C98	uP_LGPL3	O	3.3V	Local bus general purpose line 3/column address strobe. See Freescale's *MPC8360E Processor Reference Manual* for more information. Pulled down to GND through a 1K resistor.
C99	uP_LGPL5	O	3.3V	Local bus general purpose line 5. Pulled down to GND through a 1K resistor when PCI_M66EN is high; pulled up to 3.3V_IO_VDD through a 4.7K resistor when PCI_M66EN is low.
C100	GND	I	GND	Ground. Connect to digital ground.
C101	NC	NC	NA	No connect. Do not connect.
C102	uP_LCLK2	O	3.3V	Local bus clock 2.
C103	GND	I	GND	Ground. Connect to digital ground.
C104	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
C105	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.

J1B Pin#	Signal Name	I/O	Voltage	Description
C106	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
C107	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
C108	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
C109	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
C110	GND	I	GND	Ground. Connect to digital ground.

Note 1: These pins are reserved for future use, but are connected to GPIOs of the MPC8360E processor. They may be used as GPIO, but are not guaranteed to be GPIOs for future MPC83xx COM Express SOM families.

5.2.2 J1B Row D Pin Descriptions

J1B Pin#	Signal Name	I/O	Voltage	Description
D1	GND	I	GND	Ground. Connect to digital ground.
D2	ENET3_nACT	O	3.3V	Active low. Ethernet 3 activity indicator.
D3	GPIO_PC10	I/O	3.3V	Reserved for future use. Connected to GPIO_PC10 of the MPC8360. See Note 1 at the bottom of this table.
D4	GPIO_PC26	I/O	3.3V	Reserved for future use. Connected to GPIO_PC26 of the MPC8360. See Note 1 at the bottom of this table.
D5	ENET3_nLINK100	O	3.3V	Active low. Ethernet 3 speed indicator. High when 100Mb/s mode. Low when 10Mb/s mode.
D6	GPIO_PC4	I/O	3.3V	Reserved for future use. Connected to GPIO_PC4 of the MPC8360. See Note 1 at the bottom of this table.
D7	GPIO_PC11	I/O	3.3V	Reserved for future use. Connected to GPIO_PC11 of the MPC8360. See Note 1 at the bottom of this table.
D8	3.3V_IO_VDD (ENET4_CTREF)	O	3.3V	Ethernet 4 center tap. This signal is the reference voltage for Etherenet 4 magnetics center tap. See example FlexATX baseboard design for reference components.
D9	ENET3_RD-	I	3.3V	Ethernet 3 receive signal. Route as diferential pair with ENET3_RD+. Requires external magnetics. See example FlexATX baseboard design for reference components.
D10	ENET3_RD+	I	3.3V	Ethernet 3 receive signal. Route as diferential pair with ENET3_RD-. Requires external magnetics. See example FlexATX baseboard design for reference components.
D11	GND	I	GND	Ground. Connect to digital ground.
D12	ENET3_TD-	O	3.3V	Ethernet 3 transmit signal. Route as diferential pair with ENET3_TD+. Requires external magnetics. See example FlexATX baseboard design for reference components.
D13	ENET3_TD+	O	3.3V	Ethernet 3 transmit signal. Route as diferential pair with ENET3_TD-. Requires external magnetics. See example FlexATX baseboard design for reference components.
D14	ENET3_nLINK	O	3.3V	Active low. Ethernet 3 link indicator.
D15	3.3V_IO_VDD (ENET3_CTREF)	O	3.3V	Ethernet 3 center tap. This signal is the reference voltage for Etherenet 3 magnetics center tap. See example FlexATX baseboard design for reference components.
D16	NC	NC	NA	No connect. Do not connect.
D17	NC	NC	NA	No connect. Do not connect.
D18	NC	NC	NA	No connect. Do not connect.
D19	NC	NC	NA	No connect. Do not connect.
D20	NC	NC	NA	No connect. Do not connect.
D21	GND	I	GND	Ground. Connect to digital ground.
D22	PCI_AD1	I/O	3.3V	PCI Address/Data 1.
D23	PCI_AD3	I/O	3.3V	PCI Address/Data 3.
D24	PCI_AD5	I/O	3.3V	PCI Address/Data 5.

J1B Pin#	Signal Name	I/O	Voltage	Description
D25	PCI_AD7	I/O	3.3V	PCI Address/Data 7.
D26	PCI_C/nBE0	I/O	3.3V	Active low. PCI byte enable 0. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D27	PCI_AD9	I/O	3.3V	PCI Address/Data 9.
D28	PCI_AD11	I/O	3.3V	PCI Address/Data 11.
D29	PCI_AD13	I/O	3.3V	PCI Address/Data 13.
D30	PCI_AD15	I/O	3.3V	PCI Address/Data 15.
D31	GND	I	GND	Ground. Connect to digital ground.
D32	PCI_PAR	I/O	3.3V	PCI bus parity.
D33	PCI_nSERR	I/O	3.3V	Active low. PCI system error. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D34	PCI_nSTOP	I/O	3.3V	Active low. PCI bus stop. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D35	PCI_nTRDY	I/O	3.3V	Active low. PCI target ready. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D36	PCI_nFRAME	I/O	3.3V	Active low. PCI frame. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D37	PCI_AD16	I/O	3.3V	PCI Address/Data 16.
D38	PCI_AD18	I/O	3.3V	PCI Address/Data 18.
D39	PCI_AD20	I/O	3.3V	PCI Address/Data 20.
D40	PCI_AD22	I/O	3.3V	PCI Address/Data 22.
D41	GND	I	GND	Ground. Connect to digital ground.
D42	PCI_AD24	I/O	3.3V	PCI Address/Data 24.
D43	PCI_AD26	I/O	3.3V	PCI Address/Data 26.
D44	PCI_AD28	I/O	3.3V	PCI Address/Data 28.
D45	PCI_AD30	I/O	3.3V	PCI Address/Data 30.
D46	PCI_nIRQC	I	3.3V	Active low. PCI interrupt C. Pulled up to 3.3V_IO_VDD through a 10K resistor.
D47	PCI_nIRQD	I	3.3V	Active low. PCI interrupt D. Pulled up to 3.3V_IO_VDD through a 10K resistor.
D48	NC	NC	NA	No connect. Do not connect.
D49	PCI_M66EN	O	3.3V	PCI M66EN. Pulled up to 3.3V_IO_VDD through a 8.2K resistor.
D50	PCI_CLK	O	3.3V	PCI clock.
D51	GND	I	GND	Ground. Connect to digital ground.
D52	uP_LAD1	I/O	3.3V	Local bus multiplexed address/data 1.
D53	uP_LAD3	I/O	3.3V	Local bus multiplexed address/data 3.
D54	GPIO_PC15	I/O	3.3V	Reserved for future use. Connected to GPIO_PC15 of the MPC8360. See Note 1 at the bottom of this table.
D55	uP_LAD5	I/O	3.3V	Local bus multiplexed address/data 5.
D56	uP_LAD7	I/O	3.3V	Local bus multiplexed address/data 7.
D57	NC	NC	NA	No connect. Do not connect.
D58	uP_LAD9	I/O	3.3V	Local bus multiplexed address/data 9.
D59	uP_LAD11	I/O	3.3V	Local bus multiplexed address/data 11.
D60	GND	I	GND	Ground. Connect to digital ground.
D61	uP_LAD13	I/O	3.3V	Local bus multiplexed address/data 13.
D62	uP_LAD15	I/O	3.3V	Local bus multiplexed address/data 15.
D63	NC	NC	NA	No connect. Do not connect.
D64	NC	NC	NA	No connect. Do not connect.
D65	uP_LAD17	I/O	3.3V	Local bus multiplexed address/data 17.
D66	uP_LAD19	I/O	3.3V	Local bus multiplexed address/data 19.
D67	GND	I	GND	Ground. Connect to digital ground.
D68	uP_LAD21	I/O	3.3V	Local bus multiplexed address/data 21.
D69	uP_LAD23	I/O	3.3V	Local bus multiplexed address/data 23.
D70	GND	I	GND	Ground. Connect to digital ground.
D71	uP_LAD25	I/O	3.3V	Local bus multiplexed address/data 25.
D72	uP_LAD27	I/O	3.3V	Local bus multiplexed address/data 27.

J1B Pin#	Signal Name	I/O	Voltage	Description
D73	NC	NC	NA	Reserved for future use. Do not connect.
D74	uP_LAD29	I/O	3.3V	Local bus multiplexed address/data 29.
D75	uP_LAD31	I/O	3.3V	Local bus multiplexed address/data 31.
D76	GND	I	GND	Ground. Connect to digital ground.
D77	NC	NC	NA	No connect. Do not connect.
D78	uP_LA28	I/O	3.3V	Local bus non-multiplexed address 28.
D79	uP_LA30	I/O	3.3V	Local bus non-multiplexed address 30.
D80	GND	I	GND	Ground. Connect to digital ground.
D81	NC	NC	NA	No connect. Do not connect.
D82	NC	NC	NA	No connect. Do not connect.
D83	NC	NC	NA	No connect. Do not connect.
D84	GND	I	GND	Ground. Connect to digital ground.
D85	uP_nLCS4	O	3.3V	Local bus chip select 4. Pulled up to 3.3V_IO_VDD through a 10K resistor.
D86	uP_LDP2	O	3.3V	Local bus data polarity 2.
D87	GND	I	GND	Ground. Connect to digital ground.
D88	uP_LDP0	O	3.3V	Local bus data polarity 0.
D89	uP_nLWE0	O	3.3V	Local bus write enable/byte lane data mask/byte select 0. See Freescale's *MPC8360E Processor Reference Manual* for more information.
D90	GND	I	GND	Ground. Connect to digital ground.
D91	uP_nLWE2	O	3.3V	Local bus write enable/byte lane data mask/byte select 2. See Freescale's *MPC8360E Processor Reference Manual* for more information.
D92	uP_LBCTL	O	3.3V	Local bus data buffer control.
D93	GND	I	GND	Ground. Connect to digital ground.
D94	uP_LGPL0	O	3.3V	Local bus general purpose line 0/row addressbit/command bit. See Freescale's *MPC8360E Processor Reference Manual* for more information. Pulled down to GND through a 1K resistor.
D95	uP_LGPL2	O	3.3V	Local bus general purpose line 2/output enable/row address strobe. See Freescale's *MPC8360E Processor Reference Manual* for more information.
D96	GND	I	GND	Ground. Connect to digital ground.
D97	NC	NC	NA	Reserved for future use. Do not connect.
D98	uP_LGPL4	O	3.3V	Local bus general purpose line 4/transaction termination/external device wait/local bus parity byte select. See Freescale's *MPC8360E Processor Reference Manual* for more information. Pulled up to 3.3V_IO_VDD through a 1K resistor.
D99	uP_LCKE	O	3.3V	Local bus clock enable.
D100	GND	I	GND	Ground. Connect to digital ground.
D101	uP_LCLK1	O	3.3V	Local bus clock 1.
D102	MODE3	I	3.3V	This signal selects between on-board and off-board boot devices. When high, the NOR flash on the SOM is the boot device. When low, an external boot device can be used with BOOT_nCS. Pulled up to 3.3V_IO_VDD through a 10K resistor.
D103	GND	I	GND	Ground. Connect to digital ground.
D104	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
D105	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
D106	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
D107	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
D108	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.

J1B Pin#	Signal Name	I/O	Voltage	Description
D109	12V	I	12V	External 12V power input. This signal supplies the power switchers on the board.
D110	GND	I	GND	Ground. Connect to digital ground.

Note 1: These pins are reserved for future use, but are connected to GPIOs of the MPC8360E processor. They may be used as GPIO, but are not guaranteed to be GPIOs for future MPC83xx COM Express SOM families.

5.3 Ethernet Signal Link Speeds

The following table lists the LED muxing used to identify the link speed of the Broadcom BCM5481 Ethernet transceivers.

ENET1_LED2/ENET2_LED2	ENET1_LED1/ENET2_LED1	Link/Speed
0	0	Linked @ 1000Base-T
0	1	Linked @ 100Base-TX
1	0	Linked @ 10Base-T
1	1	No link

6 Differences: COM Express Standard vs. COM Express SOM

In order to accommodate the rich feature set of the Freescale PowerQUICC processor, compromises were required with regard to the COM Express Type III standard pinout. Generally, when a signal defined by the COM Express standard was not used by the MPC8360 COM Express SOM, it was left unconnected. However, when a signal defined by the MPC8360E processor did not appear in the COM Express standard, it was necessary to re-define certain signal names to accommodate the MPC8360E processor. Most of these signals can be configured to float, such that no harm will occur on either the SOM or baseboard if the SOM is inserted into a standard Type III baseboard. See Freescale's *MPC8360E Processor Reference Manual* for information on how to program these pins as floating. The following tables show these differences.

6.1 J1A Row A Differences

J1A Pin #	COM Express Standard	Logic COM Express SOM
A29	AC_SYNC	TDM1_RXD
A30	AC_RST#	TDM1_TXD
A36	USB6-	uP_SPI_nSEL
A37	USB6+	uP_SPI_CLK
A38	USB_6_7_OC#	PTP_PPS3
A39	USB4-	PTP_PPS2
A40	USB4+	PTP_PPS1
A48	EXCD0_PERST#	PTP_EXT_TRIG1
A49	EXCD0_CPPE#	PTP_EXT_TRIG2
A50	LPC_SERIRQ	TDM0_TSYNC
A52	PCIE_TX5+	TOUCH_TOP
A53	PCIE_TX5-	TOUCH_RIGHT
A55	PCIE_TX4+	uP_UART3_CTS
A56	PCIE_TX4-	uP_UART3_RTS
A58	PCIE_TX3+	uP_UART4_CTS
A59	PCIE_TX3-	uP_UART4_RTS
A61	PCIE_TX2+	TDM0_CLKO
A62	PCIE_TX2-	TDM0_nRQ

6.2 J1A Row B Differences

J1A Pin #	COM Express Standard	Logic COM Express SOM
B3	LPC_FRAME#	uP_UART1_TX
B4	LPC_AD0	uP_UART1_RX
B5	LPC_AD1	uP_UART1_CTS
B6	LPC_AD2	uP_UART1_RTS
B7	LPC_AD3	uP_UART2_TX
B8	LPC_DRQ0#	uP_UART2_RX
B9	LPC_DRQ1#	uP_UART2_CTS
B10	LPC_CLK	uP_UART2_RTS
B28	AC_SDIN2	TDM1_RSYNC
B29	AC_SDIN1	TDM1_TSYNC
B30	AC_SDIN0	TDM1_CLKO

J1A Pin #	COM Express Standard	Logic COM Express SOM
B32	SPKR	TDM1_nRQ
B36	USB7-	uP_SPI_MOSI
B37	USB7+	uP_SPI_MISO
B38	USB_4_5_OC#	PTP_ALARM1
B39	USB5-	PTP_ALARM2
B40	USB5+	PTP_REF_CLK
B47	EXCD1_PERST#	PTP_CLK
B48	EXCD1_CPPE#	TDM0_RSYNC
B52	PCIE_RX5+	TOUCH_LEFT
B53	PCIE_RX5-	TOUCH_BOTTOM
B55	PCIE_RX4+	uP_UART3_TX
B56	PCIE_RX4-	uP_UART3_RX
B58	PCIE_RX3+	uP_UART4_TX
B59	PCIE_RX3-	uP_UART4_RX
B61	PCIE_RX2+	TDM0_RXD
B62	PCIE_RX2-	TDM0_TXD
B67	WAKE1#	nINT_BTN
B71	LVDS_B0+	ENET4_nACT
B72	LVDS_B0-	ENET4_RD-
B73	LVDS_B1+	ENET4_RD+
B74	LVDS_B1-	ENET4_nLINK100
B75	LVDS_B2+	ENET4_nLINK
B76	LVDS_B2-	ENET4_TD-
B77	LVDS_B3+	ENET4_TD+
B81	LVDS_B_CK+	A/D1
B82	LVDS_B_CK-	A/D2
B83	LVDS_BKLT_CTRL	GPIO_PB7

6.3 J1B Row C Differences

J1B Pin #	COM Express Standard	Logic COM Express SOM
C14	GBE1_LINK#	ENET2_CT
C52	PEG_RX0+	uP_LAD0
C53	PEG_RX0-	uP_LAD2
C55	PEG_RX1+	uP_LAD4
C56	PEG_RX1-	uP_LAD6
C58	PEG_RX2+	uP_LAD8
C59	PEG_RX2-	uP_LAD10
C61	PEG_RX3+	uP_LAD12
C62	PEG_RX3-	uP_LAD14
C65	PEG_RX4+	uP_LAD16
C66	PEG_RX4-	uP_LAD18
C68	PEG_RX5+	uP_LAD20
C69	PEG_RX5-	uP_LAD22
C71	PEG_RX6+	uP_LAD24
C72	PEG_RX6-	uP_LAD26

J1B Pin #	COM Express Standard	Logic COM Express SOM
C74	PEG_RX7+	uP_LAD28
C75	PEG_RX7-	uP_LAD30
C78	PEG_RX8+	uP_LA27
C79	PEG_RX8-	uP_LA29
C81	PEG_RX9+	uP_LA31
C82	PEG_RX9-	NC
C85	PEG_RX10+	BOOT_nCS
C86	PEG_RX10-	uP_nLCS5
C88	PEG_RX11+	uP_LDP3
C89	PEG_RX11-	uP_LDP1
C91	PEG_RX12+	uP_nLWE1
C92	PEG_RX12-	uP_nLWE3
C94	PEG_RX13+	uP_LALE
C95	PEG_RX13-	uP_LGPL1
C98	PEG_RX14+	uP_LGPL3
C99	PEG_RX14-	uP_LGPL5
C101	PEG_RX15+	NC
C102	PEG_RX15-	uP_LCLK2

6.4 J1B Row D Differences

J1B Pin #	COM Express Standard	Logic COM Express SOM
D8	GBE2_LINK1000#	3.3V_IO_VDD (ENET4_CTREF)
D52	PEG_TX0+	uP_LAD1
D53	PEG_TX0-	uP_LAD3
D55	PEG_TX1+	uP_LAD5
D56	PEG_TX1-	uP_LAD7
D58	PEG_TX2+	uP_LAD9
D59	PEG_TX2-	uP_LAD11
D61	PEG_TX3+	uP_LAD13
D62	PEG_TX3-	uP_LAD15
D65	PEG_TX4+	uP_LAD17
D66	PEG_TX4-	uP_LAD19
D68	PEG_TX5+	uP_LAD21
D69	PEG_TX5-	uP_LAD23
D71	PEG_TX6+	uP_LAD25
D72	PEG_TX6-	uP_LAD27
D74	PEG_TX7+	uP_LAD29
D75	PEG_TX7-	uP_LAD31
D78	PEG_TX8+	uP_LA28
D79	PEG_TX8-	uP_LA30
D81	PEG_TX9+	NC
D82	PEG_TX9-	NC
D85	PEG_TX10+	uP_nLCS4
D86	PEG_TX10-	uP_LDP2

J1B Pin #	COM Express Standard	Logic COM Express SOM
D88	PEG_TX11+	uP_LDP0
D89	PEG_TX11-	uP_nLWE0
D91	PEG_TX12+	uP_nLWE2
D92	PEG_TX12-	uP_LBCTL
D94	PEG_TX13+	uP_LGPL0
D95	PEG_TX13-	uP_LGPL2
D98	PEG_TX14+	uP_LGPL4
D99	PEG_TX14-	uP_LCKE
D101	PEG_TX15+	uP_LCLK1
D102	PEG_TX15-	MODE3

7 Mechanical Specifications

7.1 Interface Connectors

The MPC8360 COM Express SOM connects to a PCB baseboard through two 220-pin board-to-board (BTB) socket connectors.

Ref Designator	Manufacturer	COM EXPRESS Connector P/N	Mating Connector P/N
J1A, J1B	Tyco Electronics	3-6318490-6	3-1827253-6

7.2 COM Express SOM Mechanical Drawings

Notes:

1. All measurements are in mm.
2. All hole dimensions have a ± 0.01 mm tolerance.
3. Maximum component height on bottom of board is 3.8 mm.
4. Point of origin is the mounting hole filled in with a solid color.
5. Connector measurements point to connector alignment holes.

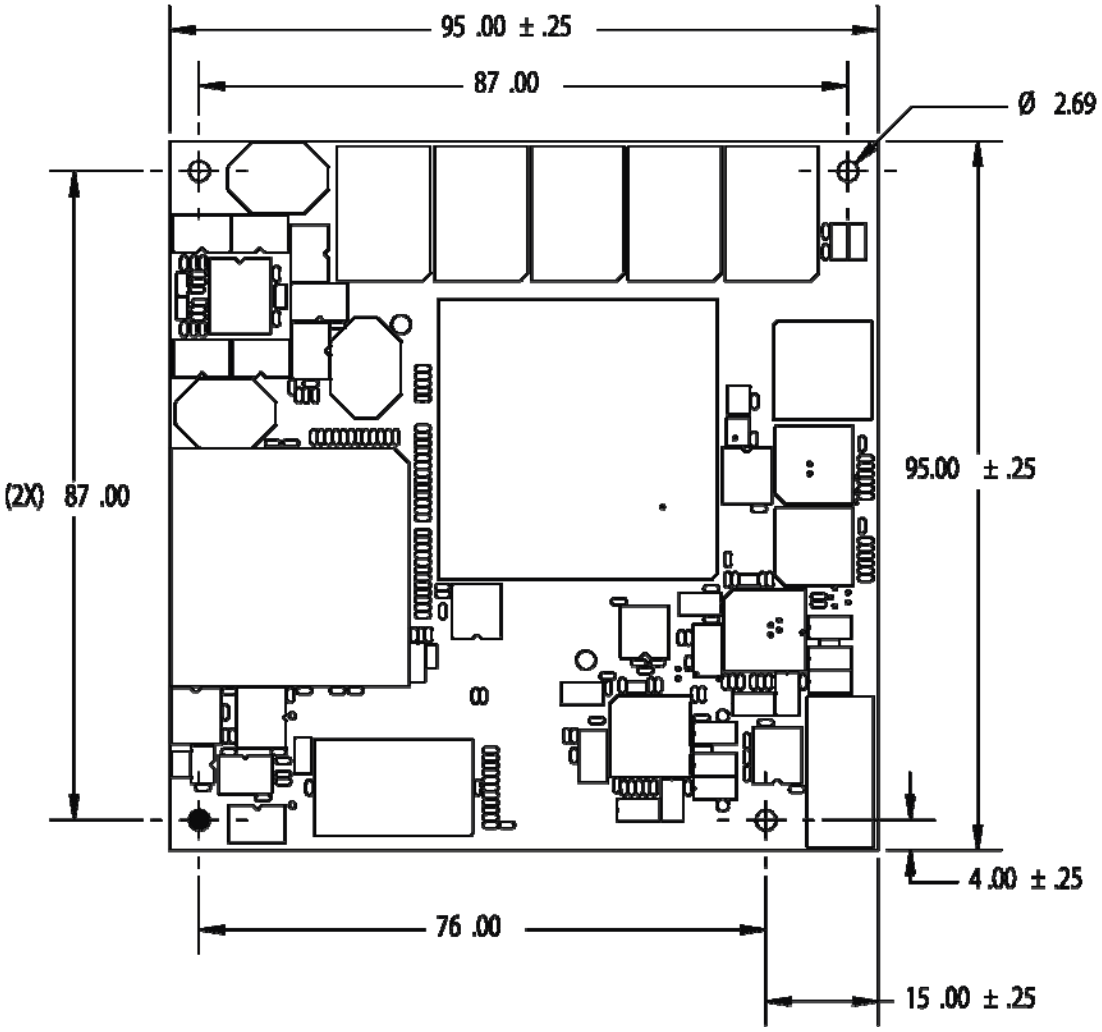

Figure 7.1: MPC8360 COM Express SOM Top View

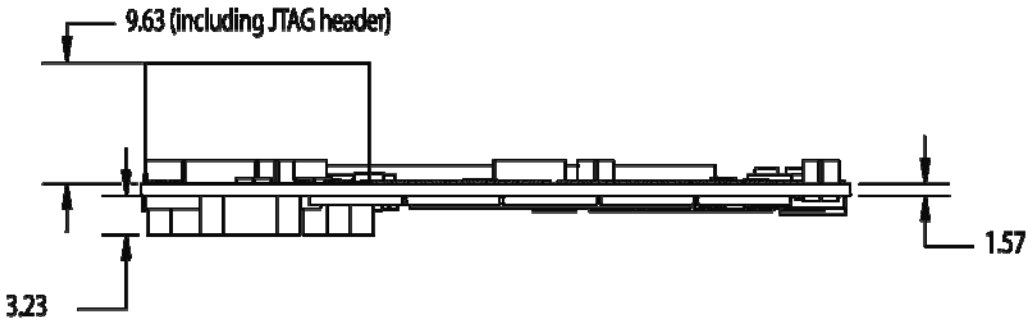

Figure 7.2: MPC8360 COM Express SOM Side View

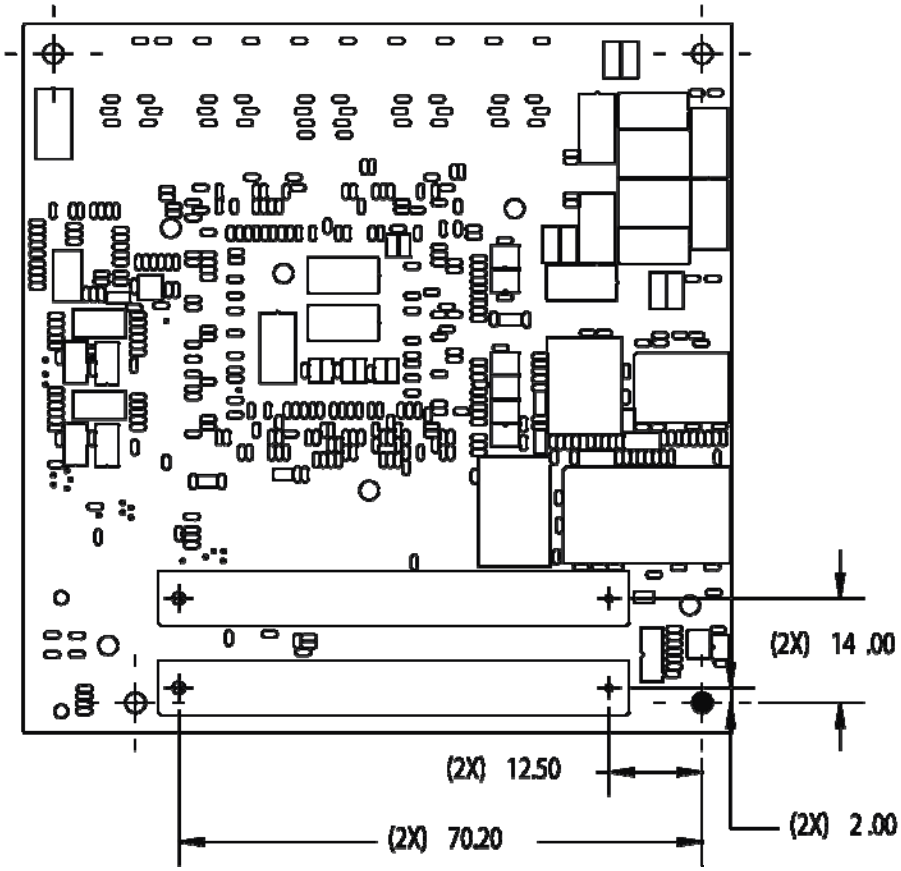

Figure 7.3: MPC8360 COM Express SOM Bottom View

7.3 Recommended Baseboard PCB Layout

Notes:

1. All measurements are in mm.
2. All hole dimensions have a ± 0.01 mm tolerance.
3. Within the layout area of the COM Express SOM, the maximum component height on the application baseboard is 1.0 mm.
4. Point of origin is the mounting hole filled in with a solid color.
5. Connector measurements point to connector alignment holes.

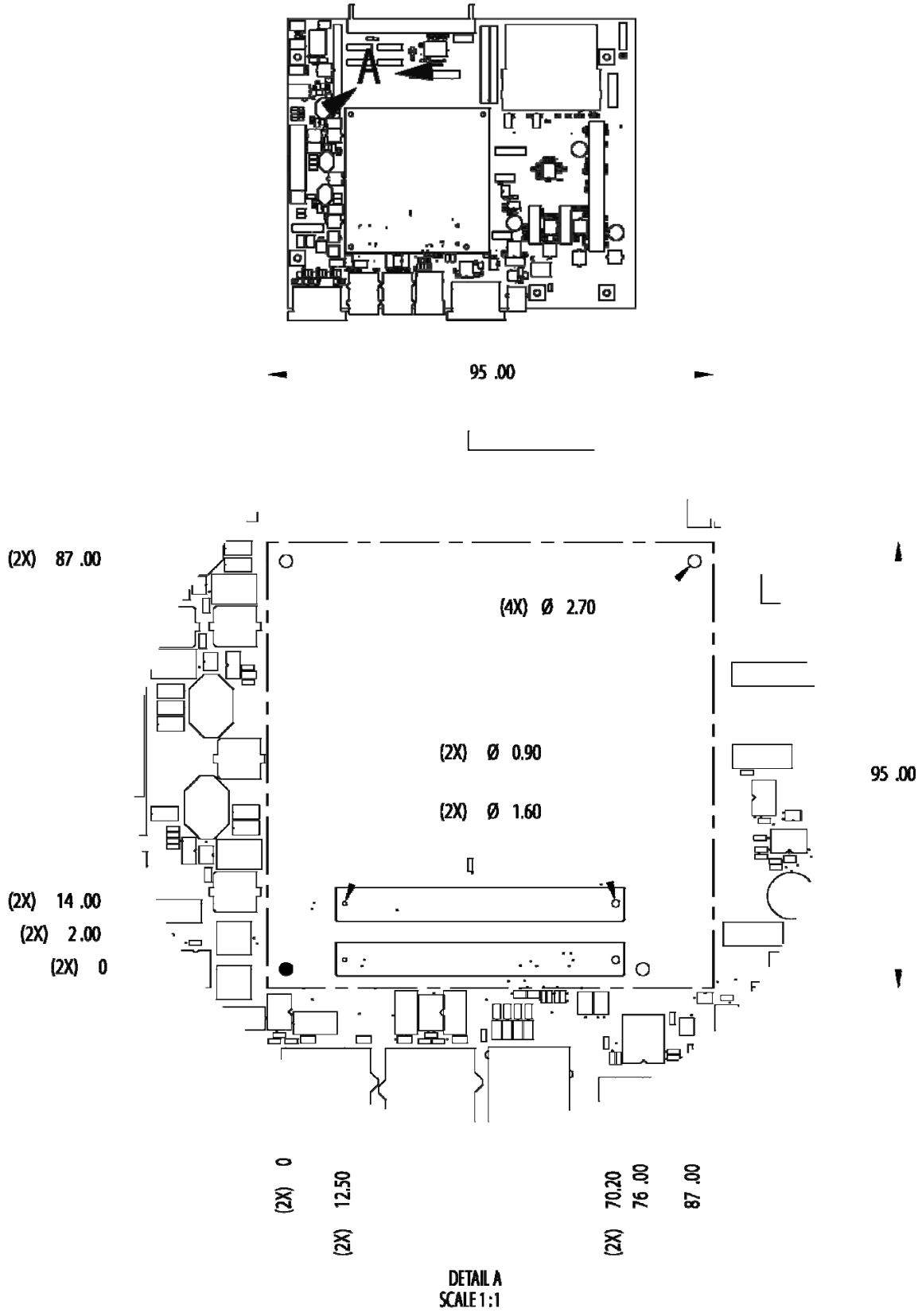

Figure 7.4: Baseboard Footprint for the COM Express SOM

8 Revision History

REV	EDITOR	REVISION DESCRIPTION	Schematic PN & REV	APPROVAL	DATE
1	Nathan Kro	First Release	1006849 Rev 3	JCA	08/05/07
2	Jed Anderson	Format conversion to new template	1006849 Rev 3	JCA	08/10/07
3	Jed Anderson	- Section 2.3.1: updated description of correction Ecc. - Section 2.9: compatible with PCI Local Bus Spec Rev 2.2	1006849 Rev 3	JCA	09/12/07
A	Nathan Kro, Jed Anderson	- Section 2.2: removed table of clock signal names; - Section 5.1.1: changed J1A Pin #A35 to No Connect from GPIO_PE24; - Section 5.1.2: changed J1A Pin #B79 to GPIO_PC16 from GPIO_PC20; changed Pin #B99 to No Connect from GPIO_PB12; - Section 2.2 & throughout: changed oscillator clock speed to 33 MHz; - Throughout: Formatting and grammatical changes	1006849 Rev 4.1	NJK	10/17/07

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.