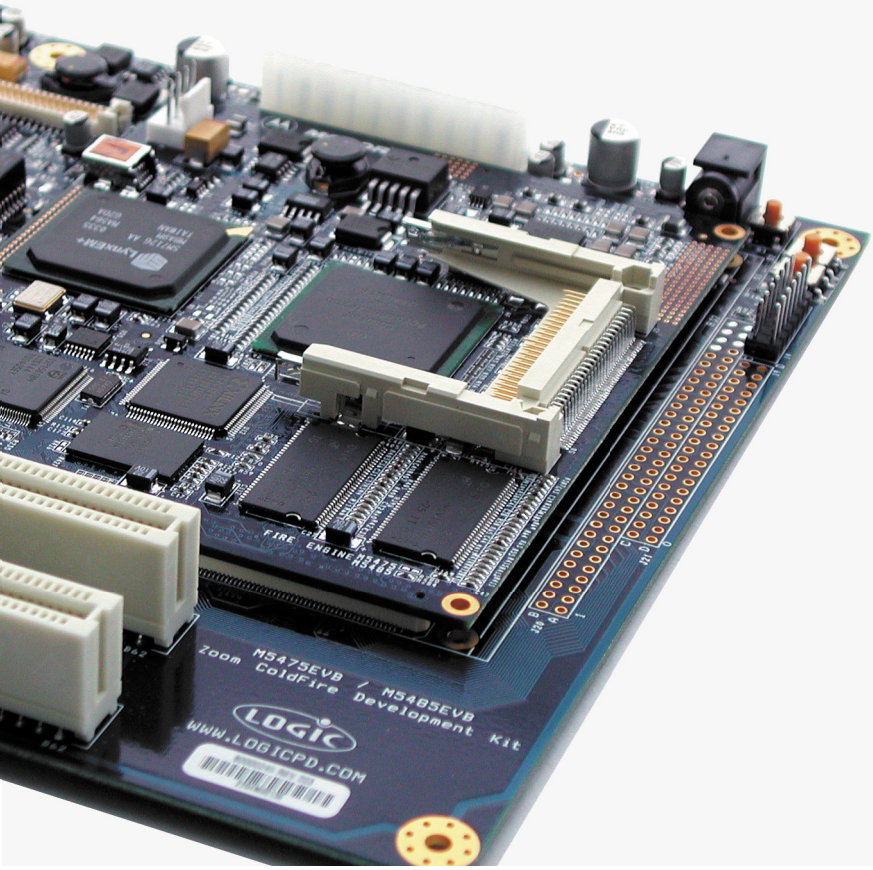
Zoom™

ColdFire Development Kit

Fire Engine Design Guideline



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Fire Engine Design Guideline

Application Note 228

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Logic Product Development

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Abstract

This document serves as a guide for engineers designing custom ETX carrier boards for Fire Engine SOM-ETX modules in custom applications.

REVISION HISTORY

REV	EDITOR	DESCRIPTION	APPROVAL	DATE
1	Ron Ross	Release	KTL	6/04/2004
A	Kurt Larson	Pilot Update	KTL	8/02/2004
B	James Wicks	Replaced MCF5475/85 with 7x/8x	KTL	8/30/2004
C	Nathan Kro	Swapped CAN0 and CAN1 signals	KTL	4/08/2005
D	James Wicks	Improved image quality: Figures 11.1, 12.1	JAW	6/07/2005

Table of Contents

1 Introduction

1.1 Objective

The intention of this design guideline is to serve as a guide for engineers designing custom system baseboards (ETX carrier boards) for the Fire Engine SOM-ETX module. This document provides reference schematics, descriptions, and application notes for implementing the various Fire Engine peripheral functions.

Further documentation: Please reference Logic's *MCF547x/8x Fire Engine Hardware Specification*.

1.2 Target Audience

This guide is intended for hardware engineers designing baseboards, ETX carrier boards, and custom application boards that will utilize the Fire Engine SOM-ETX.

1.3 Assumptions

It is assumed that the reader has an engineering background as well as experience with personal computer buses and peripheral interfaces. A working knowledge of multi-layer printed circuit board design practices is also assumed.

1.4 Scope

The circuits presented in this guide are typical application circuits – it is possible that *they may not be suitable for all applications*. For example, additional components may need to be added to these circuits in order to meet specific ESD or safety isolation requirements. Such regulations, and the techniques required to meet them, vary by industry and are beyond the scope of this document.

1.5 ETX Benefits

Logic Product Development's Fire Engines accelerate your product's time-to-market, and provide the following advantages:

- Product Ready Hardware and Software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – Allows you to focus on other aspects of your design
- Common Card Engine Footprint
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations are available to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

2 ETX Block Diagram

A block diagram of the Fire Engine is displayed below.

In the following sections of this document, each major component will be presented as it applies to its appropriate external connector (X1,X2,X3,X4).

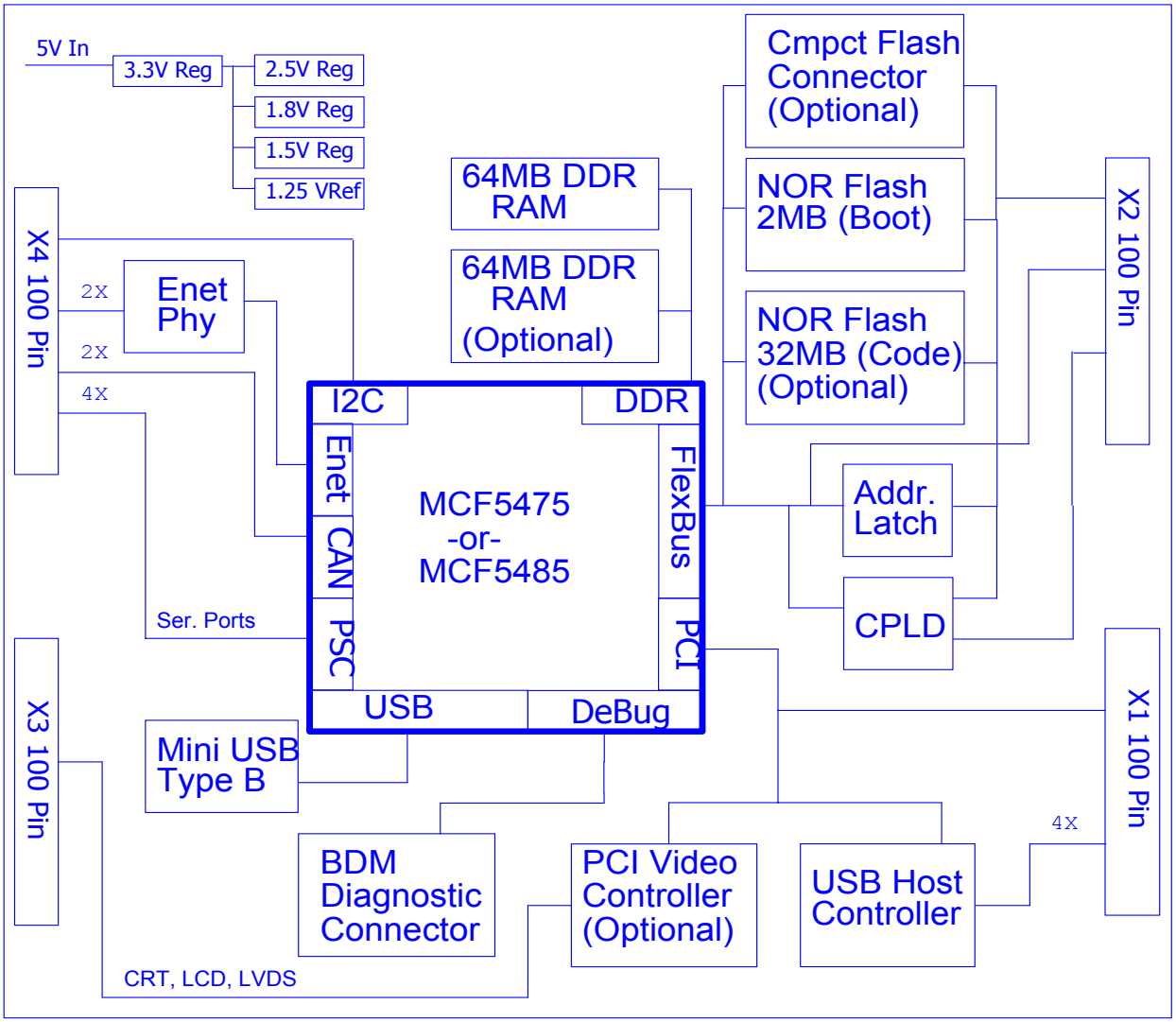

Figure 2.1: ETX Block Diagram

3 Power Supplies

The Fire Engine SOM-ETX module requires only one voltage source for proper operation (5VDC). The ETX module has onboard regulators to create the other required voltages onboard.

5V should be provided to connector J11 or the ETX X1, X2, X3, and X4 connectors. (J1, J2, J3, J4 on ETX module PCB) Depending on the features installed, the Fire Engine can be expected to draw approximately 1.0A – 1.5A from the 5V source under normal operating conditions. Current consumption varies depending on peripheral usage. Reference the MCF547x/8x Fire Engine Hardware Specification for more detailed power estimates.

A 5V DC power source capable of supplying 2.5 Amps is recommended.

ETX connector X1 (J1 on ETX module PCB) pins 12, 16, and 24 are capable of supplying 3.3V to the baseboard module for low current needs. The maximum allowed combined current draw is 500mA. This can be used for powering RS232 level shifters, external LED's, and other low current devices.

NOTE: Do not connect the 3.3V pins to an external power supply. If this occurs, the ETX module will be permanently damaged.

If an ATX power supply is used, the ATX 5VSB signal should be tied to X4 (J4) pin 3 net 5V_SB, which provides the onboard wake up circuitry power. For baseboard designs that do not require ATX or other power control circuitry, the 5V_SB signal can be left unconnected. See section 4 ATX Power Control Circuitry for more information.

4 ATX Power Control Circuitry

If an ATX Power supply is used on the baseboard design, this circuit can be used to control the power on/off functions of the supply. The 5VSB signal provides standby power to the board only powering the power on/off circuitry. The PWRBTN# signal will toggle the PS_ON# output when a rising edge is seen on the PWRBTN# signal. The PWRBTN# signal has an onboard pull up to the 5V_SB supply and a capacitor to ground. A custom baseboard can tie a momentary push button switch to the PWRBTN# signal and to ground to complete the power on/off circuitry. When the button is pushed and released, the capacitor onboard is grounded and recharges via the pull up which creates a rising edge on the PWRBTN# signal. The PS_ON# signal will toggle between low and high states for every rising edge on the PWRBTN# signal. The PS_ON# signal is an output from the ETX module that can be connected to a standard ATX supply's PS_ON# signal to turn on the supply. Reference the Mini ITX design schematics for an example implementation.

5 Reset, Power Monitor

The ETX module has a supervisory circuit that monitors the power supply voltages. The reset will remain active until the onboard 3.3V power supply goes above 2.94V.

Reset can be invoked by driving the BUTTON_MRESET# signal on X4 (J4) pin 98 low. This can be implemented by a simple momentary push button switch tied to ground. The ETX module provides de-bounce circuitry which holds the RESET# line active until approximately 130 ms after the button is released.

Reset can also be invoked by pulling the BDM_RSTI line low. This line comes from the BDM diagnostic connector (J10) and is pulled up when the BDM cable is not attached.

ETX connector X2 (J2) pin 98 is the RESET# output signal which is driven low when the ETX module is in reset. NOTE: This signal is opposite polarity from the ETX standard specification. This signal can be used to reset custom baseboard components.

The ETX module onboard reset circuitry is presented below.

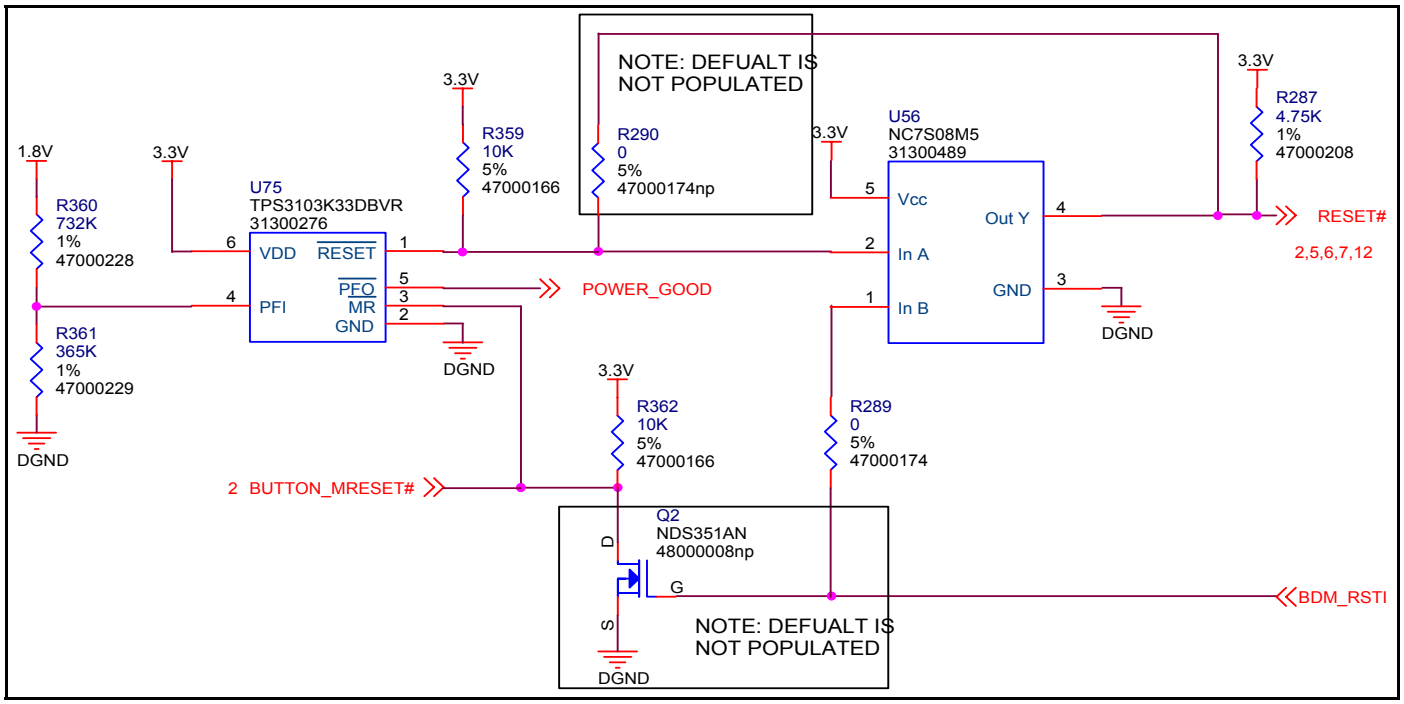

Figure 5.1: Reset Circuit

6 Clocking Options

Please reference the *MCF547x/8x Fire Engine Hardware Specification* for details on ETX module clock states.

Depending on the ETX module population, the external FlexBus and PCI bus operated at 25Mhz, 33Mhz, 50Mhz, or 66Mhz.

- The MCF547x Microcontroller Oscillator frequency of U9 is 66Mhz.
- The MCF548x Microcontroller Oscillator frequency of U9 is 50Mhz.

R285 and R288 determine the onboard bus speed and CPU input clock. The CPU multiplier is set by configuration resistors JP8-JP12. The MCF547x/8x processor has a register available that the clock multiplier can be read from. If R285 is populated, the CPU multiplier register will read back as x4. If R288 is populated, the CPU multiplier register will read back as x2.

The Fire Engine's circuit for the main oscillator is shown below.

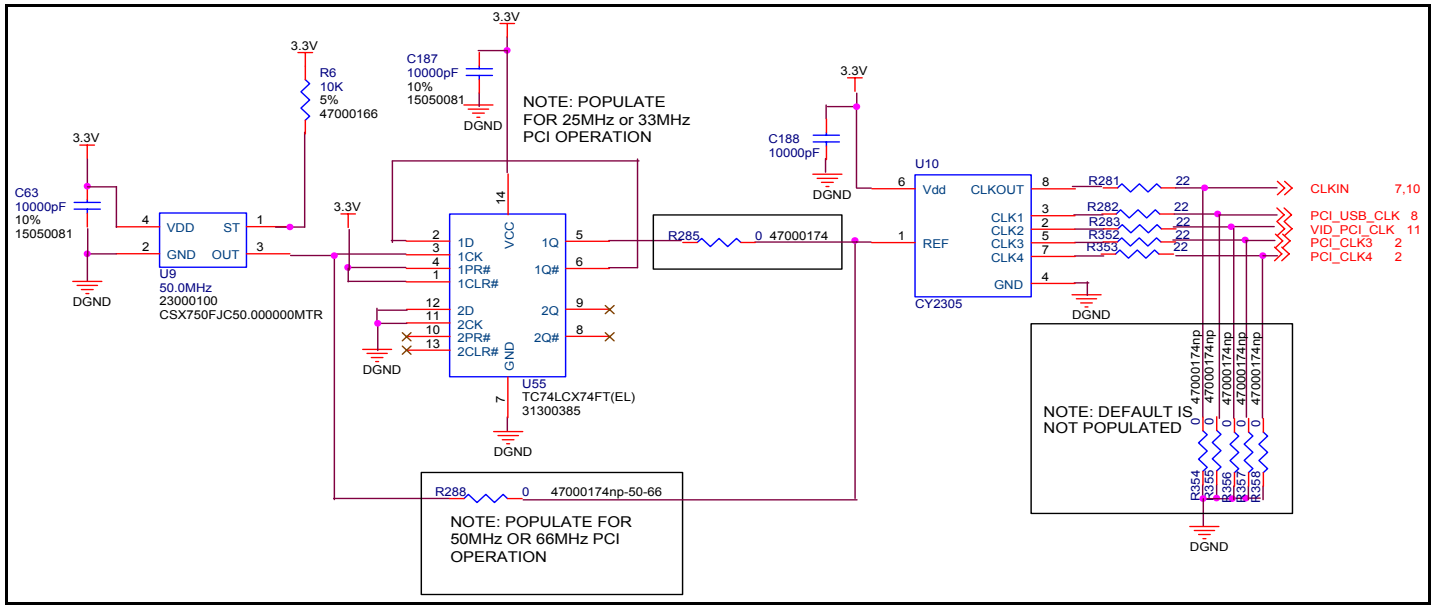

Figure 6.1: Main Oscillator Circuit

7 DDR RAM

The Fire Engine SOM-ETX module has up to 128MB of DDR Ram onboard. None of the DDR RAM signals go off board. For more information on the DDR RAM interface, please reference the MCF547x/8x Fire Engine Hardware Specification.

8 NOR Flash (Boot)

No special interfacing is required to use the onboard flash. Please contact Logic Product Development for pre-loading custom software for production.

9 NOR Flash (Code)

This is an optional block of NOR Flash memory. No special interfacing is required to use the onboard flash. Please contact Logic Product Development for pre-loading custom software for production.

10 Connector X1 (PCI, USB)

This connector has the main purpose of providing all of the necessary signals for operating the PCI Bus connectors and signal distribution for up to four USB ports on the host board. Of the four recommended PCI slots, two are used on the Fire Engine for the USB Host Controller (Slot 1) and the PCI Video controller (Slot 2). Two additional PCI slots can be put down on the baseboard if desired. Of the 100 pins available, the assignments are as follows:

Assignment	Number of Pins	Description
5V	6	
3.3V	3	
Gnd	10	
NC	26	Not Connected
PCI_ AD[31:0]	32	This is the PCI multiplexed Address and Data Bus
PCI_C/BE[3:0]	4	These are the PCI Command/Byte Enables
PCI_PARITY	1	This is the composite Parity bit for the AD[31:0] and the C/BE bits.(Even Parity)
PCI_RESET#	1	Active low, when active, resets all PCI devices
PCI_ClK3,4	2	An individual clock line for each of the two external slots
PCI_REQ2,3	2	Active low, a combination Bus Request and Bus Grant pair for each of the two external slots. When a device wishes to become a Master and use the PCI Bus, it must first assert its Bus Request to the arbiter (The arbiter is contained within the Freescale MCF547x/8x processor.) When it receives a Bus Grant, it may drive the Bus.
PCI_BG2,3	2	Active low, a combination Bus Request and Bus Grant pair for each of the two external slots. When a device wishes to become a Master and use the PCI Bus, it must first assert its Bus Request to the arbiter (The arbiter is contained within the Freescale MCF547x/8x processor.) When it receives a Bus Grant, it may drive the Bus.
M66EN	1	(Detect 66 Mhz device boards)
PCI_INTA#	2	Active low Freescale MCF547x/8x IRQ7#. INTA# is

PCI_INTB#		shared with INTB#. Should be tied to PCI slot INTA# and INTB# respectively.
PCI_INTC# PCI_INTD#	2	Active low Freescale MCF547x/8x IRQ5#. These signals share the IRQ5# interrupt with the ETX module onboard PCI USB Host chip and PCI graphics controller. Should be tied to PCI slot INTC# and INTD# respectively.
PCI_INTC#	1	The Initiator asserts this signal to begin an operation. Active low.
PCI_FRAME#	1	The Target asserts this signal to indicate that its address space has been selected. Active low.
PCI_DEVSEL#	1	Initiator Ready is the initiators response to a read or a write. Active low.
PCI_IRDY#	1	Target Ready is the target's response to a read or a write. Active low.
PCI_TRDY#	1	When Active, a Parity error has occurred. Active low.
PCI_PERR#	1	When Active, a System error has occurred. Active low.
PCI_SERR#	1	The target will assert this signal to request the initiator to stop the operation. Active low.
PCI_STOP#	1	The Initiator will assert this signal to Lock a currently addressed target for an operation such as a read/modify/write. Active low.
PCI_LOCK#	1	Active low.

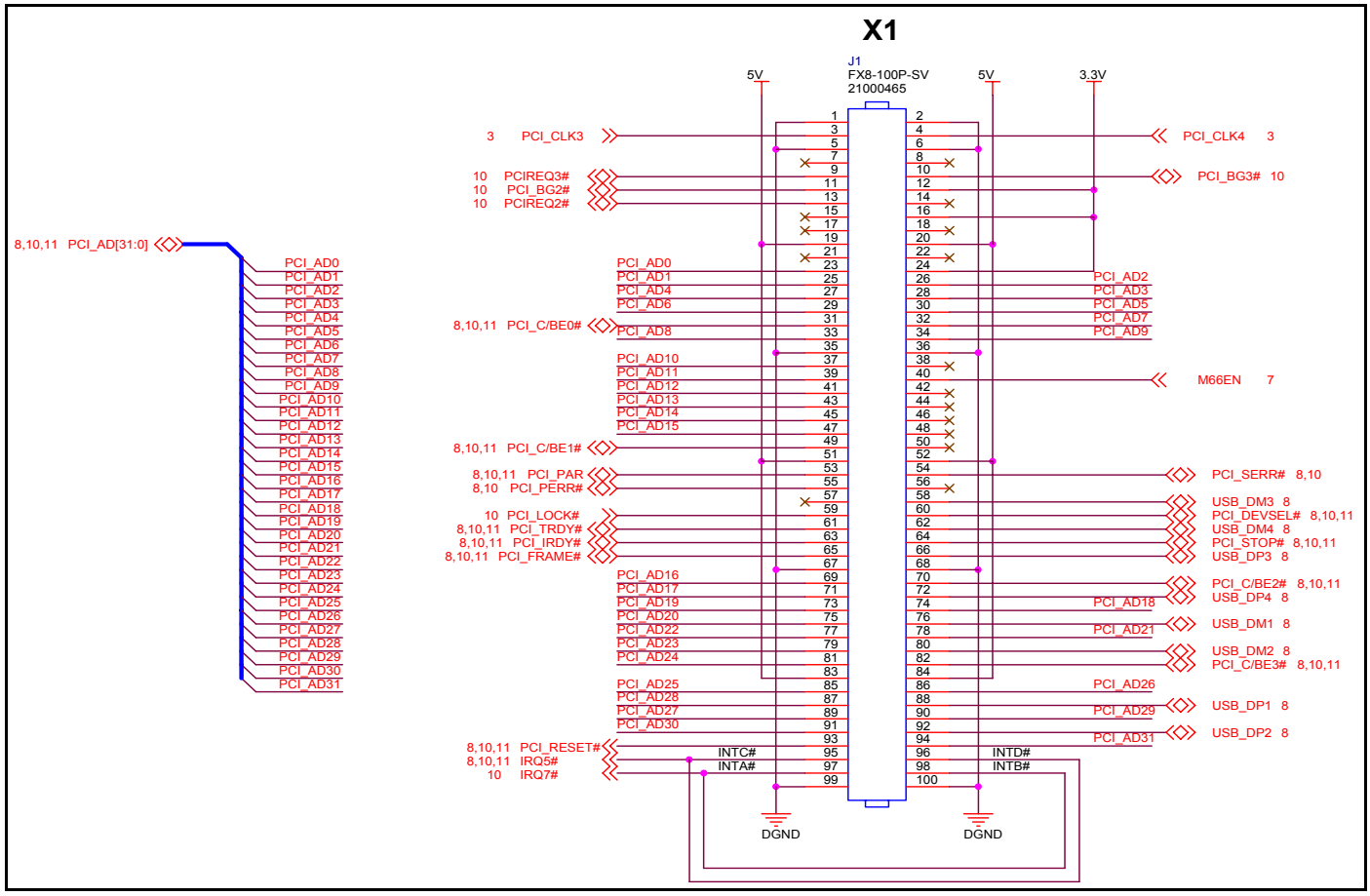

Figure 10.1: X1

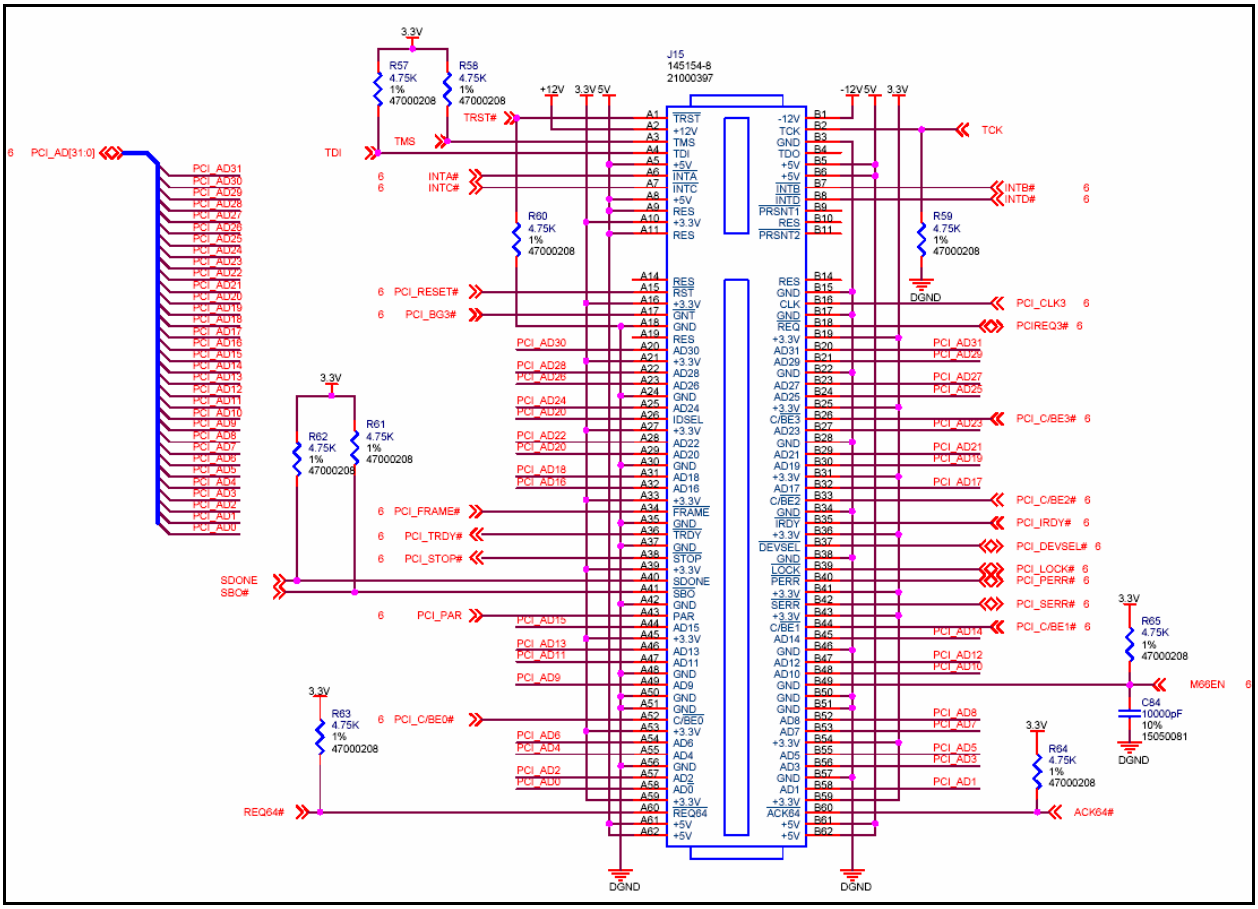

Figure 10.2: Typical PCI Connector

10.1 PCI Slot Differences

Most PCI signals are connected in parallel to all the slots (or devices). The exceptions are the following pins from each slot or device:

10.1.1 IDSEL

Connected to a different AD line for each slot. AD17 is connected to the USB Controller on the Fire Engine ETX module. AD18 is connected to the PCI Video Controller on the Fire Engine ETX module. AD20 represents slot 3 and is available to the baseboard and should be used for the first PCI connector. AD21 represents slot 4 and is available to the baseboard and should be used for the second PCI connector.

10.1.2 PCI_CLK

Connected to a different ETX PCI clock signal for each slot. PCI_CLK3 is available to the baseboard and is intended for use on slot 3. PCI_CLK4 is available to the baseboard and is intended for use on slot 4.

The trace length for all PCI clocks should be matched and controlled. PCI clock routes should be separated as far from other signal traces as possible. PCI clock signals should be routed as controlled-impedance traces, with trace impedance in the 60-70 Ohm range. Only one PCI device or slot should be driven from each ETX PCI clock output.

10.1.3 PCI_REQ#

Connected to a different ETX request signal for each slot, if used. PCIREQ2# is available to the baseboard and is intended for use on slot 3. PCIREQ3# is available to the baseboard and is intended for use on slot 4.

10.1.4 PCI_GNT#

Connected to a different ETX grant signal for each slot, if used. PCI_BG2# is available to the baseboard and is intended for use on slot 3. PCI_BG3# is available to the baseboard and is intended for use on slot 4.

10.1.5 PCI_INT

Most PCI devices use INTA# only and do not require a connection for INTB#, INTC#, or INTD#, however, for maximum flexibility all PCI_INT# signals should be routed to the external slots. The ETX module ties INTA# and INTB# together and supplies the MCF547x/8x with IRQ7#. It also ties INTC# and INTD# together and supplies the MCF547x/8x with IRQ5# which is also shared with the onboard PCI USB Host controller and PCI Graphics controller.

10.1.6 PCI_REQ/ PCI_GNT

These signals are used only by bus-mastering PCI devices. There are two REQ/GNT pairs available to support bus-mastering devices on the baseboard.

10.2 USB Host Ports

Signals USB_DP1 and USB_DM1 are a pair of high speed differential data lines (Plus & Minus). Special care must be taken when routing these signals on the ITX Baseboard. They should be separated as much as possible from other signals, the traces should be parallel, constant spacing between them for the entire distance and the traces should be of equal length.

The same is true for the other 3 USB ports:

- USB_DP2 and USB_DM2
- USB_DP3 and USB_DM3
- USB_DP4 and USB_DM4

The USB Controller used on the ETX Fire Engine is connected to the PCI Interface on the MCF547x/8x as Device ID = 1 (IDSEL= PCI_AD17). It operates as a 32 bit 33 Mhz device. If this controller is onboard, it dedicates the rest of the PCI bus to an operating speed of 33Mhz or 25Mhz in the case of the MCF548x processor. This limits the baseboard PCI_CLK.

The USBx_nEN and USB_nOVRC signals for each port can be found on the X4 (J4) connector. The schematic shown below depicts an example dual host port implementation. For an example quad host port implementation please refer to the Logic Product Development Mini ITX baseboard schematics.

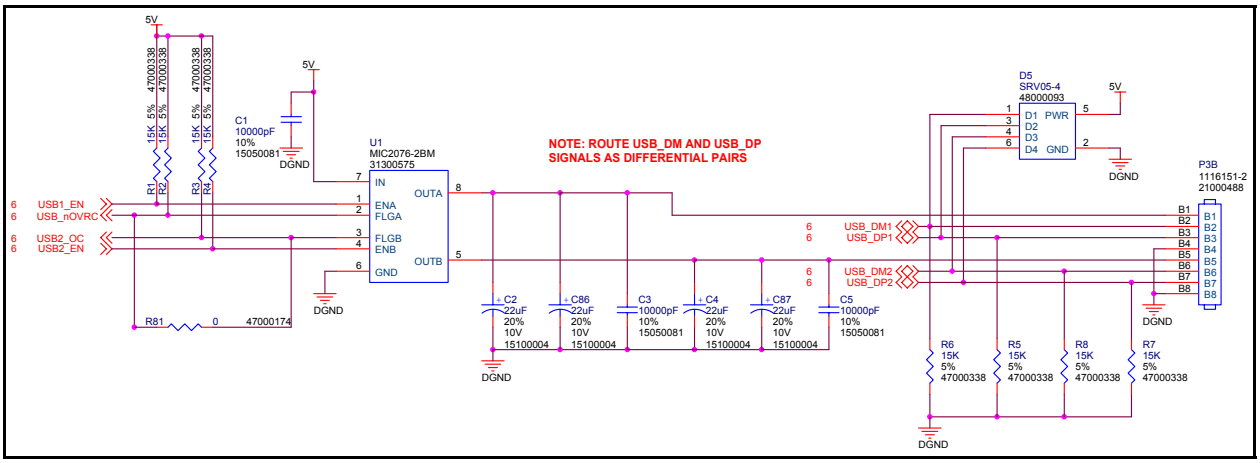

Figure 10.3: USB Host Ports Diagram

10.3 Deviations from the ETX Standard

Please refer to Logic's "MCF547x/8x Fire Engine Hardware Specification" document for deviations from the ETX standard.

11 Connector X2 (FlexBus, ISA)

According to the ETX standard, this connector is generally dedicated to signals associated with ISA bus devices. On the Fire Engine, this connector provides access to the Freescale MCF547x/8x “FlexBus”. Of the 100 pins available, the assignments are:

Assignment	Number of Pins	Description
5V	4	
Gnd	8	
NC	31	Not Connected
LA_FB_AD[19:0]	20	Latched FlexBus Address/data bits
FB_AD[31:16]	16	FlexBus Address/data bits
FB_CS[5:3]	3	FlexBus Chip Select Pins. Active Low.
MCF_OE#	1	FlexBus Output Enable. Active Low.
MCF_RW#	1	FlexBus Read/Write
MCF_TA#	1	FlexBus Transfer Acknowledge. Active Low.
SYSCLK	1	SYSCLK (same as CLKIN to Processor) Only active at reset.
RESET#	1	Master Reset. Active Low.
548X_DREQ0,1#	2	DMA Controller Request. Active Low.
548X_DACK0,1#	2	DMA Controller Acknowledge. Active Low.
ISA_IRQ[3:0]	4	ISA Interrupt requests handled by CPLD. Active Low.
AEN#, BALE, IORD#, IOWR#, CHRDY#	5	Control signals handled by CPLD.

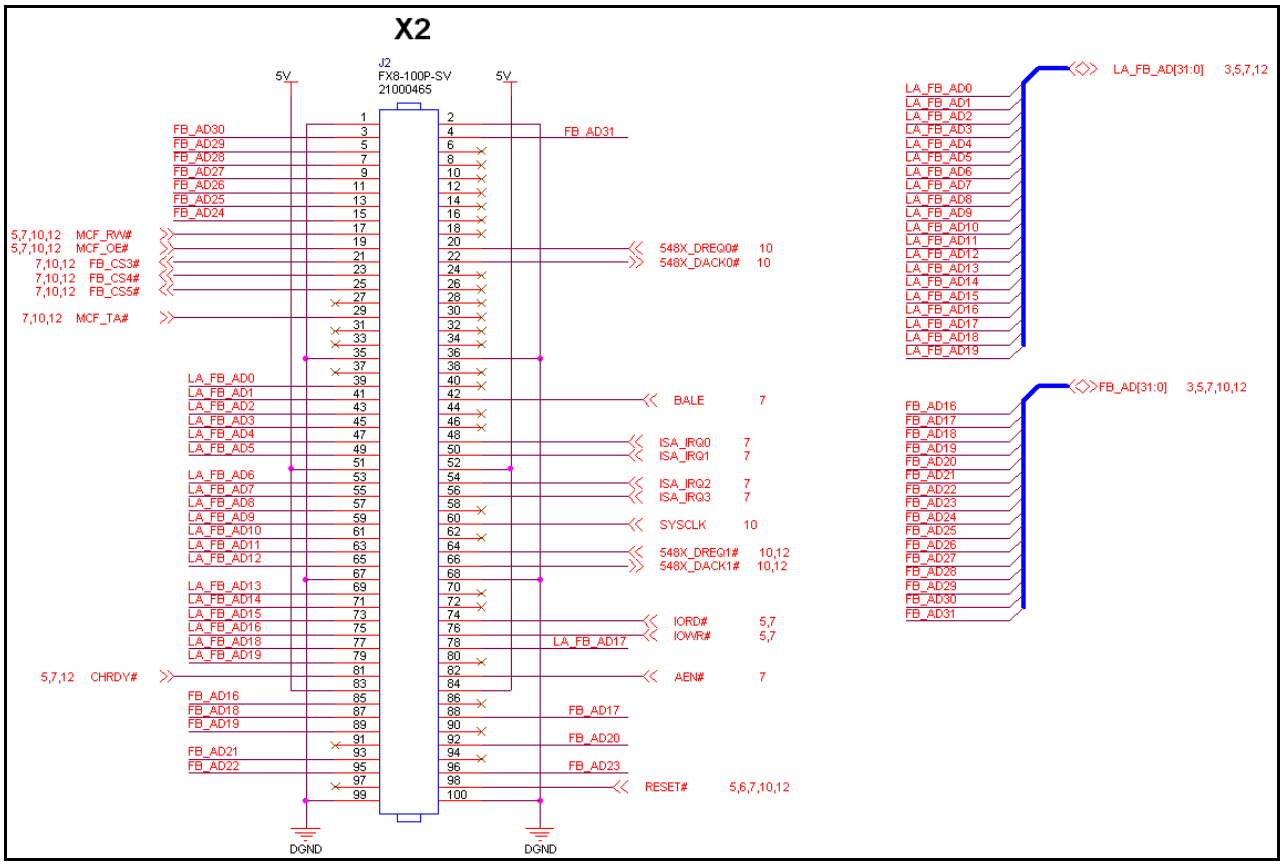

Figure 11.1: X2 Connector

11.1 FlexBus Implementation:

The Freescale FlexBus is an extremely versatile interface providing easy connectivity to a wide range of devices. On Logic Product Development's Mini ITX baseboard, ISA and PC104 implementations have been produced using FlexBus. Developing applications involves a combination of hardware interconnect and setting MCF547x/8x configuration registers. The Fire Engine intends that the interfaces developed will be 8 or 16 bits wide and controlled in conjunction with the on-board CPLD. This CPLD is a standard Xilinx component and field programmable. The CPLD code is available to accommodate several general purpose applications. For more information on the CPLD, please contact Logic Product Development.

The Fire Engine provides both dynamic multiplexed addressing and static latched addressing via on-board latches. Please refer to the MCF547x/8x documentation for more information on the FlexBus.

11.2 Deviations from the ETX Standard:

The X2 connector was intended to provide an ISA interface to the host board. Although not identical, great care has been taken to ensure that the pins assigned as inputs, if used, are still inputs; and pins assigned as outputs, if used, are still outputs. The available FlexBus can emulate the functions of an ISA bus through the use of the on-board CPLD.

Please refer to Logic's "MCF547x/8x Fire Engine Hardware Specification" document for more information.

12 Connector X3 (Video, Serial Ports)

The purpose of this connector is to provide access to the Video Display, Flat Panel display, and the 4 Programmable Serial Controllers available from the Fire Engine. Of the 100 pins available, the assignments are:

Assignment	Number of Pins	Description
5V	5	
Gnd	16	
NC	31	Not Connected
PSC[3:0]_RXD	4	Serial ports Receive Data
PSC[3:0]_TXD	4	Serial ports Transmit Data
PSC[3:0]_CTS#	3	Serial ports Clear to Send. Active low.
PSC[3:0]_RTS#	3	Serial ports Request to Send. NOTE: PSC2_CTS# and PSC2_RTS# are available on connector X4. Active low.
VID_GND	1	Video Ground
PCI_VID_POWERDOWN#	1	Output from CPLD that indicates the Video Oscillator is shut down. Active Low.
DDC_SCL	1	I2C Bus from Video Controller
DDC_SDA	1	I2C Bus from Video Controller
CRT_RED, CRT_BLUE, CRT_GREEN, CRT_HSYNC, CRT_VSYNC	5	CRT Video pins
FP_DATA[5:0], FP_DATA[13:8], FPDATA[21:16]	18	Flat Panel Data Bits
FP_HSYNC, FP_VSYNC, FP_EN, FP_DISPLAY_EN, FP_BIASEN, FP_VDDEN	6	Flat Panel Control Pins
TMDS_IDCK, FP_SHIFTCLK	2	Flat Panel Shift Clock

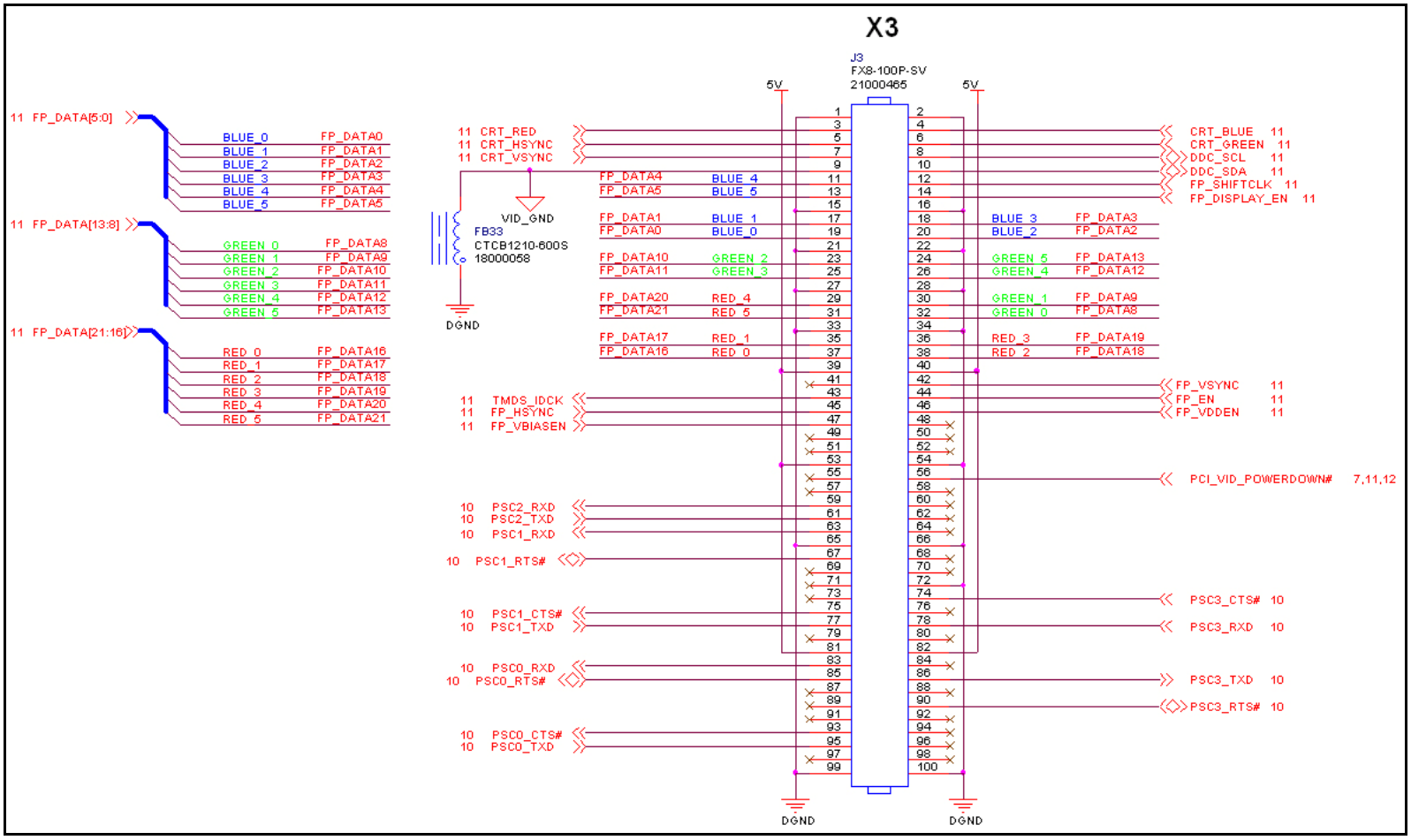

Figure 12.1: X3 Connector

12.1 Video

The Video controller used on the Fire Engine is the LynxEm+ SM712 by Silicon Motion Inc. It provides capability to simultaneously operate LCD/CRT and LCD/TV display combinations. It contains 4MB of video memory.

This PCI device utilizes Device ID =2 (IDSEL = PCI_AD18) from the MCF547x/8x processor PCI bus. It is PCI 2.1 compliant and can operate at either 33Mhz or 66Mhz.

On reset, the video controller uses its MD0 through MD23 memory data bits to configure itself for various operating modes. To accommodate this, the Fire Engine has optional resistors that can be installed to affect this configuration. Since the memory data bits have an internal pull-up in he video controller chip, the omission of a resistor would configure a particular line to a logic “1”. Adding the resistor would configure the line to a logic “0”. The figure below shows the default (Standard) configuration for the Fire Engine video controller.

Logic Loader has display drivers ported for all Zoom Display kits, visit www.logicpd.com for more information on available display kits.

For more information on the graphics controller, please visit www.siliconmotion.com

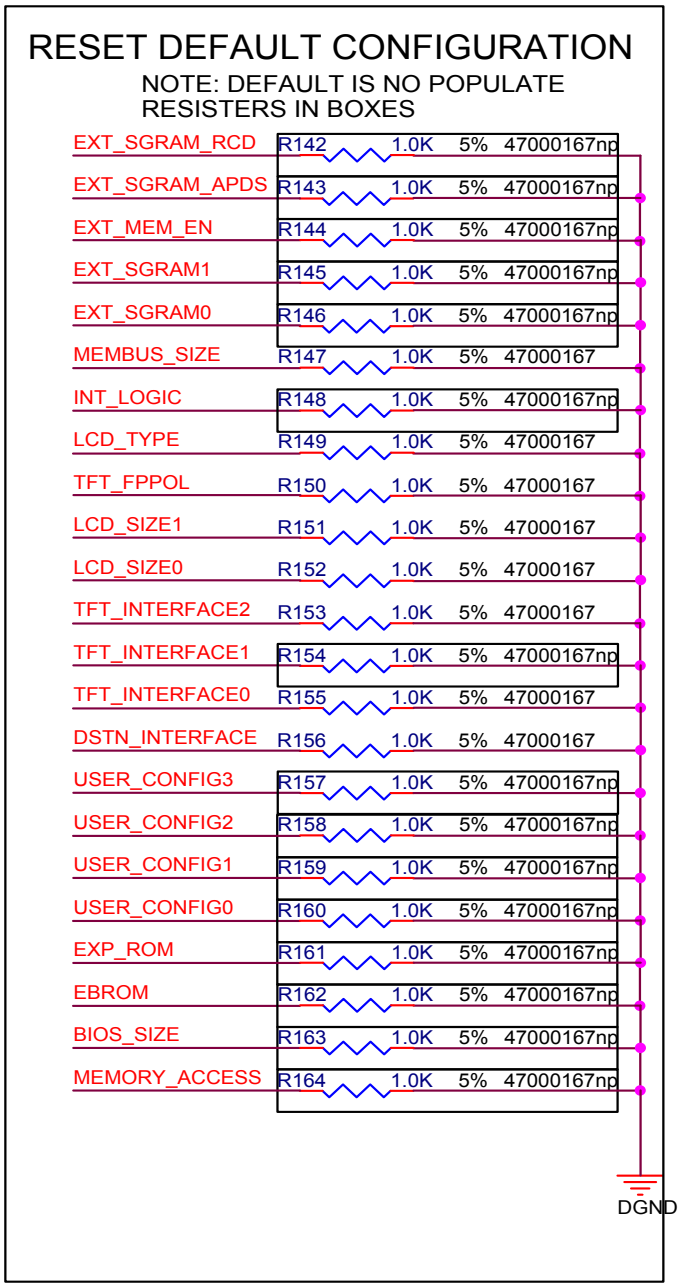

Figure 12.2: Video Diagram

12.2 CRT interface

The LynxEM+ SM712 chip provides both LCD and CRT signals. The ETX X3 (J3) connector provides the CRT signals for use on custom designs. A CRT interface example is shown below.

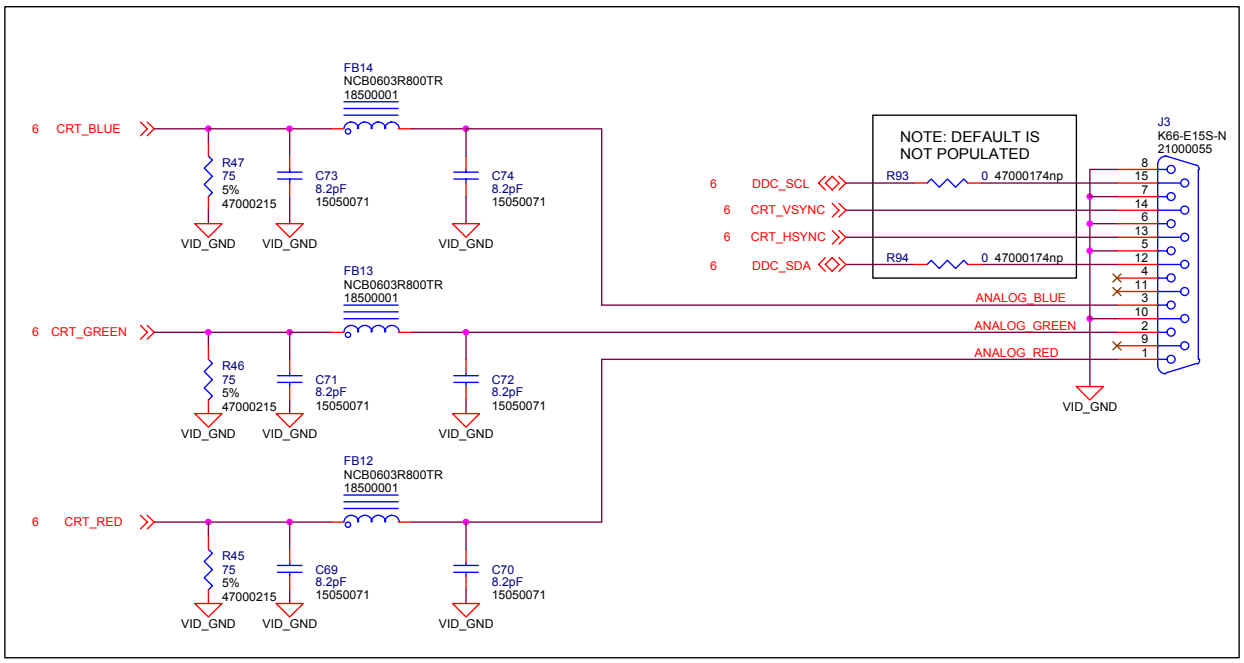

Figure 12.3: CRT Interface Diagram

12.3 Serial Ports

The Fire Engine utilizes Programmable Serial controllers (PSC's) from the MCF547x/8x to provide serial port connectivity to the X3 connector. All 4 ports are provided with signals including Rx, Tx, RTS and CTS.

A baseboard should implement a level shifter for RS232 communication. A sample circuit is shown below. The Mini ITX baseboard can be referenced for more serial port example circuits.

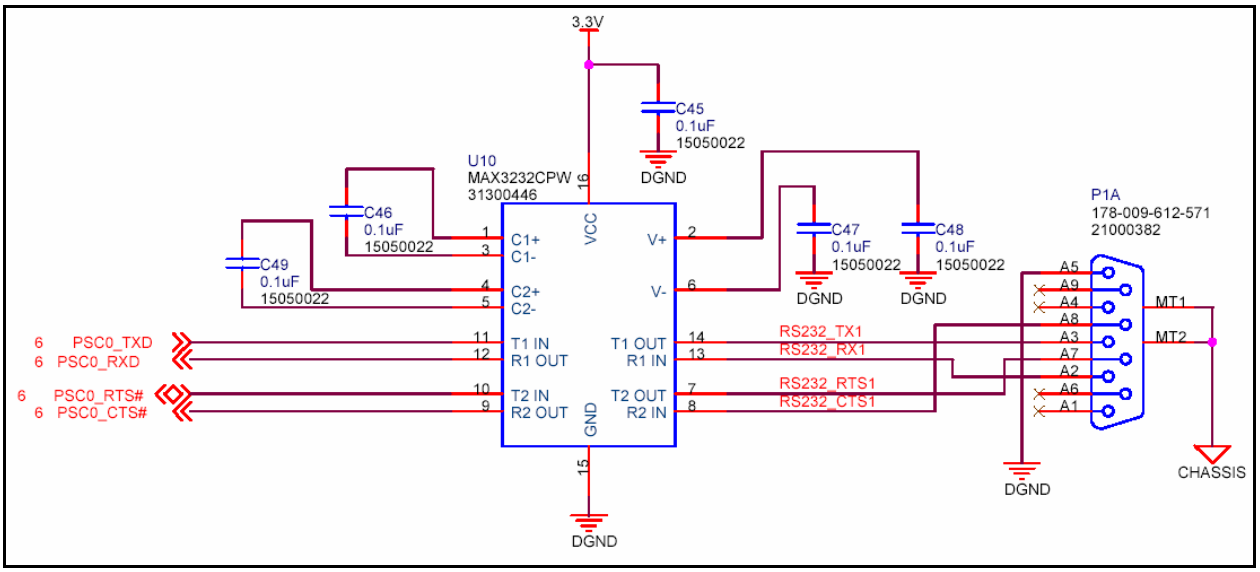

Figure 12.4: Serial Ports Diagram

Note: PSC port 2 has shared function pins for its RTS and CTS signals. They are attached to connector X4 as they must be defined in the processor initialization routine as either control signals for PSC2 or CAN0 data signals. Please refer to the Freescale MCF7x/8x reference Manual for implementation information.

12.4 Deviations from the ETX Standard:

The ETX standard defines two possible pinout schemes for this connector; Panel Link LVDS Interface pinout and Parallel Digital Flat Panel pinout. The Fire Engine pinout for this connector matches more closely with the Parallel Digital Flat Panel pinout. Also, the CRT signals (pins 1 through 10) are in common. The intended purpose of this connector is to additionally provide support for 2 Serial ports, 1 Parallel Port and a Floppy Disk interface. The Fire Engine replaces these signals with the interfaces for 4 Programmable Serial Controllers (PSC'S) These serial ports can provide a wide variety of connectivity. Great care has been taken to ensure that the power and ground connections are the same and pins assigned as inputs, if used, are still inputs and pins assigned as outputs, if used, are still outputs. No damage will result if the Fire Engine ETX board is installed into a standard ETX carrier baseboard.

Please refer to Logic's "MCF547x/8x Fire Engine Hardware Specification" document for more information.

13 Connector X4 (Ethernet, CAN, DSPI, I2C, Power Control, Timers)

The purpose of this connector is to provide access to the DMA Serial Peripheral Interface, I2C bus, CAN ports, Ethernet Ports, USB ports, Programmable Timer Ports, and available from the Fire Engine. Of the 100 pins available, the assignments are:

Assignment	Number of Pins	Description
5V	6	
Gnd	11	
NC	29	Not Connected
PSON#, PWRBTN#	2	ATX Power Supply Support
JTAG_nOE	1	Active low output during CPLD in the field programming.
DSPI_CS0, DSPI_CS2	3	DMA Serial Peripheral Interface Chip Selects
DSPISCK	1	DMA Serial Peripheral Interface Clock
DSPI_DIN	1	DMA Serial Peripheral Interface Data in
DSPI_DOUT	1	DMA Serial Peripheral Interface Data out
I2C_SCL	1	Processor I2C Clock
I2C_SDA	1	Processor I2C Data
CANTX0	1	
CANRX0	1	CAN Port 0
CANTX1	1	
CANRX1	1	CAN Port 1
TX-_0 TX+_0	2	Ethernet Port 0 Xmit Data
RX-_0 RX+_0	2	Ethernet Port 0 Rcv Data
LINKLED1 ACTLED1	2	Ethernet Port 0 LED's
TX-_1 TX+_1	2	Ethernet Port 1 Xmit Data
RX-_1 RX+_1	2	Ethernet Port 1 Rcv Data
LINKLED2 ACTLED2	2	Ethernet Port 1 LED's
LAN_GND	2	Ethernet Ground
USB_nOVRC	2	Over Current sense
USB1_nEN		USB Port 1 Enable. Active Low.
USB2_nEN	1	USB Port 2 Enable. Active Low.
USB3_nEN	1	USB Port 3 Enable. Active Low.
USB4_nEN	1	USB Port 4 Enable. Active Low.
TOUT0 TOUT1 TOUT3 TIN3	1	Programmable timer pins
BUTTON_MRESET#	1	Board reset input. Active Low.
FB_CS0#	1	FlexBus Chip Select (tied to onboard boot flash)
J_FB_AD1	1	

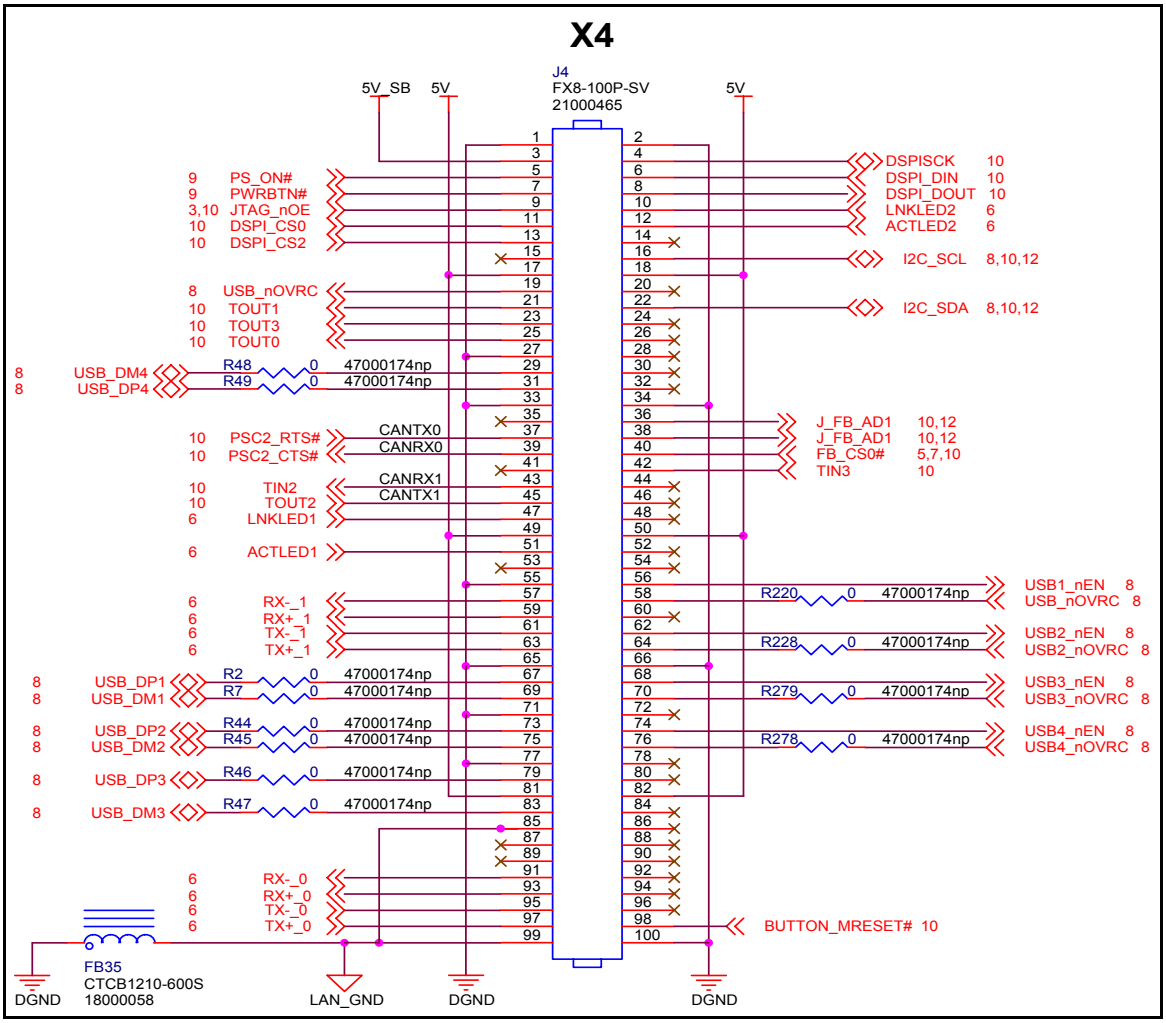

Figure 13.1: X4 Connector

13.1 Ethernet

A Broadcom Ethernet PHY is provided to give connectivity to two 10/100 Ethernet ports. It is intended that the isolation magnetics be contained on the baseboard. The Broadcom recommended devices for the magnetics are available from various vendors:

Bel S558-5999-W2
Pulse Engineering H1102
Halo TG110-S050N2

The recommended connection is shown in the figure below:

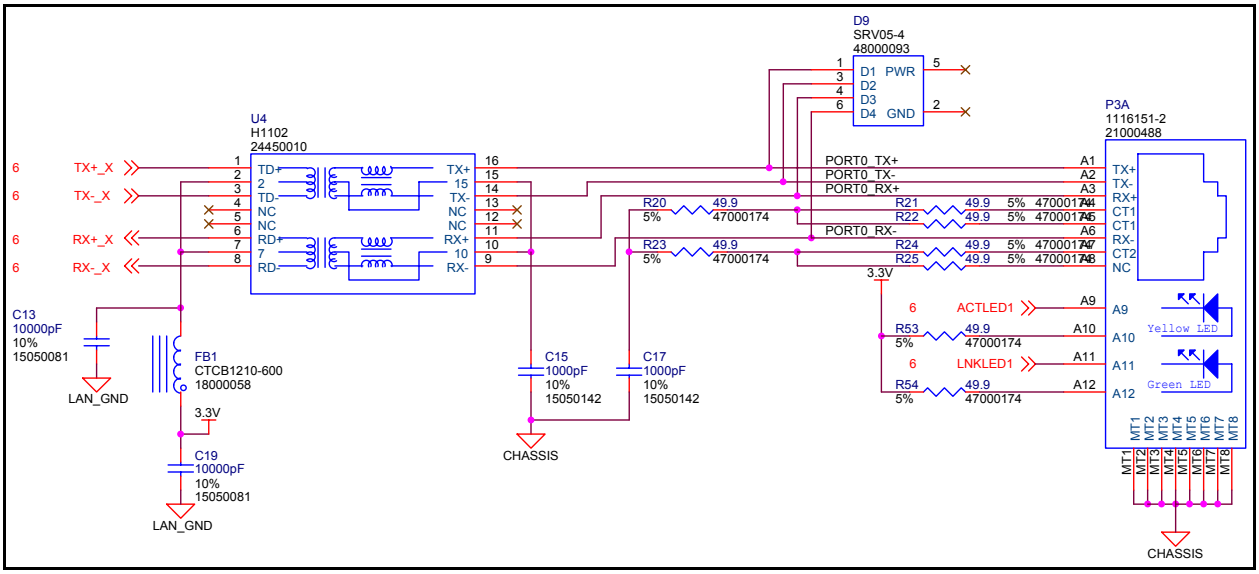

Figure 13.2: Connector X Ethernet

The last X in the TX+_X, TX-_X, RX+_X, RX-_X signal names can be replaced with the desired Ethernet port number (0 or 1).

NOTE: Implementing this interface on baseboards requires the data signals on both sides of the transformer to be routed as differential pairs, match the impedance characteristics of the board and follow all other differential pair layout considerations.

13.2 CAN

Only the MCF548x supports the Controller Area Network (CAN) ports, the MCF547x does not.

The TX and RX pins for CAN port 0 are shared with PSC2 Serial Port pins RTS# and CTS# respectively. X4 (J4) pin 37 and X4 (J4) pin 39.

The TX and RX pins for CAN port 1 are shared with Programmable Timer pins TOUT2 and TIN2 respectively. X4 (J4) 45 and X4 (J4) 43.

There are many other possible pin assignments for the CAN ports. (Please see the Freescale MCF548x Hardware specification for details). The above pin assignments were chosen to match the Logic Product Development Mini-ITX baseboard.

The use of an external CAN transceiver to interface to the CAN bus is generally required. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against a defective CAN bus or defective stations. The transceiver used on the Logic Product Development Mini-ITX board is the SN65HVD232 by Texas Instruments.

13.3 DSPI

The DMA serial peripheral interface (DSPI) block provides a synchronous serial bus for communication between the Fire Engine SOM-ETX module and an external peripheral devices. Refer to the Freescale MCF547x/8x Reference manual for details.

The Fire Engine makes 5 DSPI signals available to connector X4 (J4): Clock, Data in, Data out, Chip Select 0, Chip Select 2.

13.4 I2C

I2C is a two-wire, bi-directional serial bus, which provides a simple, efficient method of data exchange between devices. This two-wire bus minimizes the interconnection between the devices.

The interface is designed to operate up to 100kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pf.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The I2C clock line is available at X4 (J4) pin 16.
The I2C data line is available at X4 (J4) pin 22.

Logic Product Development uses this bus on it's Mini-ITX baseboard to communicate with Real Time Clock and makes it available to external devices via a connector.

13.5 Power Control

In order to comply with the ETX standard, The Fire Engine provides circuitry to control an ATX power supply. It involves the implementation of 3 signals: the push button input, the power-on control output and the 5V_SB voltage line which is used to power this circuitry even though the power may be off.

13.6 Timers

4 general-purpose timers are available on the MCF547x/8x. These 32-bit timers can capture timer values, trigger external events or internal interrupts, or count external events.

- Timer input 0 (not connected)
- Timer input 1 (not connected)
- Timer input 2 (X4 (J4) pin 43)
- Timer input 3 (X4 (J4) pin 42)

These timer inputs can be programmed as clocks that cause events in the counter and prescalers. They can also capture on the rising edge, falling edge or both edges.

- Timer output 0 (X4 (J4) pin 25)
- Timer output 1 (X4 (J4) pin 21)
- Timer output 2 (X4 (J4) pin 45)
- Timer output 3 (X4 (J4) pin 23)

These timer outputs can be programmed to pulse or toggle on various timer events.

For more information on setting up these timers, please see the Freescale MCF547x/8x Reference Manual.

Note: Timer input 2 and Timer output 2 are programmable pins with multiple functions on the MCF547x/8x microcontroller. When used with the Logic Product Development Mini-ITX baseboard, they share their function with CAN-TX1 and CAN-RX1. When it is desired to use both Timer #2 and CAN port 1, special considerations are necessary with regard to pin assignments.

13.7 Deviations from the ETX Standard:

The intent of the ETX standard X4 connector is to provide for an Ethernet Controller, 2 IDE ports and various other signals associated with a standard PC. The Fire Engine SOM-ETX supports the Ethernet Port, Adds a second Ethernet port, 2 CAN ports, up to 4 programmable Timer ports, and a DMA Serial Peripheral interface (DSPI). Great care has been taken to ensure that the power and ground connections are the same and pins assigned as inputs, if used, are still inputs and pins assigned as outputs, if used, are still outputs. No damage will result if the Fire Engine ETX board is installed into a standard ETX baseboard.

Please refer to Logic's "MCF547x/8x Fire Engine Hardware Specification" document for more information.

14 USB Device Connector

The USB device (client) module implementation on the MCF547x/8x processor provides all the logic necessary to process the USB protocol as defined by version 2.0 specification for peripheral devices.

- High-speed operation up to 480 Mbps, full-speed operation at 12 Mbps, and low-speed operation at 1.5 Mbps
- Physical interface on chip
- Bulk, interrupt, and isochronous transport modes
- Six programmable in/out endpoints and one control endpoint
- 4 Kbytes of shared endpoint FIFO RAM and 1 Kbyte of endpoint descriptor RAM

The type B Mini USB Connector pins are shown below:

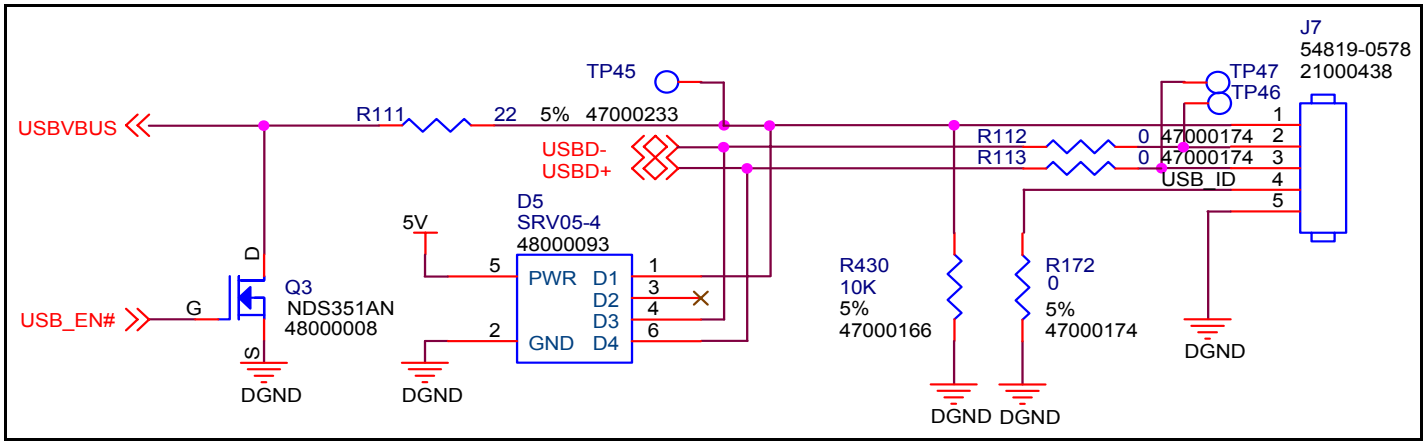

Figure 14.1: USB Connector

15 CompactFlash Connector

This connector provides connectivity to Compact Flash memory devices. Please contact Logic Product Development for details. Hot-swapping is not available.

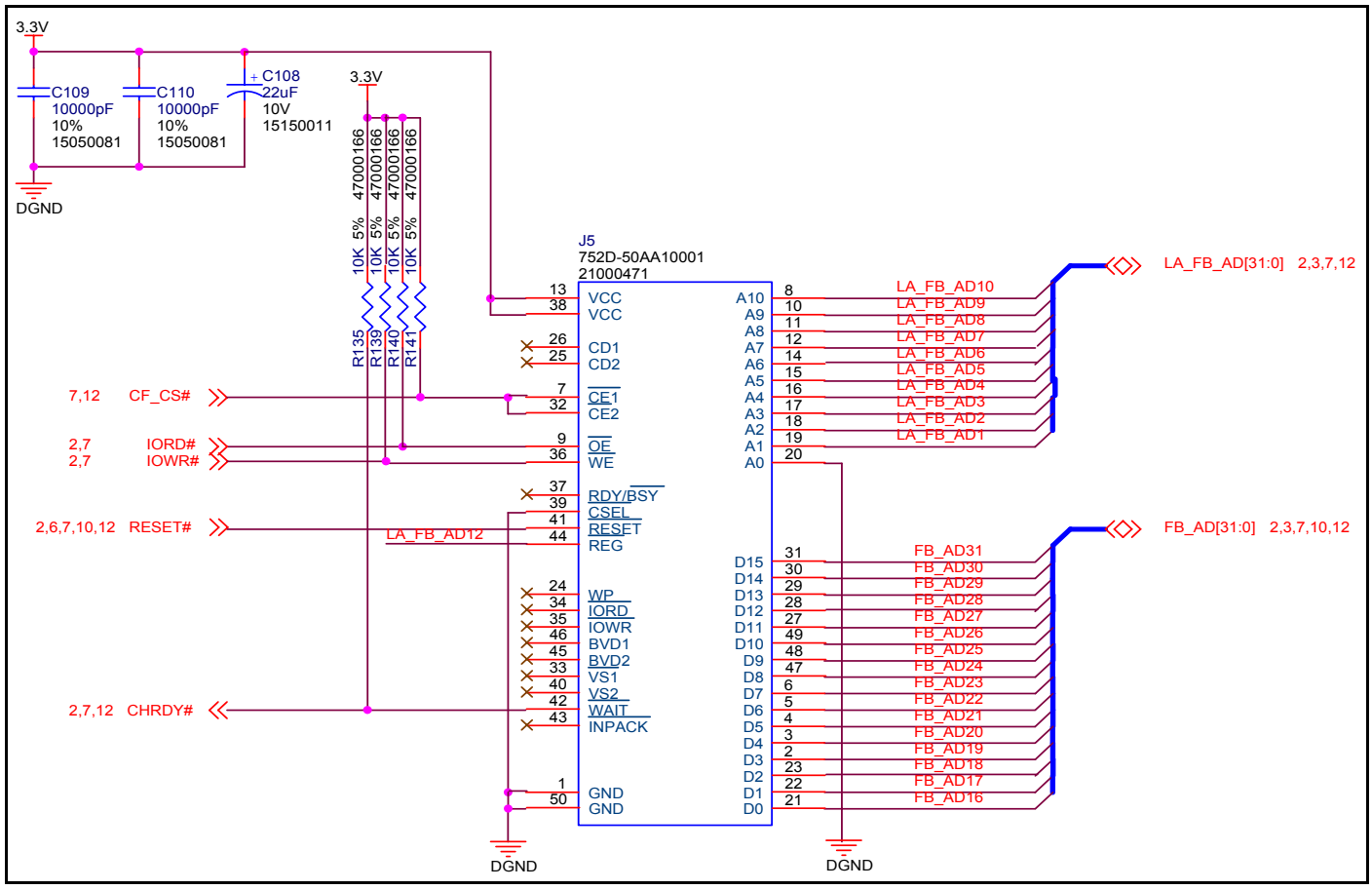

Figure 15.1: CompactFlash Connector

16 BDM Connector

The Fire Engine SOM-ETX module has a BDM connector for board debug. No special interfacing is required to use the BDM interface.

17 Support Services

If you have questions or need additional help with designing custom ETX carrier boards for Fire Engine SOM-ETX modules in custom applications, please contact Logic Product Development for more information.

Please keep in mind that we have additional support services and support packages available for purchase. In addition Logic provides a free Technical Discussion Group and FAQ's for our products.

Visit our downloads section on the Logic website at http://www.logicpd.com/auth/login.php in order to access our most recent documentation.