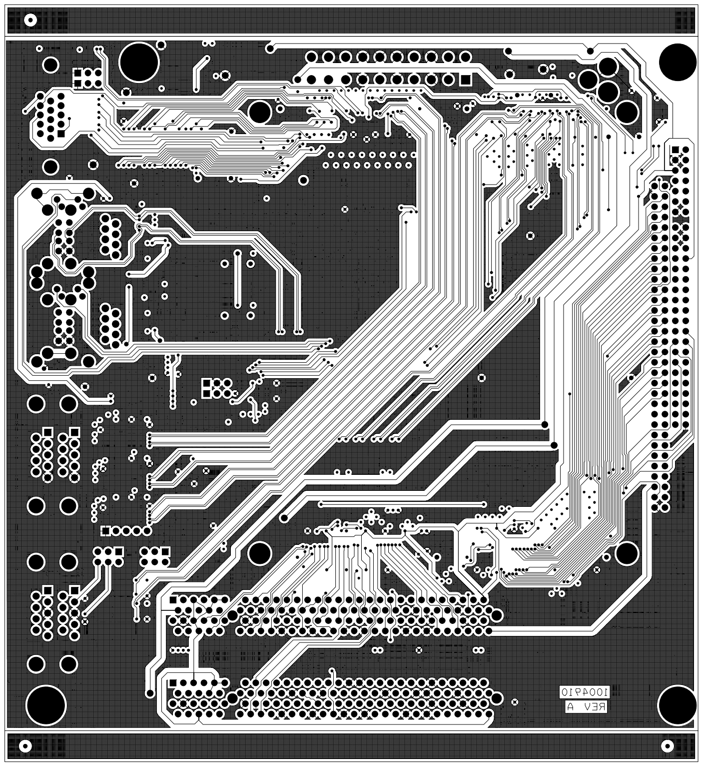

LOGIC PRODUCT DEVELOPMENT
ZOOM ITX
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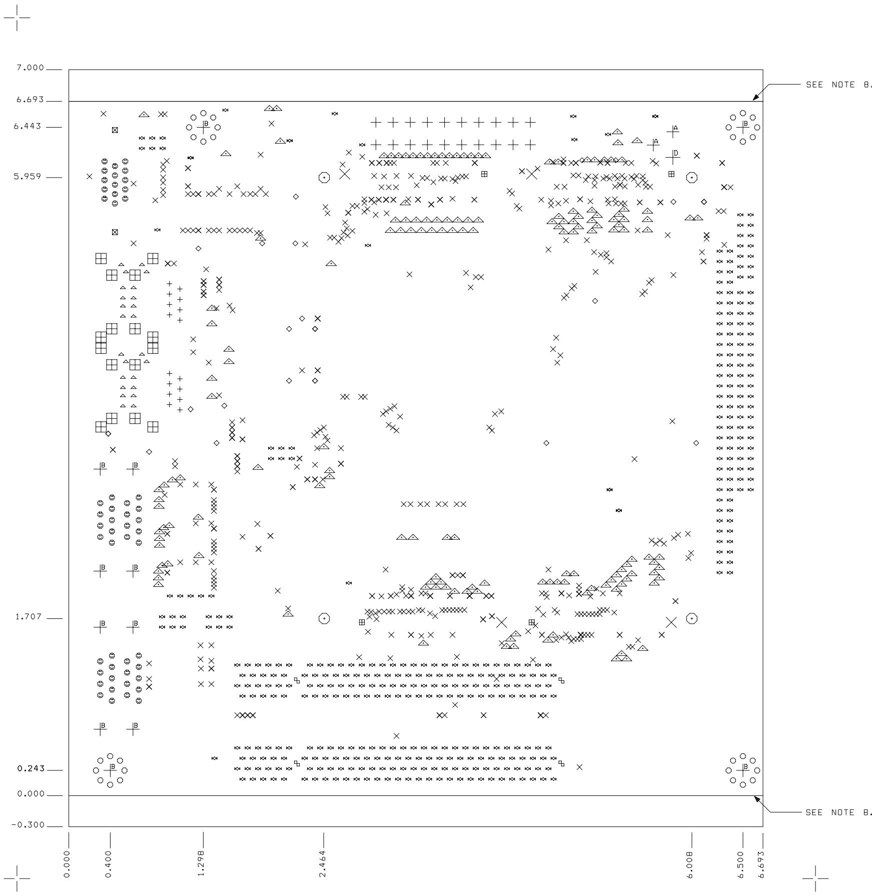
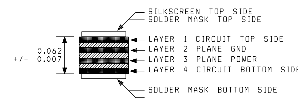
LAYER 4 CIRCUIT BOTTOM SIDE



DRILL

NOTE:

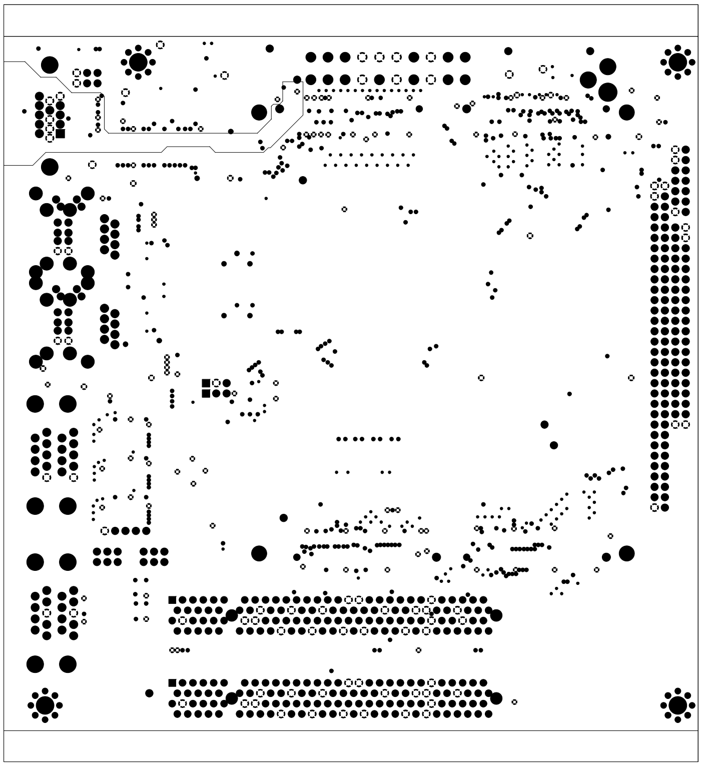
1. MATERIAL SELECTION:
   4 LAYER. EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/- 0.007 THICK.
   0.5 OZ. MINIMUM COPPER CLADDING WITH SMOBC.
2. FINISH ON ALL SOLDERABLE SURFACES TO BE:
   - [x] ENIG (ELECTROLESS NICKEL IMMERSION GOLD).
   - [ ] OSP - ENTEK PLUS 106A.
   - [ ] WHITE TIN.
3. SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - BLUE. USE LIQUID PHOTOIMAGEABLE RESIST.
4. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK.
5. MANUFACTURER'S IDENTIFICATION: ADD TO SILKSCREEN ON TOP SIDE.
6. ELECTRICAL BARE BOARD TEST REQUIRED.
7. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
8. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG. AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
9. BOARD TO BE IMPEDANCE CONTROLLED.
   IMPEDANCE TO BE CALCULATED AT 50 OHMS +/- 10%, .008" LINE WIDTH.
10. THE PRINTED CIRCUIT BOARDS MANUFACTURED TO THIS DRAWING MUST BE RoHS COMPLIANT.
    LAMINATE AND PREPREG SHALL BE POLYCLAD 370HR.
    ALTERNATIVE MATERIAL MUST BE APPROVED BY LOGIC/MDC PRIOR TO USE.



4 LAYER STACK-UP

DRILL CHART

SYM	DIAM	TOL	QTY	NOTE
△	0.010	+/- 0.003	159	PLATED
×	0.012	+/- 0.003	453	PLATED
◇	0.020	+/- 0.003	21	PLATED
⊞	0.028	+/- 0.003	4	NON-PLATED
○	0.035	+/- 0.003	32	PLATED
▵	0.036	+/- 0.003	24	PLATED
⋈	0.040	+/- 0.003	402	PLATED
⊖	0.043	+/- 0.003	51	PLATED
╳	0.043	+/- 0.003	4	NON-PLATED
+	0.045	+/- 0.003	16	PLATED
┼	0.055	+/- 0.003	20	PLATED
⊞	0.091	+/- 0.003	16	PLATED
⧉	0.096	+/- 0.003	4	NON-PLATED
⊙	0.098	+/- 0.003	4	PLATED
┼A	0.120	+/- 0.003	2	PLATED
┼B	0.125	+/- 0.003	12	PLATED
⊠	0.125	+/- 0.003	2	NON-PLATED
┼D	0.140	+/- 0.003	1	PLATED
TOTAL			1227	



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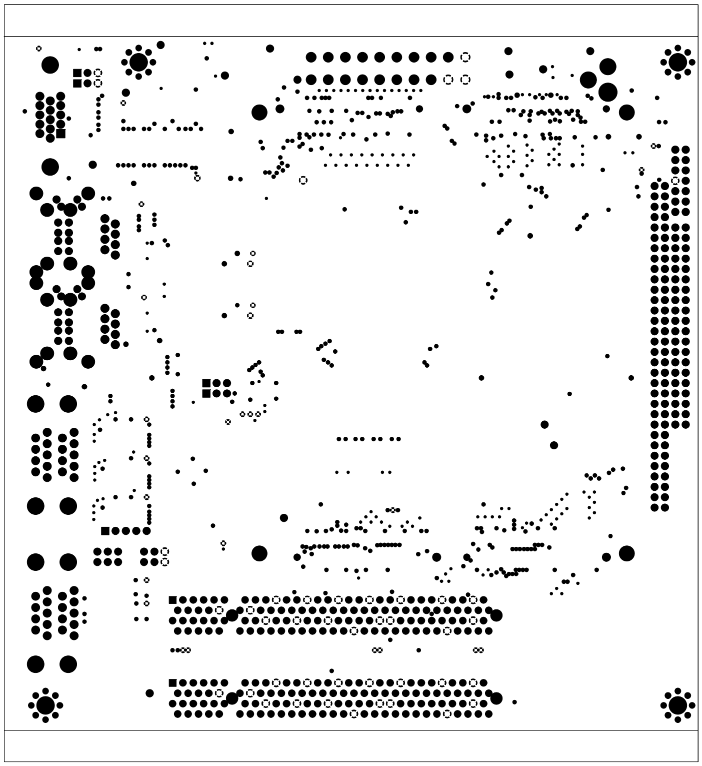
LAYER 2 PLANE GND



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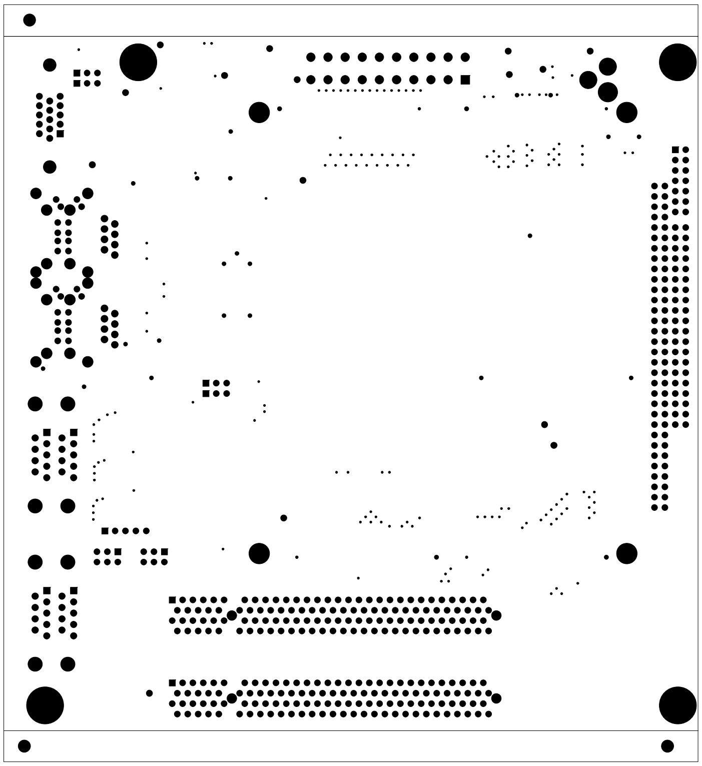
LAYER 3 PLANE POWER



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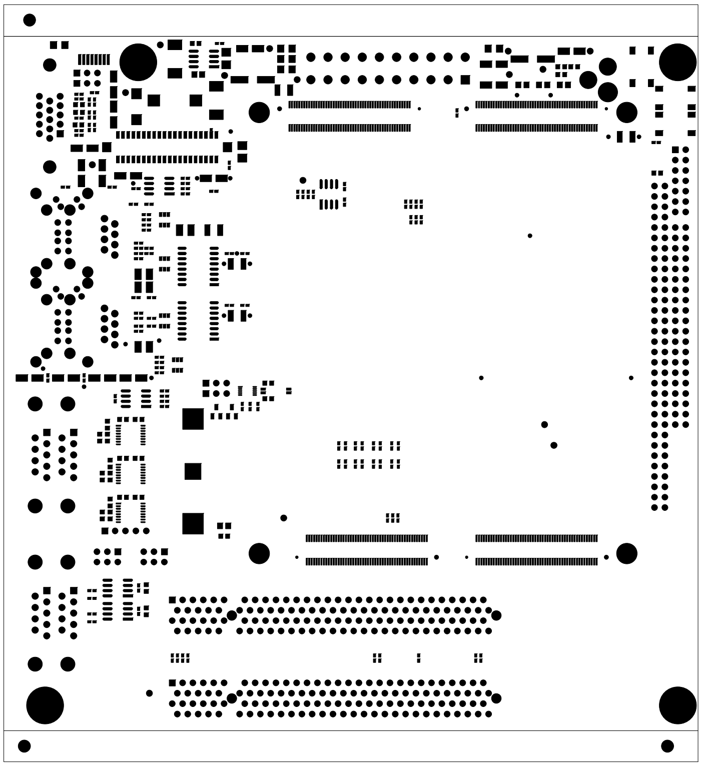
SOLDER MASK BOTTOM SIDE



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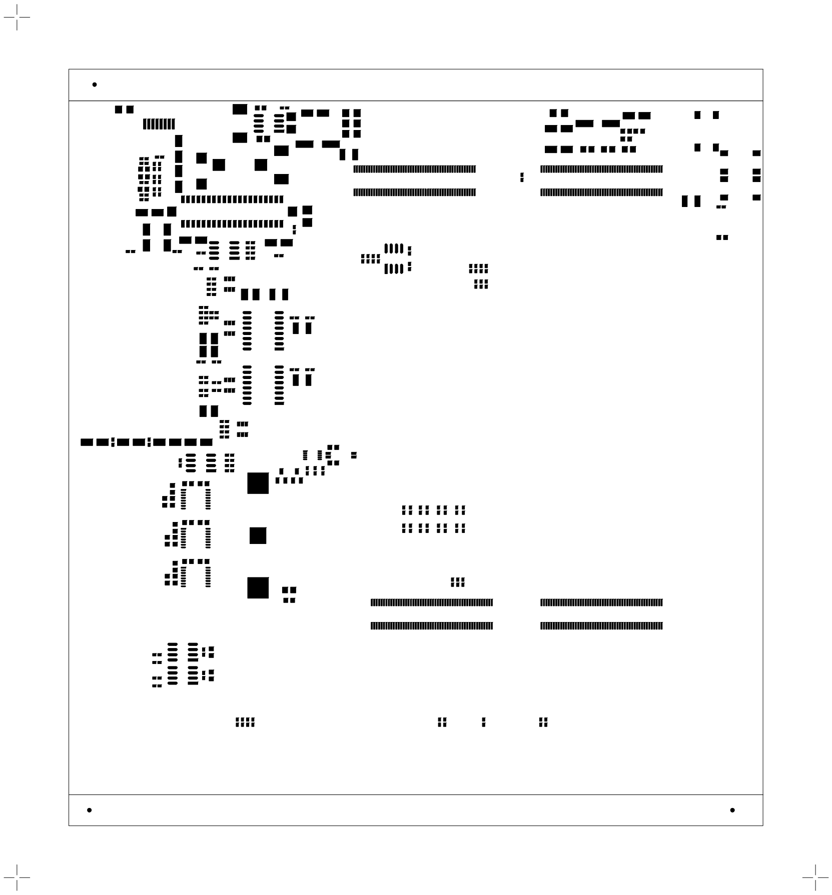
SOLDER MASK TOP SIDE



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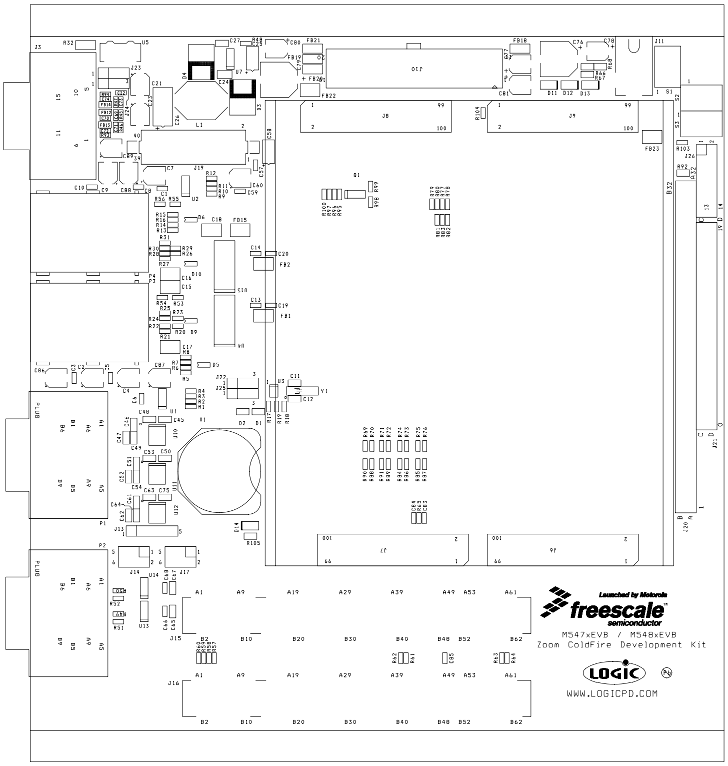
SOLDERPASTE TOP SIDE



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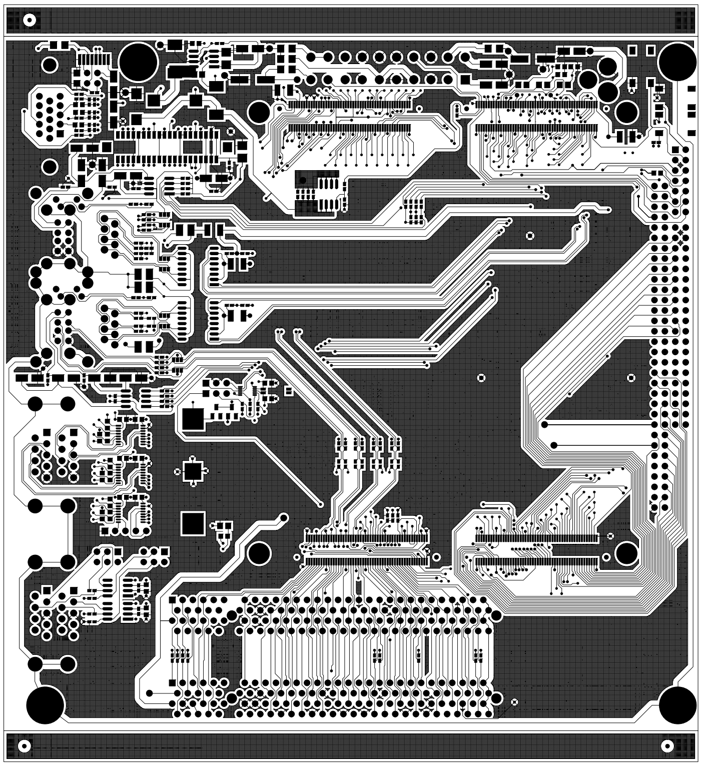
SILKSCREEN TOP SIDE



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LAYER 1 CIRCUIT TOP SIDE