LH7A404-11
Card Engine

ZOOM

LOGIC

IO Controller Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CPLD VERSION	APPROVAL	DATE
1	Erik Reynolds	Document Created	--	ER	05/28/04
A	James Wicks	Removed Preliminary References	--	ER	08/19/04
B	James Wicks	Updated Product Brief Section	--	KTL	12/08/04
C	Nathan Kro	Updated ISA-like BUS Diagrams, added Fast Area Diagrams	3.0	HAR	03/04/05
D	Hans Rempel	Rev C was incorrectly related to CPLD version 3.0 – Rev C of this document should have been for v.3.1.	3.1	HAR	03/18/05
E	Chris Rempel	Updated reset state of GPACT bit to “1” in GPIO Direction Register. Formatted register bit descriptions from high bit to low bit and added bit number to each description.	3.2	HAR	05/06/05
F	Jed Anderson	Added note to reference App Note 303 in Section 4	3.2	JCA	12/28/05
G	Jed Anderson	Formatting, design changes, and updated Product Brief; Updated acronyms section; Section 1.3: Replaced Altera CPLD information with Xilinx CPLD	3.2	JCA	06/26/07

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

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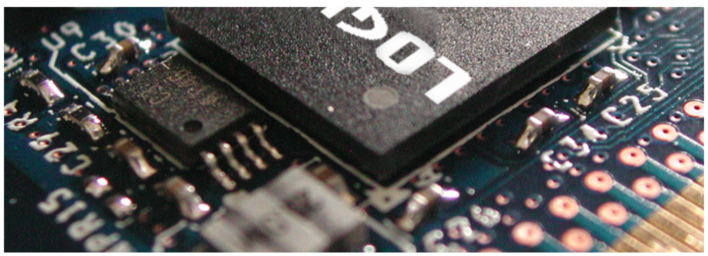
PRODUCT BRIEF:
Logic embedded product solutions

LH7A404 IO Controller

Logic offers production-ready IO controller devices and design packages for customers creating custom Card Engine designs and CPLD code for Logic's Card Engines. Logic has optimized the VHDL code to fit in the smallest possible programmable logic device. This helps you stay focused on your high-value core technologies and fast forwards your embedded designs.



Product Features

IO Controller written in VHDL and contains the following:

+ ISA-like bus interface
+ SMSC LAN91C111 wired LAN bus interface and power control logic
+ Buffer control logic
+ Chip select decoder logic
+ Interrupt encoder logic
+ Flash program control logic
+ Processor mode control logic
+ IC code revision register

Source Code

+ Includes all VHDL code (licensable .vhd source code files)

Support

+ VHDL IP Core Source Code Design Package includes the Bronze level support package

LOGIC WEBSITE :: DESIGN RESOURCES:

+ Logic Technical Support : http://www.logicpd.com/support/
+ Technical Discussion Group : http://www.logicpd.com/support/tdg/
+ Frequently Asked Questions (FAQ) : http://www.logicpd.com/support/faq/
+ For more information contact Logic Sales : product.sales@logicpd.com

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1.2 Acronyms

BALE	Buffered Address Latch Enable
CF	CompactFlash
CPLD	Complex Programmable Logic Device
CS	Chip Select
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
IO	Input Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LAN	Local Area Network
SPI	Serial Peripheral Interface

1.3 Technical Specifications

Please refer to the following component specifications and data sheets.

- Xilinx Coolrunner™-II CPLD Product Specification (XC2C128-7VQG100C) http://www.xilinx.com/
- Xilinx Device Package User Guide http://www.xilinx.com/

1.4 IO Controller Advantages

Some of the key features in the IO Controller include:

- Chip Select Decoder
- Interrupt Decoder
- ISA-Like Bus Interface
- Bus Control Logic
- Programmable Register Control
- GPIO Interface
- In-System Programmability via JAM Player

The IO Controller VHDL source code is available for purchase. Contact Logic for more information.

2 IO Controller Block Diagram

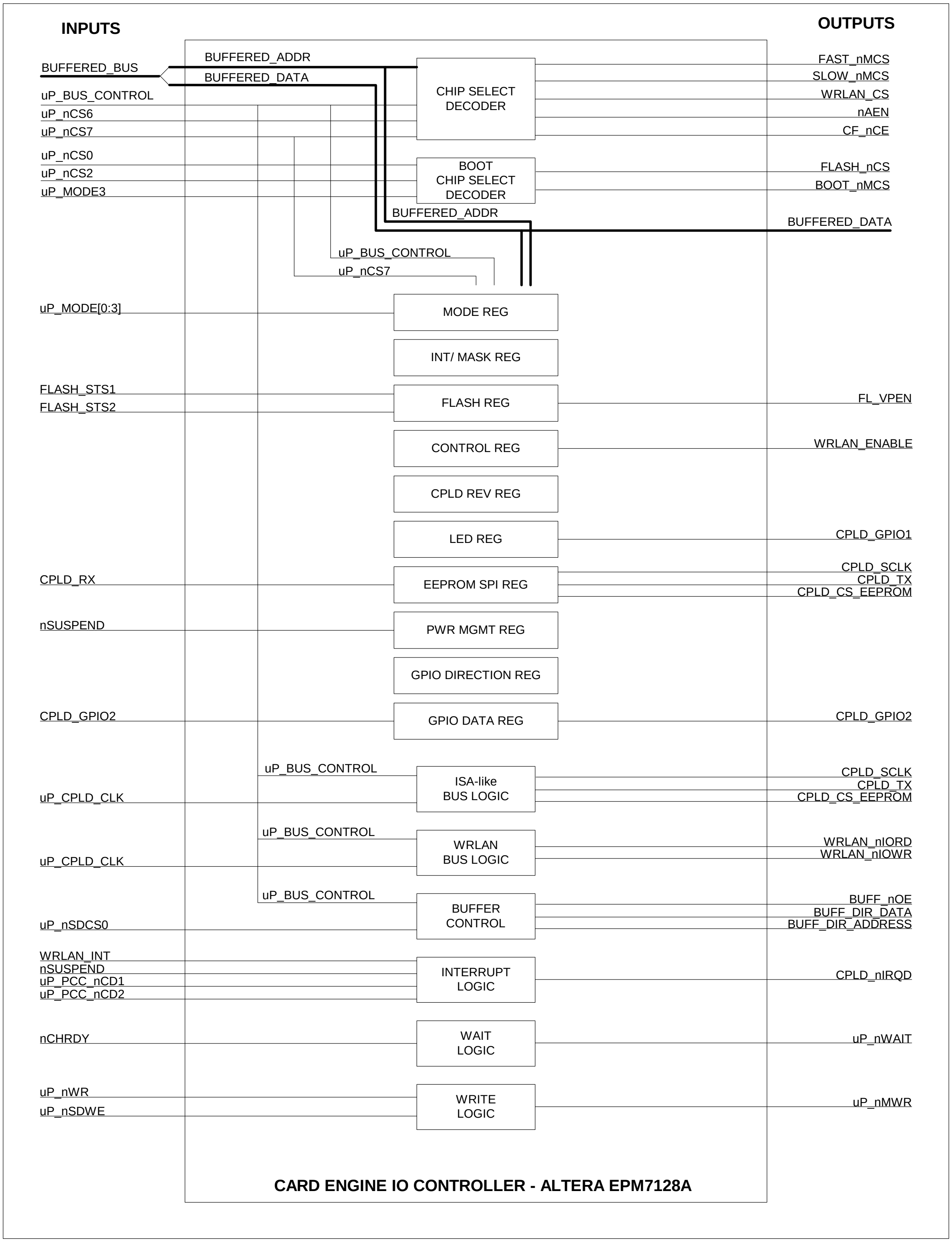

Figure 2.1: IO Controller Block Diagram

3 IO Controller Address and Register Definitions

Address Range	Memory Block Description	Size
0x7000 0000 – 0x7FFF FFFF	Fast Peripherals Chip Select 7 (CS7)	64MB
0x6000 0000 – 0x6FFF FFFF	Slow Peripherals Chip Select 6 (CS6)	64MB

3.1 Fast Peripherals Chip Select 7 (CS7)

Address Range	Memory Block Description	Size
0x7000 0000 – 0x701F FFFF	Wired LAN Chip Select	2MB
0x7020 0000 – 0x703F FFFF	Card Engine Control Reg	2MB
0x7040 0000 – 0x705F FFFF	Reserved	2MB
0x7060 0000 – 0x707F FFFF	Reserved	2MB
0x7080 0000 – 0x709F FFFF	Reserved	2MB
0x70A0 0000 – 0x70BF FFFF	EEPROM SPI Reg	2MB
0x70C0 0000 – 0x70DF FFFF	Interrupt/Mask Reg	2MB
0x70E0 0000 – 0x70FF FFFF	Mode Reg	2MB
0x7100 0000 – 0x711F FFFF	FLASH Reg	2MB
0x7120 0000 – 0x713F FFFF	Power Management Reg	2MB
0x7140 0000 – 0x715F FFFF	IO Controller Code Revision Reg	2MB
0x7160 0000 – 0x717F FFFF	Extended GPIO Reg	2MB
0x7180 0000 – 0x719F FFFF	GPIO Data Reg	2MB
0x71A0 0000 – 0x71BF FFFF	GPIO Direction Reg	2MB
0x71C0 0000 – 0x71FF FFFF	Reserved - On-Board Expansion	2MB (X2)
0x7200 0000 – 0x72FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x7300 0000 – 0x73FF FFFF	Open – Available for User	1MB (X16)

Each memory block for chip select 7 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.1.1 Wired LAN Chip Select

Address Range: 0x7000 0000 – 0x701F FFFF

- This area of memory is used when accessing the wired LAN chip (internal registers/memory).

3.1.2 Card Engine Control Register

Address Range: 0x7020 0000

- This register holds control bits for the Card ngine.

7	6	5	4	3	2	1	0	
SWINT	-	-	-	-	AWKP	-	nWLPE	
1	-	-	-	-	0	-	0	reset
R/W	-	-	-	-	R/W	-	R/W	R/W

SWINT (7): Software settable interrupt source
0 = generate an interrupt on uP_CPLD_nIRQ
1 = do not generate an interrupt on uP_CPLD_nIRQ

NA (6:3): Reserved.

AWKP (2): Auto-Wakeup enable signal. This bit enables/disables the uP_WAKEUP signal which is used at power up to automatically bring the processor out of the standby state.
0 = Auto-Wakeup feature enabled, note that this feature has been removed
1 = Auto-Wakeup feature disabled, note that this feature has been removed

NA (1): Reserved.

nWLPE (0): wired LAN power enable signal. This bit enables/disables power to the on-board wired LAN chip.
0 = Wired LAN enabled
1 = Wired LAN disabled

3.1.3 Reserved

Address Range: 0x7040 0000 – 0x709F FFFF

- These memory blocks are reserved.

3.1.4 EEPROM SPI Interface Register

Address Range: 0x70A0 0000

- This register holds SPI data during a read/write between the processor and on-board EEPROM. The processor, not the IO Controller, implements the SPI interface used for the EEPROM.

7	6	5	4	3	2	1	0	
-	-	-	-	EECS	EECK	EETX	EERX	
-	-	-	-	0	0	0	0	reset
-	-	-	-	R/W	R/W	R/W	R	R/W

NA (7:4): Reserved.

EECS (3): EEPROM chip select.
0 = not selected
1 = EEPROM chip selected

EECK (2): EEPROM SPI clock.

EETX (1): EEPROM SPI data transmit.

EERX (0): EEPROM SPI data receive.

3.1.5 Interrupt/Mask Register

Address Range: 0x70C0 0000

- This register contains the information used by the IO Controller to generate an interrupt to the processor on signal CPLD_nIRQ.

7	6	5	4	3	2	1	0	
-	-	-	-	-	WMSK	-	nWIRQ	
-	-	-	-	-	0	-	1	reset
-	-	-	-	-	R/W	-	R	R/W

NA (7:3): Reserved.

WMSK (2): wired LAN chip interrupt mask.
0 = interrupt not masked
1 = interrupt masked

NA (1): Reserved.

nWIRQ (0): wired LAN chip interrupt request (IRQ).
0 = interrupt
1 = no interrupt

3.1.6 Mode Register

Address Range: 0x70E0 0000

- This register holds the values of the mode pins.

7	6	5	4	3	2	1	0	
BVD2	CD2	BVD1	CD1	MDP3	MDP2	MDP1	MDP0	
-	-	-	-	-	-	-	-	reset
R	R	R	R	R	R	R	R	R/W

BVD2 (7): PCMCIA Voltage Detect 2 input. Signal name uP_PCC_BVD2.
0 = Active slot Voltage Detect 2 is low
1 = Active slot Voltage Detect 2 is high

CD2 (6): PCMCIA Card Detect 2 input. Signal name PCC_nCD2.
0 = Active slot Card Detect 2 is low
1 = Active slot Card Detect 2 is high

BVD1 (5): PCMCIA Voltage Detect 1 input. Signal name uP_PCC_BVD1.
0 = Active slot Voltage Detect 1 is low
1 = Active slot Voltage Detect 1 is high

CD1 (4): PCMCIA Card Detect 1 input. Signal name PCC_nCD1.
0 = Active slot Card Detect 1 is low
1 = Active slot Card Detect 1 is high

MDP3 (3): mode pin 3. Mode pin 3 selects between on-board and off-board boot device. See Section 4.2 for detailed information on mode pin 3.
0 = off-board boot device
1 = on-board boot device (32 bit FLASH)

MDP2 (2): mode pin 2. Mode pin 2 represents the endian setting for the processor. (The LH7A404 supports little endian only. The value of this bit is ignored.)
0 = big endian
1 = little endian

MDP1, MDP0 (1:0): mode pin 1 and mode pin2. These mode pins represent the bus width at boot. Bit MDP0 controls processor pin BOOTWIDTH0 and bit MDP1 controls processor pin BOOTWIDTH1. (Note: See LH7A404 datasheet for specific setting options for pins BOOTWIDTH0 and BOOTWIDTH1.)

3.1.7 Flash Register

Address Range: 0x7100 0000

- This register holds status information for the FLASH.

7	6	5	4	3	2	1	0	
-	-	-	-	nFPOP	FST2	FST1	FPEN	
-	-	-	-	1	-	-	0	reset
-	-	-	-	R/W	R	R	R/W	R/W

NA (7:4): Reserved.

nFPOP (3): Flash populated bit. This bit is used to generate the flash chip select, when mode pin 3 is low. This bit is ignored when mode pin 3 is high. See Section 4.2 for detailed information on mode pin 3.
0 = Flash populated
1 = Flash not populated

FST2 (2): Flash status pin. This is the RY/BY# pin for the upper 16-bit flash chip.
0 = Flash busy
1 = Flash ready

FST1 (1): Flash status pin. This is the RY/BY# pin for the lower 16-bit flash chip.
0 = Flash busy
1 = Flash ready

FPEN (0): Flash program enable.
0 = normal flash operations
1 = program flash enabled

3.1.8 Power Management Register

Address: 0x7120 0000

- This register holds the value of the nSUSPEND and nSTANDBY input signals to the CPLD. When nSUSPEND or nSTANDBY is low, an interrupt to the processor will be generated. There are no interrupt mask bits for the nSUSPEND or nSTANDBY signals.

7	6	5	4	3	2	1	0	
-	-	-	STBY	-	SPND	-	-	
-	-	-	-	-	-	-	-	reset
-	-	-	R	-	R	-	-	R/W

NA (7:5): Reserved.

STBY (4): value of the nSTANDBY input signal to the CPLD. The nSTANDBY signal has a pull up resistor on the Card Engine.
0 = nSTANDBY signal is low
1 = nSTANDBY signal is high

NA (3): Reserved.

SPND (2): value of the nSUSPEND input signal to the CPLD. The nSUSPEND signal has a pull-up resistor on the Card Engine.
0 = nSUSPEND signal is low
1 = nSUSPEND signal is high

NA (1:0): Reserved.

3.1.9 IO Controller Code Revision Register

Address Range: 0x7140 0000

- This register holds the IO Controller code revision number.

7	6	5	4	3	2	1	0	
8-bit revision number								
8-bit revision number								reset
R								R/W

3.1.10 Extended GPIO Register

Address Range: 0x7160 0000

- This register controls extended general-purpose signals.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	CPLD_GPIO_1	
-	-	-	-	-	-	-	1	reset
-	-	-	-	-	-	-	R/W	R/W

NA (7:1): Reserved.

CPLD_GPIO_1 (0): General purpose output-only bit.
0 = set pin low
1 = set pin high

3.1.11 GPIO Data Register

Address: 0x7180 0000

- This register controls data for the CPLD general purpose input/output pins. Note: The direction (input or output) of the CPLD pins are set in the GPIO Direction Register in Section 3.1.12.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	-	CPLD_GPIO_2	
-	-	-	-	-	-	-	0	reset
-	-	-	-	-	-	-	R/W	R/W

NA (7:1): Reserved.

CPLD_GPIO_n (0): Controls the state of general purpose input/output bit CPLD_GPIO_n (where n = 2.3) when configured as an output, reads pin state when configured as an input.
0 = Set pin low if configured as output, read pin state low if configured as input
1 = Set pin high if configured as output, read pin state high if configured as input

3.1.12 GPIO Direction Register

Address: 0x71A0 0000

- This register controls the direction for the CPLD general purpose input/output pins. Note: The value (high or low) of the CPLD pins are read/written in the GPIO Data Register in Section3.1.11.

7	6	5	4	3	2	1	0	
-	-	-	-	-	-	GPACT	GPDR0	
-	-	-	-	-	-	1	0	reset
-	-	-	-	-	-	R/W	R/W	R/W

NA (7:2): Reserved.

GPACT (1): GPIO active bit 1.
0 = input PCMCIA control signals to CPLD enabled (GPIO disabled).
1 = input PCMCIA control signals to CPLD disabled (GPIO enabled).

GPDR0 (0): GPIO direction bit 0.
0 = external CPLD signal CPLD_GPIO_2 is an output
1 = external CPLD signal CPLD_GPIO_2 is an input

3.1.13 Reserved On-Board Memory Blocks

Address Range: 0x71C0 0000 – 0x71FF FFFF

- These two memory blocks are reserved for future on-board expansion.

3.1.14 Reserved Off-Board Memory Blocks

Address Range: 0x7200 0000 – 0x72FF FFFF

- These sixteen memory blocks are reserved for off-board IO controller expansion.

3.1.15 Open Memory Blocks – Available for User

Address Range: 0x7300 0000 – 0x73FF FFFF

- These sixteen memory blocks are open and available for the user to utilize.

3.2 Slow Peripherals Chip Select 6 (CS6)

Address Range	Memory Block Description	Size
0x6000 0000 – 0x601F FFFF	Reserved	2MB
0x6020 0000 – 0x603F FFFF	CF Chip Select	2MB
0x6040 0000 – 0x605F FFFF	ISA-like Bus Chip Select	2MB
0x6060 0000 – 0x61FF FFFF	Reserved - On-Board Expansion	2MB (X13)
0x6200 0000 – 0x62FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x6300 0000 – 0x63FF FFFF	Open – Available for User	1MB (X16)

Each memory block for chip select 6 is described below. The register definitions include bit descriptions, read/write access allowed, and the initial value upon reset.

3.2.1 CompactFlash (CF) Chip Select

Address Range: 0x6020 0000 – 0x603F FFFF

- This area of memory is used when accessing the off-board memory-mapped CompactFlash Type 1 Memory Only slot.

3.2.2 ISA-like Bus Chip Select

Address Range: 0x6040 0000 – 0x605F FFFF

- The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This area of memory is used when accessing off-board components on the “ISA-like” bus. See Section 5 for read and write timing diagrams.

3.2.3 Reserved On-Board Memory Blocks

Address Range: 0x6060 0000 – 0x61FF FFFF

- These memory blocks are reserved for future on-board expansion.

3.2.4 Reserved Off-Board Memory Blocks

Address Range: 0x6200 0000 – 0x62FF FFFF

- These memory blocks are reserved for off-board IO controller expansion.

3.2.5 Open Memory Blocks – Available for User

Address Range: 0x6300 0000 – 0x63FF FFFF

- These memory blocks are open and available for the user to utilize.

4 IO Controller Functions

This section describes in detail the different IO Controller function blocks. See Section 2 for the IO Controller block diagram.

Note: A specific software protocol must be followed to access IO devices on Sharp Card Engines. Please see Logic's Application Note 303: *Interfacing to IO Devices via the Static Memory Controller on LH7xxxx Card Engines* for examples of the protocol when accessing registers within the CPLD. This document can be found at: http://www.logicpd.com/auth/.

4.1 Chip Select Decoder Logic

This logic decodes processor memory areas 6 and 7 into smaller segments of memory. See Section 3.1 for the chip select 7 memory map, and Section 3.2 for the chip select 6 memory map.

CPLD signal FAST_nCS is output when uP_nCS7 is low and uP_MA25 is high. CPLD signal SLOW_nCS is output when uP_nCS6 is low and uP_MA25 is high. Signals FAST_nCS and SLOW_nCS are brought off the Card Engine through the expansion bus connectors.

4.2 Boot Chip Select Decoder Logic

Note: Mode pin 3 selects between on-board and off-board boot device.

The Card Engine can boot from the 32-bit on-board flash or an 8-, 16-, or 32-bit off-board memory device. The boot device is determined by a jumper setting (mode pin 3) on the application board. The boot device is always located in area 0 (CS0). When mode pin 3 is high, the on-board flash is selected for boot, and when mode pin 3 is low, the off-board memory device is selected for boot. This logic implements the following table.

Flash register bit (3) is used to generate the flash chip select, when mode pin 3 is low. This bit is ignored when mode pin 3 is high. See Section 3.1.7 for more information on the flash register.

Flash (on-board)	Off-board memory	Mode Pin 3	Flash Reg (3)	Function
CS0 (area 0)	CS2 (area 2)	1	ignored	boot from flash in area 0, off-board memory device is in area 2
CS2 (area 2)	CS0 (area 0)	0	0	boot from off-board memory device in area 0, flash is in area 2
CS2 (area 2)	CS0 (area 0)	0	1	boot from off-board memory device in area 0, (flash not populated) area 2 is open

The chip selects for area 0 and 2 are routed externally to the flash and off-board memory device by signals FLASH_nCS and BOOT_nMCS.

4.3 ISA-like Bus Logic (CompactFlash and ISA peripherals in area 6)

The ISA-like bus is similar to the ISA bus standard, but does not meet every requirement within the standard. This logic outputs the ISA chip select, CompactFlash chip select, BALE, read (nIORD), and write (nIOWR) signals. It also creates two timing delays in the ISA-like bus timing: first, the delay between the falling edge of the chip select (CompactFlash or ISA) and falling edge of read (nIORD) or write (nIOWR) signal, and second, the delay between the rising edge of the read or write signal and rising edge of the chip select.

The first delay is created by shifting the falling edge of the read (nIORD) or write (nIOWR) signal to create a delay from the chip select. The rising edge of the read and write signals are not delayed from the rising edge of the processor read and write signals. See Section 5 for sample read and write ISA-like timing diagrams.

The ISA device chip select is output by the CPLD when an access to address range 0x6040 0000 – 0x605F FFFF is made, and the CompactFlash chip select is output when an access to address range 0x6020 0000 – 0x603F FFFF is made. To create a timing delay between the rising edge of the read or write signal and the rising edge of the chip select, the chip select rising edge is delayed from the processor's area 6 chip select by a single bus clock cycle. The Card Engine buffers are turned off during this chip select extension, to retain the data on the bus while the chip select is still valid. This is only for the ISA and CompactFlash peripherals in area 6. See Section 5 for sample read and write ISA-like timing diagrams.

The ISA-like bus timing is shown with internal wait states programmed for the processor. This is shown in order to meet the CompactFlash timing. The user can verify/change these values by modifying the WST1 and WST2 fields in the processor's Static Memory Controller Bus Configuration Register, for area 6.

The nCHRDY input signal to the CPLD is shown in the ISA-like bus timing diagrams. It can be asserted by CompactFlash or an ISA device. When pulled low, the nCHRDY signal generates a low on the uP_nWAIT signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. The nCHRDY low pulse width for CompactFlash is a maximum of 350ns, and an example of this signal is shown in the timing diagrams. Not all CompactFlash cards or ISA devices will assert the nCHRDY signal. Therefore, the other signals in the read and write timing diagrams are shown assuming the nCHRDY signal was not pulled low.

4.4 Wired LAN Bus Logic

This logic creates read and write output signals to the wired LAN chip by shifting the falling edge of the read and write signals from the processor, to meet the required Wired LAN timing. The rising edge of the wired LAN read and write signals are not shifted.

An interrupt to the processor is generated when an interrupt from the wired LAN is seen at the CPLD.

4.5 Buffer Control Logic

This logic controls the output enable and direction of the on-board buffers.

4.6 Interrupt Logic

This logic generates the processor's CPLD_nIRQ, from information in the Interrupt/Mask register, Section 3.1.5, and the Power Management register, Section 3.1.8.

5 ISA and Fast Area Timing Diagrams

Note: All timing parameters shown in nanoseconds (ns). Timing is based on a 10ns clock cycle. SLOW_nCS and FAST_nCS are only asserted when A25 is zero. Signals nIORD and nIOWR are generated for any access to either uP_nCS6 or uP_nCS7, regardless of the address line states. WRLAN_nIORD and WRLAN_nIOWR are generated for any access to uP_nCS7, regardless of the address line states.

5.1 ISA-like Bus, Read Cycle Timing Diagram

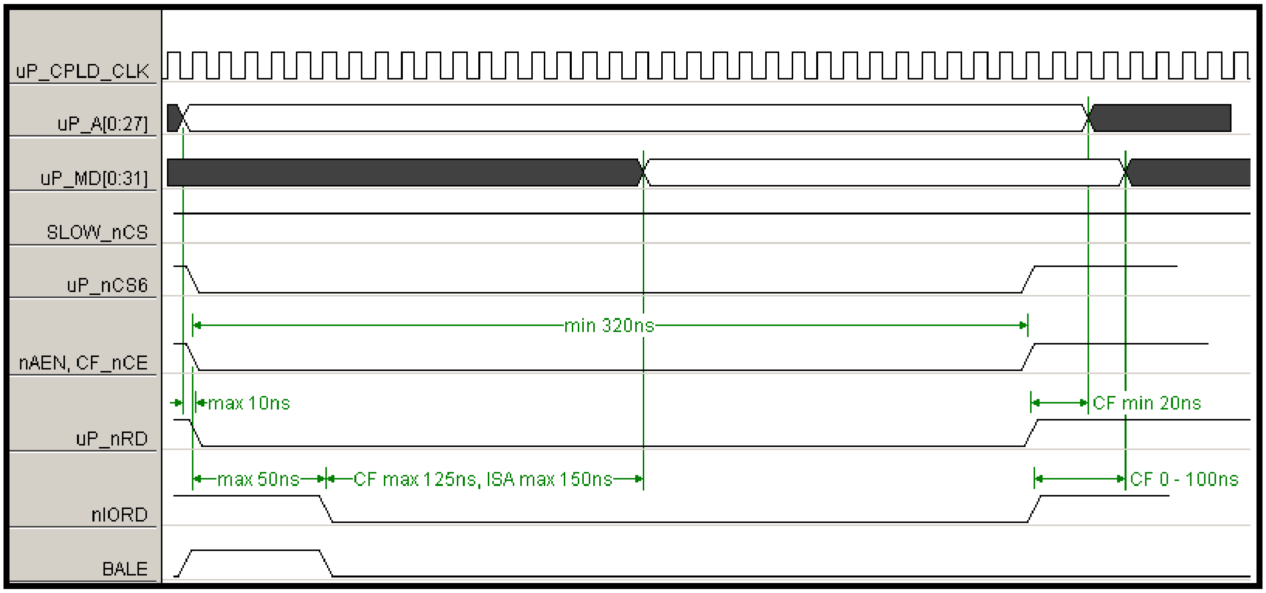

Figure 5.1: ISA-like Bus, Read Cycle Timing

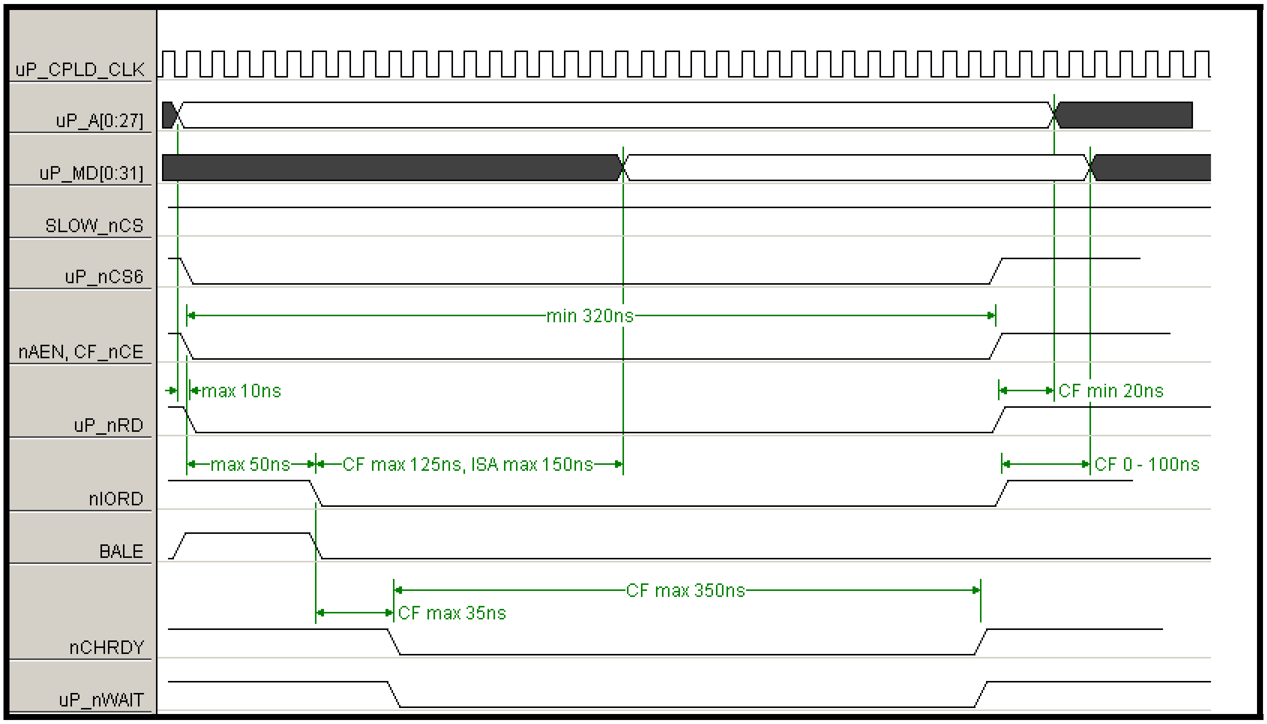

Figure 5.2: ISA-like Bus, Read Cycle Timing, uP_nWAIT asserted

5.2 ISA-like Bus, Write Cycle Timing Diagram

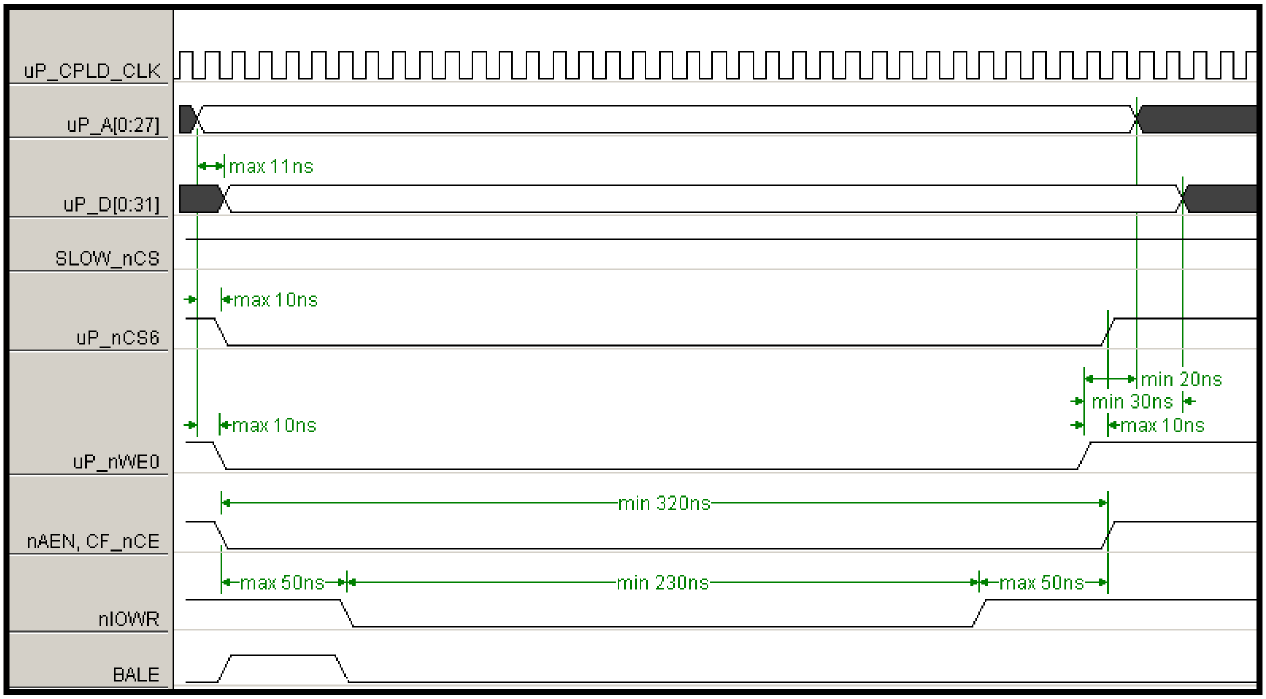

Figure 5.3: ISA-like Bus, Write Cycle Timing

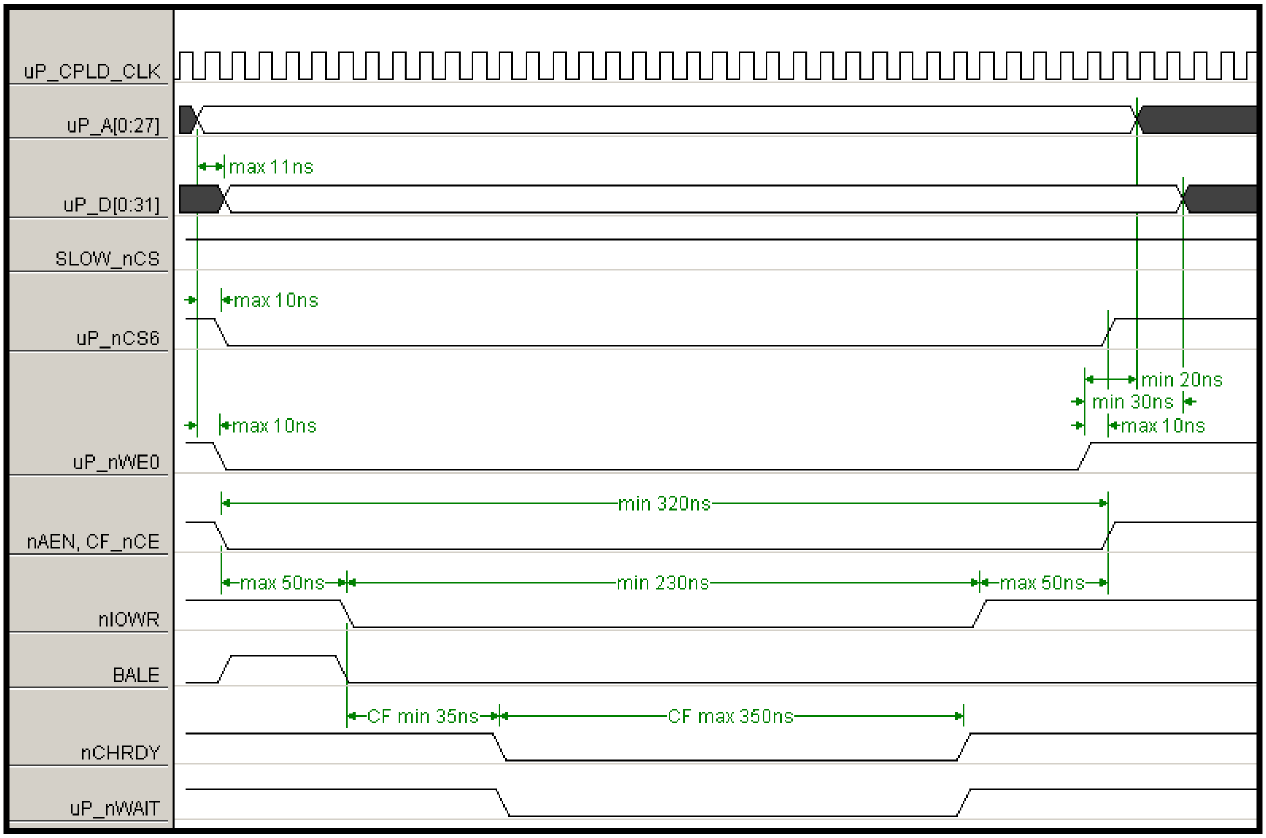

Figure 5.4: ISA-like Bus, Write Cycle Timing, uP_nWAIT asserted

5.3 Fast Area, WRLAN, Read Cycle Timing Diagram

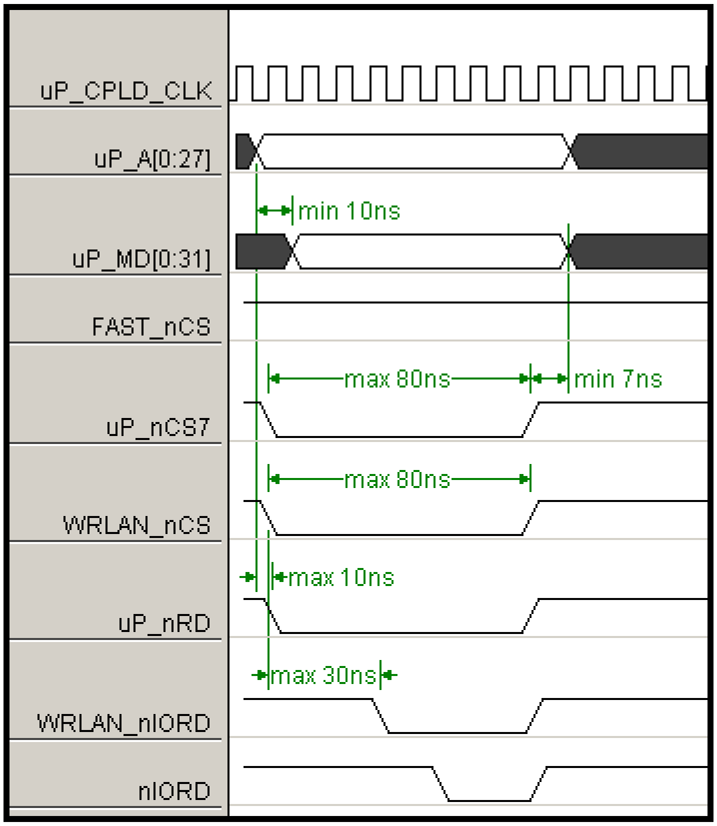

Figure 5.5: Fast Area, WRLAN, Write Cycle Timing

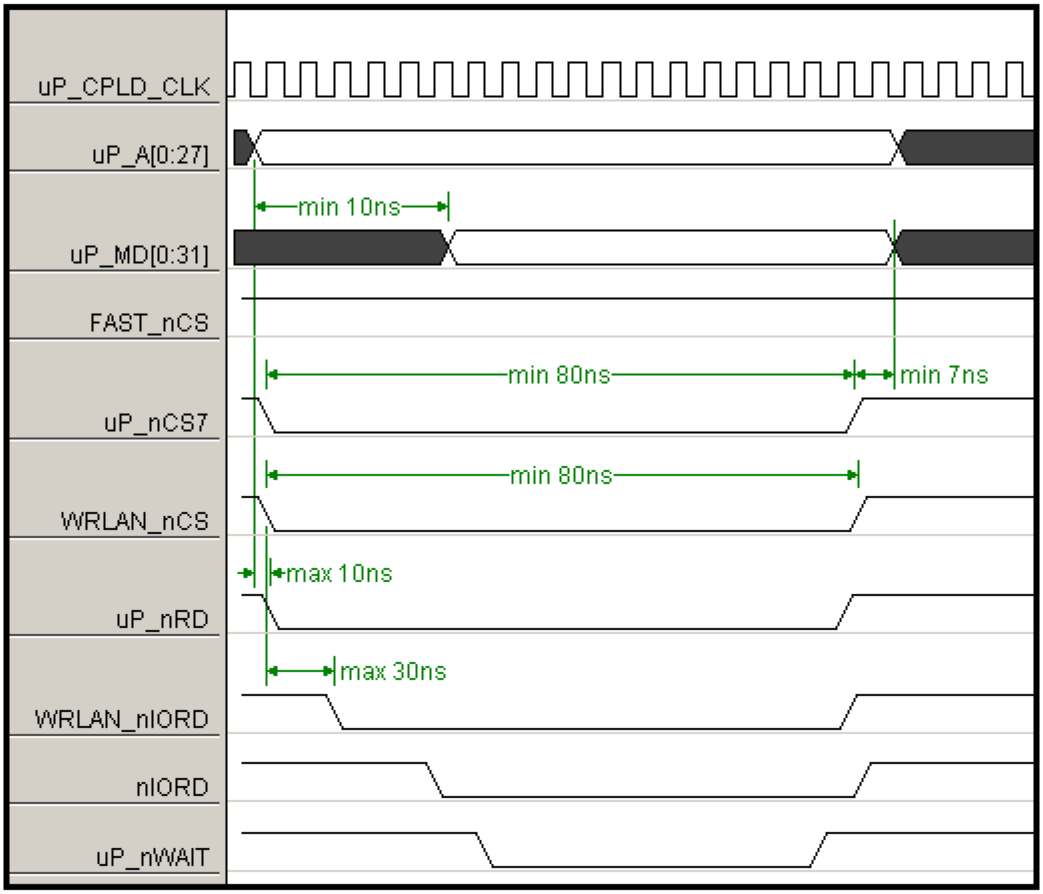

Figure 5.6: Fast Area, WRLAN, Write Cycle Timing, uP_nWAIT asserted

5.4 Fast Area, WRLAN, Write Cycle Timing Diagram

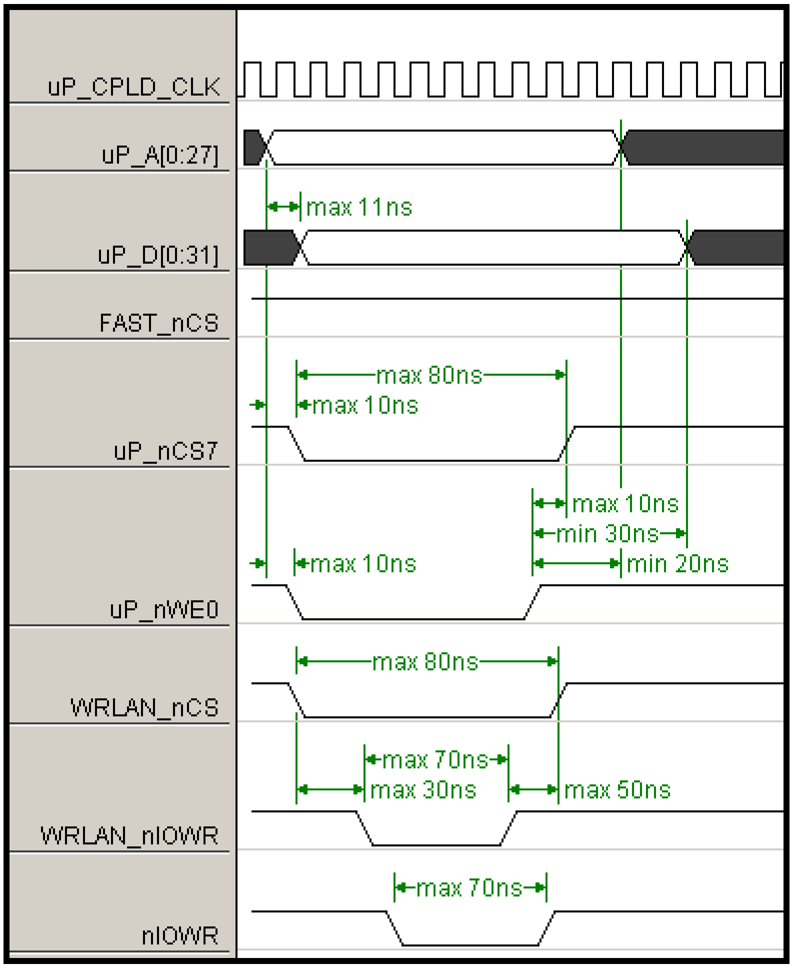

Figure 5.7: Fast Area, WRLAN, Read Cycle Timing

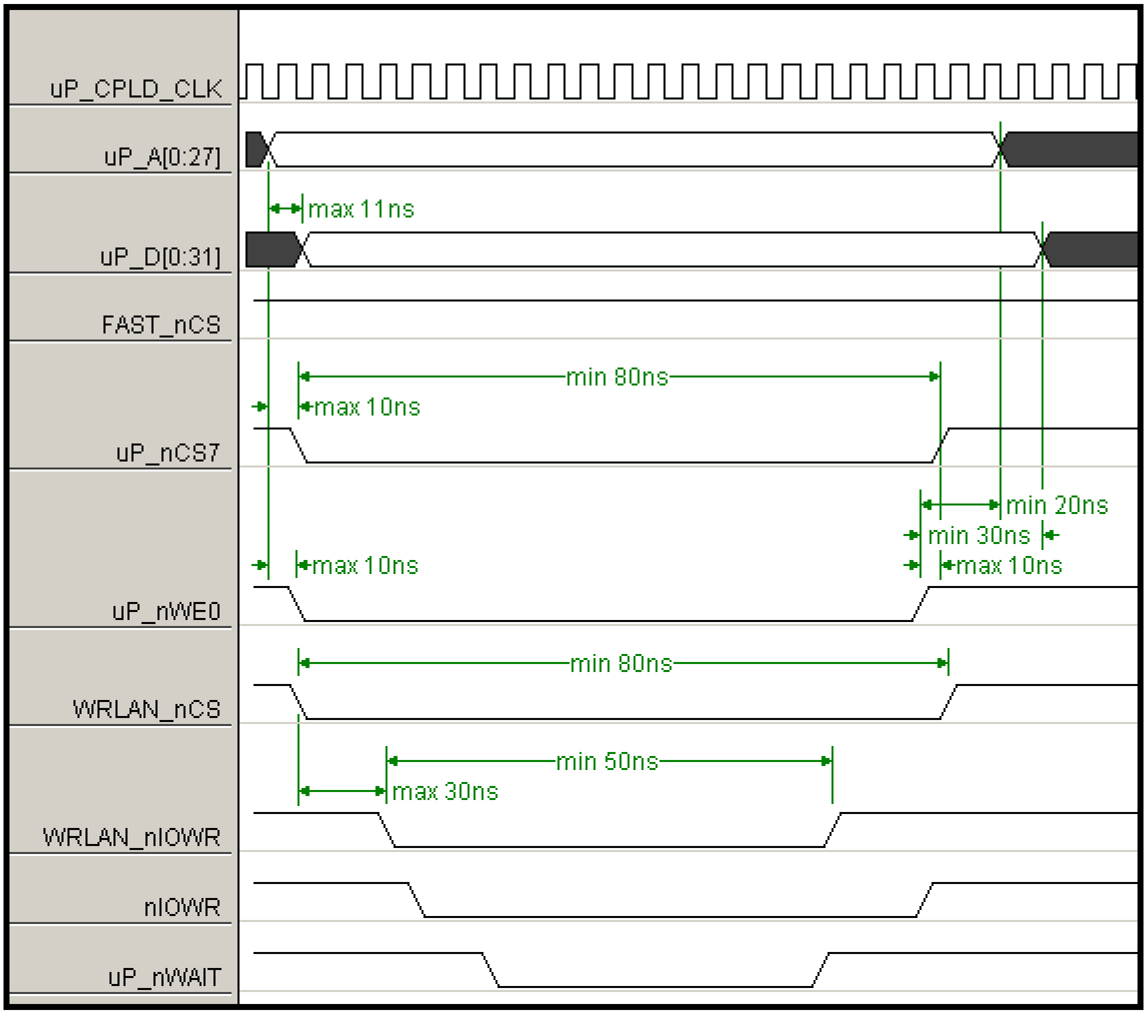

Figure 5.8: Fast Area, WRLAN, Read Cycle Timing, uP_nWAIT asserted

6 IO Controller Pin Information

Pin	Signal Name	Input/Output
14	uP_nCS0	Input
17	uP_nMCS2	Input
33	uP_nMCS6	Input
32	uP_nMCS7	Input
35	SLOW_nMCS	Output
36	FAST_nMCS	Output
34	WRLAN_nCS	Output
18	uP_PCC_nCD1	Input
19	uP_PCC_nCD2	Input
39	uP_nWR	Input
63	CPLD_CS_EEPROM	Output
15	BOOT_nMCS	Output
16	FLASH_nCS	Output
46	CPLD_SCLK	Output
54	CPLD_TX	Output
59	CPLD_RX	Input
27	uP_CPLD_CLK	Input
3	UP_MA25	Input
4	UP_MA24	Input
1	UP_MA23	Input
2	UP_MA22	Input
6	UP_MA21	Input
50	uP_MODE3	Input
52	uP_MODE2	Input
53	uP_MODE1	Input
55	uP_MODE0	Input
56	FL_VPEN	Output
42	FLASH_STS1	Input
43	FLASH_STS2	Input
58	WRLAN_ENABLE	Output
29	CPLD_nIRQ	Output
37	uP_nSDWE	Input
30	WRLAN_INT	Input
49	nSUSPEND	Input
67	UP_MD0	Input/Output
68	UP_MD1	Input/Output
70	UP_MD2	Input/Output
71	UP_MD3	Input/Output
72	UP_MD4	Input/Output
74	UP_MD5	Input/Output
76	UP_MD6	Input/Output
77	UP_MD7	Input/Output

Pin	Signal Name	Input/Output
41	CPLD_GPIO_1	Output
60	CPLD_GPIO_2	Input/Output
7	uP_nSDCS0	Input
23	uP_nRD	Input
22	uP_nMWE0	Input
40	uP_nMWR	Output
97	uP_nWAIT	Output
10	BUFF_nOE	Output
11	BUFF_DIR_DATA	Output
12	WRLAN_nIOWR	Output
13	WRLAN_nIORD	Output
65	nIOWR	Output
66	nIORD	Output
73	BALE	Output
80	nCHRDY	Input
82	nAEN	Output
99	MSTR_nRST	Input
85	CF_nCE	Output
61	uP_nSTANDBY	Input
90	uP_PCC_nCE2B	Output
91	uP_PCC_nCE1B	Output
94	uP_PCC_nCE2A	Output
92	uP_PCC_nCE1A	Output
89	uP_PCC_nCE2	Input
81	uP_PCC_nCE1	Input
78	uP_PCC_nSLOTA	Input
79	uP_PCC_nSLOTB	Input
64	uP_nPWFL	Output
8	uP_PCC_nOE	Input
9	uP_PCC_nIORD	Input
86	uP_PCC_BVD1	Input
87	uP_PCC_BVD2	Input
95	NAND_nWE	Output
93	NAND_nRE	Output
96	NAND_nCE	Input
45	CPLD_TDI	JTAG
47	CPLD_TMS	JTAG
48	CPLD_TCK	JTAG
83	CPLD_TDO	JTAG
24	CDRST_1	unused
28	DGE_1	unused
20,38,51,88,98	3.3V	Vi/o
57,26,5	1.8V	Vcore
21,31,62,69,84,100,25,75	GND	GND

